Voltage-Tunable Quantum-Dot Array by Patterned Ge-Nanowire-Based Metal-Oxide-Semiconductor Devices

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We report the fabrication of an array of highly scaled Ge-nanowire-based (radius ∼ 25 nm) vertical metal-oxide-semiconductor devices that can operate as voltage-tunable quantum dots (VTQDs) at room temperature. The electrons in such nanowires experience geometrical confinement in the radial direction, whereas they can be confined axially by tuning the applied bias to manipulate the quantum states. Such three-dimensional confinement of electrons is confirmed from the steplike responses in the room-temperature capacitance-voltage (*C*-*V*) characteristics at relatively low frequency (200 kHz). Each step is observed to encompass convolution of the quantized states occupying about six electronic charges. Such ultrasmall capacitance (∼aF) is measured by exploring a technique that utilizes the method of removing frequency dispersion. Details of such carrier confinement are analyzed in the current work by theoretically modeling the device's transport properties based on the nonequilibrium Green function formalism.

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I. INTRODUCTION

Semiconductor quantum dots (QDs) are regarded as the primary unit for a wide range of advanced and emerging technologies, including electronics [1], optoelectronics [2], photovoltaics [3], and biosensing applications [4], as well as the domain of *q*-bit-based quantum information processing [5]. Such QDs are suitable for several advanced device applications for their unique property of confining carriers three dimensionally to create discrete quantum states. However, the realization of such QDs in practice exhibits serious challenges regarding their fabrication in arrays with desired scalability and repeatability, as well as control over the quantum states at room temperature. In this context, ultrascaled nanowire-based vertical metal-oxide-semiconductor devices are theoretically explored to operate as voltage-tunable quantum dots, even at room temperature [6,7]. The electrons in such nanowires experience geometric confinement in the radial direction, whereas they can be confined axially by tuning the applied bias to manipulate the quantum states.

On the other hand, the advancement of nanotechnology has provided a systematic route for the controlled fabrication of several nanostructures, including two-dimensional (2D) nanofilms, one-dimensional (1D) nanowires or nanotubes, and zero-dimensional quantum dots, by adopting top-down or bottom-up approaches, as well as through hybrid technology [1,8–10]. Among such miniaturized structures, special efforts have also been made to realize voltage-tunable quantum dots (VTQDs) to achieve appropriate control over their quantum states [11–15]. However, fabricating patterned arrays of such nanostructures of the physical dimensions that exhibit quantum effects at room temperature is still a challenge. The current decade has witnessed several reports on fabricating nanowire arrays, although their radii are in the order of 50 nm, which are too large for such quantum confinement to be observed [16–20].

In this context, here, we report on the realization of voltage-tunable quantum confinement of electrons at room temperature by fabricating an array of vertical Ge-nanowire-based (radius approximately 25 nm) metal-oxide-semiconductor (Ge NWMOS) devices on *p*-Si substrate. The patterned array of sites for such nanowire formation is scaled down in the current work by optimizing the *e*-beam lithographic process to obtain nanowires with radii in the order of the Ge excitonic Bohr radius (i.e., 24.3 nm [21]). The vertical NWMOS devices are fabricated by employing the *e*-beam evaporation technique to deposit Ge and SiO_2 sequentially on *p*-Si substrate, followed by dc sputtering of Pt over it; for the ground contact, Al is deposited on the back face of the substrate through the thermal evaporation technique. It is noteworthy that Ge is chosen as the semiconductor nanowire material due to its large excitonic Bohr radius, and SiO_2 is selected as an insulator, since it is expected to reduce tunneling leakage significantly due to its larger electron effective mass [7]. On application of a positive bias at the metal terminal of such

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a NWMOS, the electrons are three-dimensionally confined in the quantum well created at the semiconductor-oxide (Ge NW/SiO_2) junction due to geometrical quantization in two transverse dimensions (i.e., the radial directions of the nanowire) and electrostatic quantization along the nanowire axis. For a particular NWMOS, the positions of the quantum states in the energy space significantly depend on the shape of such quantum wells, and the corresponding electrostatic quantization can be manipulated by varying the applied bias, leading to the formation of VTQDs [6,7].

II. SCHEME OF NWMOS-BASED VTQDs

A schematic of such NWMOS-based VTQDs is shown in Fig. 1(a), along with the energy-band diagram of the device under unbiased conditions, which is depicted in Fig. 1(b). In the current work, the applied voltage is varied to study the entire range of the so-called "accumulation-to-inversion" region of MOS capacitance. Generally, the device to exhibit such transitions requires the semiconductor to be of a specific doping concentration, i.e., p or n type. However, the fabrication of ultrascaled semiconductor nanowires of a particular type with controlled doping is technologically very challenging, since even a single dopant results in a very high doping concentration (e.g., $\sim 10^{16}$/cc) in such nanostructures.

In this context, an array of Ge NWMOS devices Are developed in the current work on p-Si substrate based on a scheme of nanowire doping, which is conceptually different from conventional p- or n-MOS technology. The intrinsic Ge nanowire here forms a heterojunction with the p-Si substrate, which results in a hole-dominated (i.e., p type) semiconductor; this is attributed to the inherent valence-band offset of 0.5 eV at the Ge NW/p-Si interface, as shown in Fig. 1(b).

While applying a negative bias at the metal terminal, such holes remain accumulated within Ge nanowires, leading to the development of the "accumulation" capacitance in the device. However, during the transition from negative to positive bias, such holes tend to move towards the substrate, where the potential barrier at the Ge/p-Si interface due to the valence-band offset of 0.5 eV creates a semiconfining region. When further positive bias is applied at the metal terminal of the NWMOS, electrons are confined three dimensionally in the quantum well created at the semiconductor-oxide (Ge NW/SiO_2) junction due to voltage-driven band bending in the nanowire, as illustrated in Fig. 1(c). It is noteworthy that, under such conditions (i.e., positive bias), the holes are 2D-confined in radial directions, whereas they are free to move along the nanowire axis, thereby exhibiting 1D density of states (DOS); however, the 3D-confined electrons observe

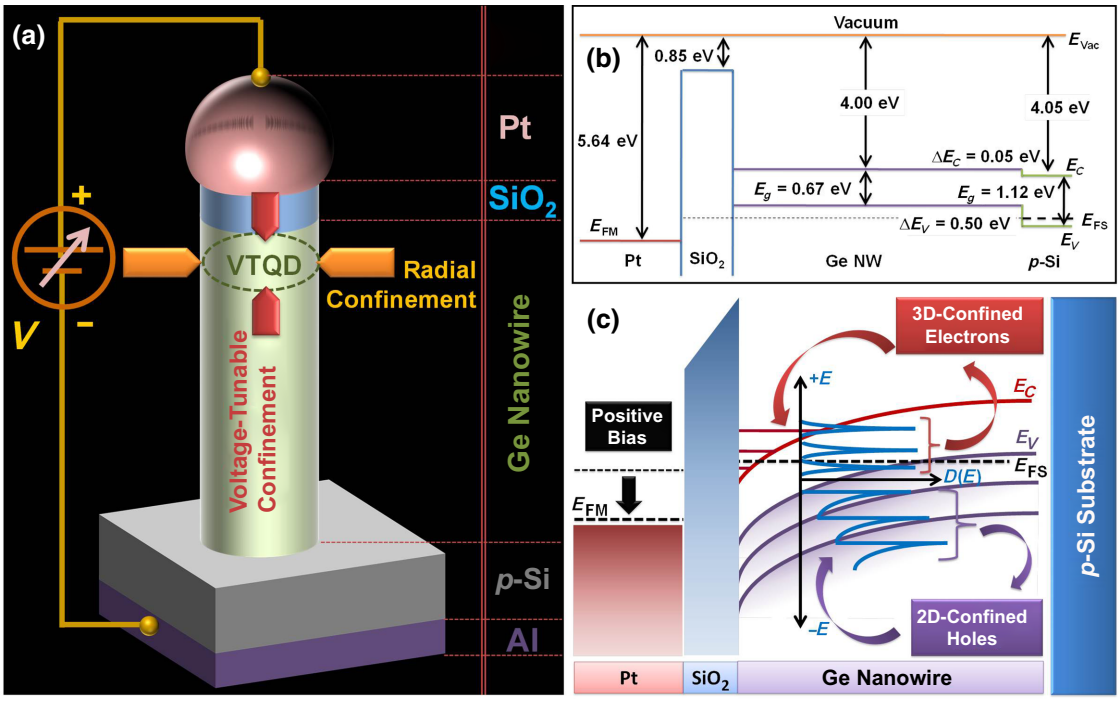

FIG. 1. (a) Schematic of Ge-nanowire-based MOS device on Si substrate, indicating the formation of VTQDs near the Ge NW/SiO_2 interface due to the combined effect of structural and electrical confinement along radial and longitudinal directions, respectively. (b) Energy-band diagram of the NWMOS device under unbiased conditions, illustrating Si and Ge valence- and conduction-band offsets. (c) Energy-band diagram for positive bias applied on the metal, depicting regions of 3D-confined electrons and 2D-confined holes, along with their respective local density of states; 3D-confined electrons form VTQDs.

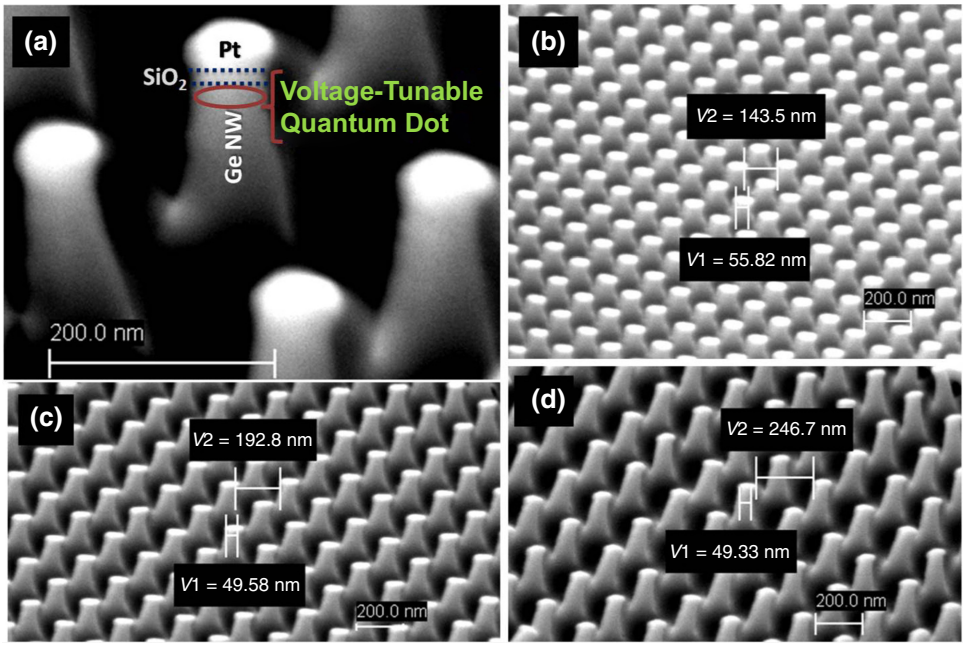

FIG. 2. (a) FESEM image of $Pt/SiO_2/Ge$ NW vertical MOS device, indicating the formation of voltage-tunable quantum dot region on top of Ge nanowires beneath the oxide-semiconductor interface. Image is captured at a magnification of 120×10^3 times and extra high tension of 3 kV. FESEM images of the array of NWMOS-based VTQD devices with inter-nanowire spacings of (b) about 150 nm, (c) about 200 nm, and (d) about 250 nm. Such devices are patterned using an electron dose of 65k $\mu c/cm^2$. Nanowire radii for all cases are about 25 nm (distribution of nanowire radii is given in Ref. [22]).

the DOS as a delta function in energy space around the respective quantum states [see Fig. 1(c)]. Therefore, the resulting "inversion" capacitance is the manifestation of electron confinement in such quantum states created within the NWMOS and can be manipulated by applying an appropriate voltage to the device.

III. FABRICATION AND CHARACTERIZATION

The patterned arrays of Ge nanowire MOS devices for room-temperature VTQD applications are fabricated by optimizing the *e*-beam lithographic process to achieve the desired order of nanowire radii followed by a top-down approach of the *e*-beam evaporation technique to deposit Ge and SiO_2 sequentially on *p*-Si substrate and thereafter dc sputtering of Pt for NWMOS formation. The process flow for such fabrication is described in detail in Ref. [22].

The field-emission (FE) SEM images of such $Pt/SiO_2/Ge$ nanowire MOS structures fabricated as patterned arrays on *p*-Si substrate with various interspacings are shown in Fig. 2. Different material regions of such voltage-tunable quantum dots are indicated in Fig. 2(a), while Figs. 2(b)–2(d) depict arrays with interdot spacings of about 150, 200, and 250 nm. The average radius of Ge nanowires is about 25 nm, with a standard deviation of about 5 nm [22], which correlates with the excitonic Bohr radius of Ge (24.3 nm). Such variation of interdot spacing offers a desired array of VTQD-based devices, as per the requirement for emerging technological applications and large-scale production.

Figure 3(a) presents the TEM image of a single NWMOS structure, where the different regions of Ge nanowire, SiO_2, and Pt are indicated, whereas the corresponding selected-area electron diffraction (SAED) pattern obtained from the Ge nanowire is shown in Fig. 3(b). It is apparent from Fig. 3(b) that such SAED spots are arranged in a circular ring, which is attributed to electron diffraction from the nanowire [18] and the corresponding *d* value indicates the [200] plane of Ge [23].

The elemental content of such a single nanostructure is shown in Fig. 3(c) by plotting the characteristic peaks of energy-dispersive x-ray (EDX), measured *in situ* under TEM, which confirm the presence of a considerable weight percentage (approximately 25%) of Ge along with the top-electrode metal Pt (approximately 19%); however, the x-ray peaks characteristic of Si and O are negligibly small. Furthermore, the XRD plot, shown in Fig. 2(d), exhibits a single peak at $2\theta = 62.6°$, confirming the formation of the [400] plane of Ge nanowire (JCPDS 72-1089) on [400]-Si ($2\theta = 69.6°$) substrate (JCPDS 01-0791), which also corroborates with the direction of the crystal plane obtained from the SAED pattern.

IV. CAPACITANCE MEASUREMENTS

The capacitance-voltage (*C-V*) characteristics of a single Ge NWMOS are experimentally obtained by performing the measurement inside the FESEM chamber under high vacuum (approximately 10^{-6} mbar) at room temperature. The contacts for such measurements are made by tungsten (W) nanoprobes attached to micromanipulators connected to the semiconductor characterization system (SCS) [24]. After careful setting of the probe contact, the electron beam is blanked between measurement to avoid any perturbing contribution From charges from the background source of the FESEM *e* beam. However, it is noteworthy that the SCS measuring apparatus generally overestimates the capacitance of ultrascaled NWMOS

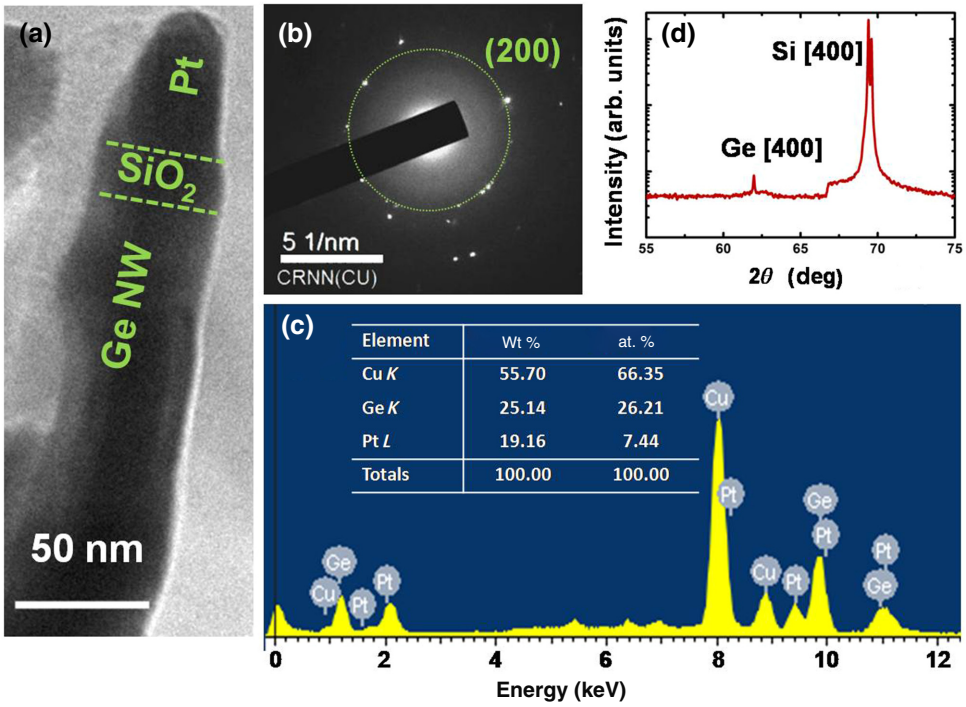

FIG. 3. (a) TEM image of single-nanowire MOS, showing Ge (semiconductor), SiO_2 (oxide), and Pt (metal) regions, where nanowire radius and thickness of oxide material are observed to be about 25 and 20 nm respectively. (b) SAED pattern of Ge nanowire, showing a ring with bright spots, corresponding to the [200] plane of Ge. (c) Results of EDX measurements performed *in situ* under TEM, along with atomic and weight percentages of relevant materials. (d) Plot of XRD profile of patterned NWMOS, confirming Ge [400] plane at $2\theta = 62.6°$ on [400] plane of Si substrate.

significantly (in multiplicative order) due to a large contact resistance (Si/Al/W). Such overestimated capacitance values obtained from the direct measurements can, however, be corrected to obtain the "real capacitance" by utilizing the method of removing frequency dispersion associated with interface traps by reconstruction of lossy MOS capacitance [25]. In fact, the equivalent circuit, as perceived by the SCS measuring instrument, cannot appropriately describe the real MOS device exhibiting frequency dispersion, and thus, needs to be modified by a relevant equivalent circuit to remove such frequency dispersion. Therefore, all measured capacitance and conductance values are overestimated by a multiplicative factor, "f," which cannot be obtained directly from the SCS instrument and requires the method of removing frequency dispersion for capacitance reconstruction. This methodology is utilized in the current work to estimate the C-V characteristics of a single Ge NWMOS [22]. At this point, it is noteworthy that such a multiplicative factor for the present Ge nanowire MOS device is $f = 2 \times 10^6$, independent of all frequencies and voltages, which suggests that the real capacitance should be in the aF range, although the measured capacitance was in the pF range.

The corrected capacitance-voltage characteristics are plotted in Fig. 4(a), illustrating the high- (1 MHz) and low- (200 kHz) frequency responses of such devices in the accumulation-to-inversion region [22]. It is noteworthy that, in the present case, frequencies belonging to the order that corresponds to the inverse of the minority carrier lifetime of Ge (approximately 1 μs [26]) are considered to be "low" and those above such a range are assumed to be "high". It is apparent from Fig. 4(a) that the low-frequency (200 kHz) C-V characteristics exhibit a "steplike" behavior in the inversion region (e.g., steps @ +2, +4 V), indicating strong 3D confinement of electrons in the quantum well created at the Ge nanowire/SiO_2 interface at room temperature. The capacitance steps arise as a result of voltage-driven lowering of the quantized states below the Fermi level and are occupied at room temperature discretely.

Careful investigation shows that each major step in the C-V curve exhibits a leap of about six electronic charges per volt and is partially smoothed by a number of smaller convoluted steps. Such smaller steps originate due to radial (i.e., geometrical) confinement, whereas the major steps are attributed to axial (i.e., electrical) confinement tunable by the applied voltage. However, such a 3D-quantization effect diminishes significantly at high frequency (exhibiting very small humps) since at high frequencies, the electrons, being the minority carriers can not follow the applied ac signal [27]. On the other hand, the C-V curves for both low and high frequencies exhibit hump(s), while transiting from accumulation to inversion; the latter (i.e., high-frequency humps) is reduced, but not removed completely. Such humps arise from interface traps and the confinement of holes at the Ge/p-Si interface (due to the valence-band offset of 0.5 eV); the contribution of the former is diminished at high frequency, whereas that of the latter subsists [22,28]. Such a confinement effect is contributed to by both "light" and "heavy" holes, leading to different humps being convoluted in the C-V curve [Fig. 4(a)]. At this point, it is noteworthy that intrinsic Ge nanowires grown by the vapor-liquid-solid method are generally hole dominated due to the

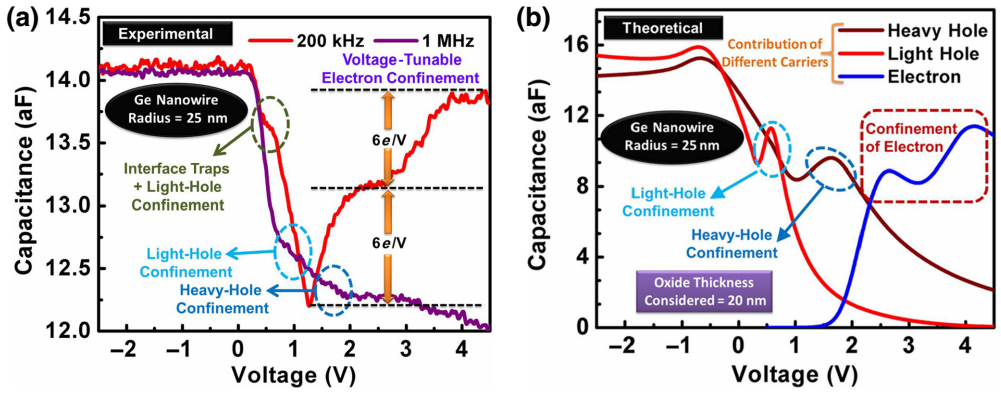

FIG. 4. (a) Plot of *C-V* characteristics measured *in situ* under FESEM at room temperature for 200 kHz and 1 MHz frequencies, showing accumulation-to-inversion region. Low-frequency response of *C-V* curve exhibits steplike nature, indicating 3D confinement of electrons with about 6*e* per volt per step in the VTQD formation region. Humps created due to interface traps and hole (light-heavy) confinement are also shown. (b) Theoretical plot of *C-V* characteristics of single-nanowire MOS device of identical dimensions obtained from the analytical model based on NEGF formalism. In such a plot, contributions of different carriers (heavy holes, light holes, and electrons) in the net capacitance behavior are shown along with experimental results.

presence of surface states exhibiting significant hysteresis in their electrical characteristics [29–31]. However, no hysteresis is observed in the electrical characteristics of the present Ge NWMOS devices fabricated by *e*-beam deposition under high vacuum, indicating a negligible impact of such surface states.

V. THEORETICAL MODELING

The nature of such variation of NWMOS capacitance with applied bias is investigated theoretically in the current work by solving quantum-electrostatic equations self-consistently based on the nonequilibrium Green function (NEGF) formalism [22]. The theoretical results are plotted in Fig. 4(b), illustrating the contributions of an electron, a heavy hole, and a light hole to the net capacitance of the device. Such a theoretical model considers the Ge nanowire to be an "active device" coupled to the p-Si substrate as the "reservoir". The corresponding retarded Green functions of the NWMOS for electrons in the conduction band and holes in the valence band are given by [22]

$$\underline{\underline{G}}^{C}(E_e) = \underset{\underline{\underline{\Sigma}}_{p\text{-Si}}(E_e)\to 0}{Lt}[E_e\underline{\underline{I}} - \underline{\underline{E}}^{C} - \underline{\underline{\Sigma}}_{p\text{-Si}}(E_e)]^{-1}, \quad (1)$$

and

$$\underline{\underline{G}}^{V}(E_h) = [E_h\underline{\underline{I}} - \underline{\underline{E}}^{V} - \underline{\underline{\Sigma}}_{p\text{-Si}}(E_h)]^{-1}, \quad (2)$$

where E_e and E_h are the total electron and hole energies varying from the band edges to +/− infinity, respectively. $\underline{\underline{E}}^{C}$ comprises all 3D-quantized energy states created in the voltage-tunable quantum well in the conduction band, and $\underline{\underline{E}}^{V}$ represents the matrix consisting of the 2D-confined valence subbands. The self-energy corresponding to coupling between electrons and holes of the Ge NW and p-Si substrate are represented by $\underline{\underline{\Sigma}}_{p\text{-Si}}(E_e)$ and $\underline{\underline{\Sigma}}_{p\text{-Si}}(E_h)$, respectively. It is noteworthy that the electron self-energy is considerably smaller for two reasons: first, electrons are minority carriers in p-Si and, second, the quantized energy states within the well of the nanowire exhibit significant mismatch with possible electron-energy states in the Si substrate due to voltage-induced band banding. Therefore, the density of states in the conduction band, which is equivalent to the imaginary part of the Green function [32] is

$$\underline{\underline{D}}^{C}(E_e) = 2\delta(E_e - \underline{\underline{E}}^{C}), \quad (3)$$

indicating the 3D quantization of electrons. However, the occupancy of such electrons depends on whether the quantized states are near or below the p-Si Fermi level and controlled by the applied bias, which finally manifests as the steplike behavior of device capacitance [Figs. 4(a) and 4(b)]. The comparison of such experimental and theoretical plots of capacitance suggests that the prominent hump at about 0.5 V for low frequency originates due to the confinement of light holes, whereas heavy-hole confinement corresponds to the convoluted hump at about 1 V observed for high frequency. Such a frequency response is attributed to the Ge NW↔p-Si hole transmission lifetime [22]:

$$\langle t\rangle \equiv \frac{\hbar}{2}\mathrm{Im}[-\underline{\underline{\Sigma}}_{p\text{-Si}}(E_h)]^{-1}, \quad (4)$$

which significantly depends on the mismatch of the hole effective masses (m_h^*) of Ge and Si.

The Ge NW↔p-Si coupling is stronger for heavy holes in comparison with light holes due to their lesser effective-mass mismatch ($m_h^{\mathrm{HH}} * (\mathrm{Ge}) = 0.33$; $m_h^{\mathrm{LH}} * (\mathrm{Ge}) = 0.043$; $m_h^{\mathrm{HH}} * (\mathrm{Si}) = 0.49$; $m_h^{\mathrm{LH}} * (\mathrm{Si}) = 0.16$ [33]), resulting in

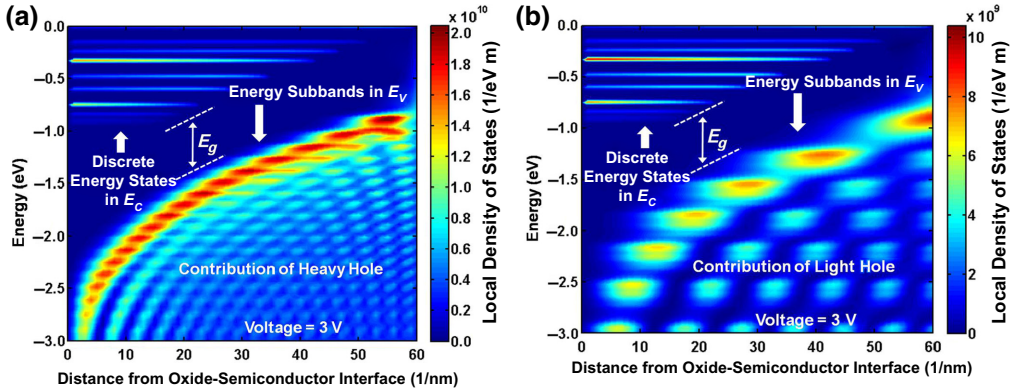

FIG. 5. Plots of local density of states in energy space with distance from oxide-semiconductor interface for 3D-confined electrons and 2D-confined holes: (a) heavy holes and (b) light holes. Applied voltage at the metal terminal is considered to be 3 V. Results are obtained from NEGF-based analytical model developed in the current work. LDOS for electrons show spikes for created 3D-confined discrete states in the voltage-tunable quantum-well region, whereas such LDOS for holes are broadened due to their free longitudinal motion towards the substrate. Such broadening is observed to depend significantly on hole effective-mass (i.e., light-heavy hole) mismatch between Si and Ge.

greater broadening of hole subbands associated with reduced contact resistance [34], thereby exhibiting the corresponding frequency responses. To illustrate the overall charge quantization and available energy space in the present NWMOS device (for a given voltage of 3 V), the variation of the local density of states (LDOS) with energy along the nanowire axis from the SiO_2/Ge NW interface is plotted for both the 3D-confined electrons and 2D-confined light and heavy holes in Figs. 5(a) and 5(b), respectively.

VI. CONCLUSION

An array of voltage-tunable quantum dots (VTQDs) based on ultrascaled (radius $\sim$ 25 nm) Ge NWMOS devices with controlled variation of interspacing are fabricated, which exhibit strong quantum confinement at room temperature. The steplike behavior of capacitance shows about six electrons per step to be confined per volt in such devices. The confinement properties of different types of carriers are theoretically investigated on the basis of the NEGF formalism, which provides physical insights into quantum transport in such devices. The scheme of developing such an array of VTQDs with relevant materials and geometric dimensions can be further utilized in advanced quantum technologies, including advanced photodevices [6,35], as well as q-bit generation for quantum information processing.

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