Atomistic Mechanism of 4*H*-SiC/SiO_2 Interface Carrier-Trapping Effects on Breakdown-Voltage Degradation in Power Devices

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The SiC/SiO_2 interface in the termination area is a crucial component in limiting high-temperature reverse-bias (HTRB) reliability for SiC-based high-voltage devices. However, the atomic structure and carrier-trapping behavior of the SiC/SiO_2 interface defects therein and the underlying physical mechanisms of breakdown-voltage (V_{BD}) variation are still largely unclear. Here, the SiC/SiO_2 interface defects of 4*H*-SiC gate turn-off (GTO) thyristors before and after HTRB stress are investigated by transient capacitance measurements and density-functional-theory (DFT) calculations. It is found that the bias stress at 4.4 kV enlarges the interface state density at $E_C - 0.60$ eV to $E_C - 1.33$ eV by electron capturing. As a result, the negative interface charge is generated. As high-resolution transmission electron microscopy reveals the presence of excess carbon near the SiC surface, DFT calculations are focused on carbon-related interface defects to clarify the atomic and electronic structures of the SiC/SiO_2 interface trap and assign them to negatively charged excess split-interstitial carbon at the interface. Furthermore, technical computer-aided-design simulation further proves that the negatively charged SiC/SiO_2 interface defect is the main cause for the observed V_{BD} degradation after the HTRB test, which leads to a strong electric field crowding effect. These results not only provide deep physical insights underlying V_{BD} degradation in HTRB-stressed high-voltage devices, but are also of significant importance in the optimizations of device structure and oxidation technology for SiC/SiO_2 interfaces in high-voltage SiC devices.

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I. INTRODUCTION

Excellent physical properties make silicon carbide (SiC) a promising candidate for high-power and high-temperature applications, such as power supplies, photovoltaic converters, air conditioners, and motor controls for elevators and railcars. The native SiO_2 oxide makes SiC distinguishable from other wide-band-gap semiconductors, which can be used as the dielectric layer in metal-oxide-semiconductor field-effect transistors (MOSFETs) or applied in the terminal structure for high-voltage SiC devices [1]. However, thermal oxidation generates an unacceptably high density of SiC/SiO_2 interface states, giving rise to a complex energy distribution [2–4]. Additionally, the smaller energy-band offsets between SiC and SiO_2 result in a reduced barrier for carriers to scale and contribute to leakage-current and gate-dielectric degradation [5,6]. These two aspects lead to two kinds of severe reliability hazards for SiC power devices: first, a decrease in breakdown voltage (V_{BD}) under high-temperature reverse-bias (HTRB) stressing [7–9], and, second, time-dependent dielectric breakdown and threshold-voltage (V_{th}) instability under high-temperature gate bias (HTGB) for SiC MOSFETs [10–12]. Herein, it should be noted that HTRB and HTGB are routinely performed qualification tests and well-known reliability hazards for power devices. However, while the gate-dielectric instability has been exhaustively addressed [10–15], reports on the role of SiC/SiO_2 interface defects in V_{BD} stability of an actual power device are relatively limited because of the complexity of fabricating high-voltage devices, to a certain extent. With the increase in blocking voltage, higher electrical stress on termination makes V_{BD} degradation more intractable. Therefore, a comprehensive understanding of the physical origin and electronic properties of interface defects responsible for V_{BD} changes is crucial for

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the further development or improvement of higher-voltage SiC power devices.

Reports in the literature suggest two main classes of SiC/SiO_2 interface defects as carrier traps: near-interface traps (NITs) and deep traps from carbon clusters [16–18]. The NIT gives rise to a narrow and dense state distribution near the conduction-band minimum of 4*H*-SiC and is suggested to originate from border traps in SiO_2 and be located within less than 1 nm distance from the interface plane [19]. Carbon clusters are proposed to account for the interface-state spectrum throughout the SiC band gap, with several distinct energy peaks [16]. The position of the upper filled electron states is also suggested to depend on the cluster size [16,20]. However, an atomic level understanding of carrier-trapping effects by the SiC/SiO_2 interface defects on breakdown-voltage degradation has not been reported either experimentally or theoretically so far.

This work investigates the SiC/SiO_2 interface defect in the termination area and its influence mechanisms on the V_{BD} value of 4*H*-SiC gate turn-offs (GTOs) subjected to HTRB tests. The SiC/SiO_2 interface defects before and after HTRB stress are probed by deep-level transient spectroscopy (DLTS), which can easily distinguish between interface and bulk defects in SiC [21]. High-resolution transmission electron microscopy (TEM) and density-functional theory (DFT) calculations are performed to clarify the atomic scale structures of SiC/SiO_2 interface defects. Finally, technical computer-aided-design (TCAD) simulations are carried out to validate the influence of negatively charged SiC/SiO_2 interface defects on V_{BD} degradation for SiC power devices. The combination of in-depth analysis of device performance, spectroscopy data, microstructure observation, and theoretical calculations in this work presents a physical and systematic understanding of correlations between SiC/SiO_2 interface defects and overall device behavior.

II. EXPERIMENTAL AND THEORETICAL APPROACH

A. Device fabrication

A simplified cross-section view of the fabricated 4*H*-SiC GTOs is shown in Fig. 1. A *p*-*n*-*p*-*n* structure is formed by epitaxial growth on 4 inch 4° off-axis *n*+4*H*-SiC substrate in one continuous run to reduce the number of defects at the interface between neighboring layers. The *p*-type drift epilayer is 40 μm thick and has an Al doping of 2×10^{14} cm^{-3}. Subsequently, a 2-μm *n*-type base layer is grown with a nitrogen doping concentration of 2.3×10^{17} cm^{-3}, followed by the growth of a 1×10^{19}-cm^{-3} Al-doped *p*-type anode layer. The structure is formed by first etching through the anode layer down to the *n* base. Then, sloped etching is performed through the *n* base at the edge of the device for edge termination. Subsequently,

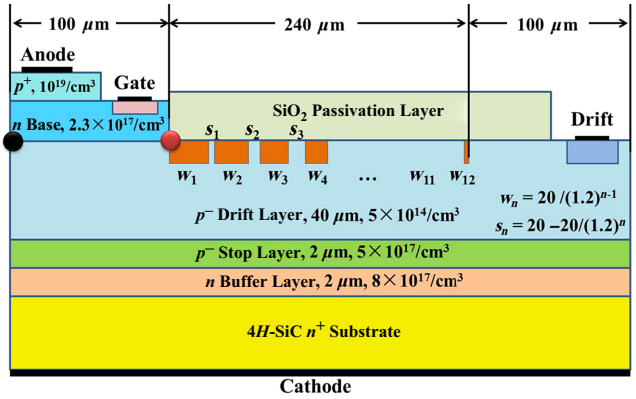

FIG. 1. Schematic view of 4*H*-SiC GTO device with junction-termination-extension (JTE) structure.

thick oxide layers are patterned and used as ion-implant masks to create highly doped regions of *n*-type contacts for the gate, and to form the multiple-floating-zone (MFZ) JTE by a single pattern-implant step and activation annealing at 1650 °C for 30 min [22]. The MFZ JTE structure has 12 zones, with a constant doping concentration of 2×10^{17} cm^{-3}. The widths of the consecutive zones follow geometric progression and decrease by a ratio (α) of 1.2, with a width of 20 μm for the first ring (w_1). Then, the SiO_2 passivation layer at the termination is first formed by 1100 °C wet thermal oxidation and then deposited by plasma-enhanced chemical vapor deposition, with a total thickness of approximately 0.6 μm. Finally, the ohmic contact on the drift is formed through Al implantation and Ni/Ti/Al stack deposition by magnetron sputtering.

B. HTRB stress and device performance test

The HTRB test is conducted at 150 °C and under a bias stress of −4.4 kV on the cathode, which is about 85% of the breakdown voltage in the fresh device (∼5.2 kV), with the anode and gate shorted and grounded. The leakage current ($I_{leak.}$) is recorded *in situ* at different time intervals, with a total stress time of 23 h. Before and after the test, a Keysight B1505A semiconductor parameter analyzer is used to characterize the electrical performance of devices at room temperature. The blocking characteristics are measured in the range of 0 V to 10 kV, and the leakage current is limited to 10 μA. For on-state characteristics, the applied voltage ranges from 0 to 5.5 V, with a trigger current on the gate of −500 mA. Additionally, the capacitance-voltage (*C*-*V*) characteristics of the anode-cathode are monitored from 0 to 3 kV at a modulation frequency of 10 kHz by the MFCMU module in the Keysight B1505A analyzer.

C. DLTS analysis and TCAD simulation

Before and after HTRB tests, capacitance DLTS measurements for the drift-gate (*D*-*G*) diode are performed by

using a Fourier-transform DLTS system, where the signal might originate from both bulk defects in drift and SiC/SiO_2 interface defects in the terminal area. A Phystech FT1030 DLTS system is used here; this system is equipped with a Boonton 72 B capacitance meter with an ac test signal of 1 MHz. DLTS spectra are obtained by temperature scanning from 100 to 750 K, whereby capacitors are repetitively pulsed from a reverse voltage V_R to filling pulse V_P, with a duration of filling time t_p. The measured capacitance transient signal following the bias pulse is then used to calculate the DLT spectrum by Fourier transform. For hole-trap detection, the applied filling pulse voltage V_P and reverse bias V_R are 2 and 15 V, respectively. To probe the electron trap, i.e., minority carrier trap, a forward bias of -5 V is applied on the G-D (n^+-p) junction to inject electrons into the p-type drift layer with a filling time, t_p, of 20 ms [23,24]. The sampling period, t_w, of the bias pulse from V_R to V_P is 1.5 s. To clarify the nature of the deep-level defect, isothermal measurements are performed at 550 K by varying the filling time, t_P, from 10^{-6} to 1 s, while V_P and V_R are kept constant at -5 and 15 V, respectively.

Then, a two-dimensional simulator, Sentaurus Device, is used to investigate the effects of positive and negative SiC/SiO_2 interface charges on V_{BD} and the electric field distribution, with a variable density in the order of 10^{12} cm^{-2}. A protocol is used for V_{BD} simulation, where V_{BD} is defined as the anode-cathode voltage (V_{AC}) corresponding to $I_{leak.} = 10$ μA. The key parameters for the cell and JTE structures are described in Sec. II A. These two structures are described using the x-y coordinates in the simulation, where x is the coordinate parallel to the SiC/SiO_2 interface and y is the coordinate perpendicular to the SiC/SiO_2 interface. The origin of x-y is the leftmost edge at the surface of SiC, marked as a black dot in Fig. 1. Variable amounts of net interface charges are uniformly introduced along the SiC/SiO_2 interfaces in the JTE structure ($x = 100$–340 μm are shown in Fig. 1), and the corresponding V_{BD} values are simulated. Then, electric field distributions along the SiC/SiO_2 interface, as a function of interface charge densities, are calculated under $V_{AC} = 5.2$ kV. The models used in the analysis include an incomplete impurity ionization model, a carrier generation-recombination model, a concentration-dependent mobility model, and a high-field saturation model. All simulations are done at a default temperature of 25 °C.

D. TEM observation and theoretical approach of SiC/SiO_2 interface

The SiC/SiO_2 specimens adopting the same oxidation process as that described in Sec. II A are selected for cross-section TEM observation. Specimens are prepared using the *in situ* focused-ion-beam (FIB) lift-out technique with a Thermo Scientific Helios G4 HX double-beam FIB. Before ion milling, platinum deposition is performed to minimize surface damage. The final thickness of the TEM specimen is about 50 nm. Then, Z-contrast bright-field scanning TEM (STEM) and energy-dispersive spectroscopy (EDS) are performed to characterize the structure and composition of the SiC/SiO_2 interfaces using a Thermo Scientific Themis TEM with an acceleration voltage of 200 kV.

For DFT calculations, the orthorhombic supercell of the SiC/SiO_2 interface is created by stacking α-quartz SiO_2 on top of the Si-terminated (0001) surface of 4H-SiC, with dimensions of $10.94 \times 12.63 \times 48.31$ $Å^3$. The lateral dimensions correspond to the $\sqrt{8} \times \sqrt{32}$ Si (0001) surface unit cell, and there are six Si-C bilayers in the SiC side with a thickness of about 13.1 Å. The thicknesses of the a-SiO_2 and vacuum layers are 15.8 and 19.1 Å, respectively. The bond-density mismatch at the interface is accommodated by the introduction of C or Si atoms, which eliminates all residual dangling bonds. Then, the a-SiO_2 layer, either with or without the transition layer, is heated at 2000 K for 200 ps with an isothermal and isochoric (NVT) ensemble. The heating temperature and duration are sufficient to melt the unit cell of the SiO_2 crystal and remove the memory of the initial crystalline structure. In addition, the melting process can also be investigated to explore the effect of local strain, possibly induced by the creation of the interface.

The models are then optimized using first-principles calculations based on DFT implemented by the Vienna *ab initio* simulation package (VASP) code [25]. The calculations are performed by using the projector-augmented-wave (PAW) method with cutoff energies of 520 eV. The Perdew-Wang (PW91) form of the generalized gradient approximation (GGA) is applied as the exchange-correlation functional [26]. Only the Γ point is taken into account for Brillouin-zone integration because of the large supercell size. The error in the total energy is 10^{-5} eV for the electronic loops. Structure optimization is performed with the conjugate-gradient (CG) algorithm and is kept running until the residue force on each atom is less than 0.05 eV/Å.

Hybrid-functional (HSE06) calculations are adopted to correct the band gaps of SiC, SiO_2, and the SiC/SiO_2 interface. The accuracy of band alignment is assessed through the calculation of the ionization potential (V_{ip}), which is defined formally as the energy difference between the vacuum level, E_{vac}, and the interface valence-band maximum (VBM), namely,

$$V_{ip} = E_{vac} - \varepsilon^s_{VBM}. \quad (1)$$

For a slab model, it is convenient to determine the VBM in a separate bulk calculation and to align it to the electronic structure in the slab calculation through a local reference potential, V_{ref}, to accelerate convergence with the thickness of the slab [27]. Therefore, the average electrostatic

potential of the SiC part of the SiC/SiO_2 interface is aligned to that of bulk SiC and introduced as a common reference. V_{ip} is then calculated as

$$V_{ip} = (E_{vac} - V^s_{ref}) - (\varepsilon^b_{VBM} - V^b_{ref}), \quad (2)$$

where the superscripts "s" and "b" refer to slab and bulk, respectively. It follows that

$$\varepsilon^b_{VBM} - V^b_{ref} = \varepsilon^s_{VBM} - V^s_{ref}, \quad (3)$$

according to which the band-edge positions of the slab can be aligned. The VBM position can be adjusted further by taking into account the difference between V_{ip} calculated with the exchange correlation and the experimental value [27]. The conduction-band minimum (CBM) can then be aligned by using the band gap calculated with the HSE06 functional. This alignment scheme has a negligible effect on the deep defect levels, which are almost unaffected by the band-gap renormalization [28].

The split-interstitial carbon defect is created in interfacial models by inserting a carbon (C) atom near a C atom on the top unoxidized monolayer of the SiC side. The two C atoms share a site. The energy levels are calculated by using the VASP code with the PW91 GGA exchange-correlation functional. However, the capture cross-section σ at the SiC/SiO_2 interface, as the other main fingerprint, is not calculated due to the extremely large size of the supercell (>300 atoms) with the expensive HSE06 functional, based on currently available computational methods [29].

III. RESULTS AND DISCUSSION

A. Device performance after HTRB

Figure 2(a) shows the changes of leakage currents ($I_{leak.}$) at $V_{AC} = 4.4$ kV and $T = 150\,°C$ as a function of stress time. $I_{leak.}$ nearly remains unchanged during initial stressing for 3 h, and then steeply increases with growing stress time, reaching 34.8 μA after a prolonged time of 23 h. After stress, the device is immediately cooled to room temperature in the air, and then the blocking characteristic is measured. The relevant results for the fresh and stressed device are shown in Fig. 2(b). We can see that V_{BD} is remarkably reduced from the initial value of about 5.2 kV to about 4.6 kV by bias stress. Meanwhile, after the HTRB, test the forward voltage drop at 40 A in on-state characteristics is slightly increased from 4.4 to 5.0 V, which is shown in Fig. 2(c).

B. Interface defect characterization and failure analysis

Figure 3(a) shows the DLTS spectra for the *G-D* junction before and after the HTRB test. Two negative DLTS peaks at 310 and 645 K are detected in the p-type drift layer when the diode is in depletion from 15 to 2 V, indicating that they are hole traps. According to the previous investigations reported in the literature [30,31], these two traps are identified as HK0 ($E_V + 0.74$ eV, 1.2×10^{-16} cm^{-2}) and HK4 centers ($E_V + 1.46$ eV, 1.5×10^{-14} cm^{-2}), respectively. The HK0 center is ascribed to interstitial carbon (C_i) related complexes, as it is usually observed after thermal oxidation or carbon implantation, both of which inject C_i into the SiC bulk. The nature of the HK4 level is still uncertain, but it is known to be a *C-V*-related donor defect. A pronounced $E1$ peak at 550 K is probed in the case of minority carrier injection by the forward biased *G-D* junction, meaning that it is an electron trap. In addition, we also find the $E1$ trap in the n-SiC/SiO_2/Al MOS structure as an interface electron-trapping center (not shown here). Additionally, the well-reported Z1/2 center at 290 K ($E_C - 0.64$ eV, 6.5×10^{-14} cm^{-2}) is also present, which is attributed to the double-negatively-charged carbon vacancy (*C-V*) [32,33]. The Z1/2 center has an excellent thermal stability [34], and thus, shows an insignificant change after bias stress at 150 °C, as shown in Fig. 3(a). The same behavior is also

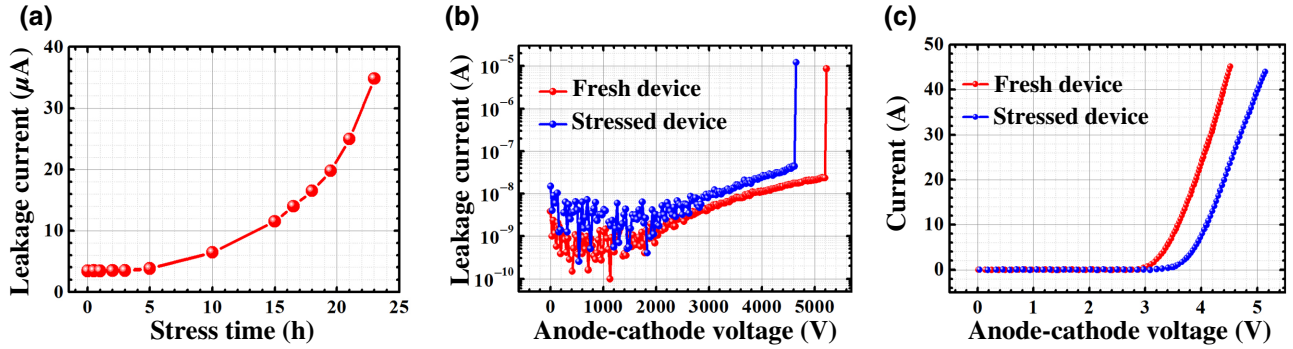

FIG. 2. (a) Evolution of leakage current as a function of stress time at $V_{AC} = 4.4$ kV and $T = 150\,°C$. Typical blocking (b) and on-state characteristics (c) at room temperature for fresh and stressed devices.

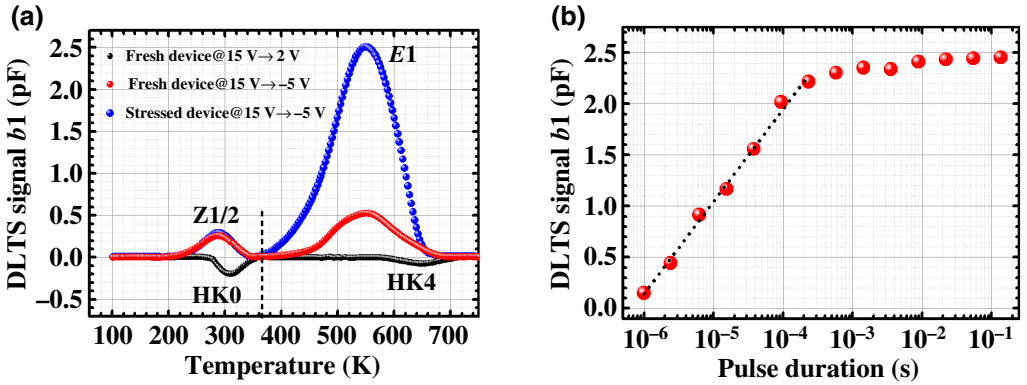

FIG. 3. (a) DLTS spectra for G-D junction before and after HTRB stress. (b) DLTS signal versus filling pulse at 550 K pulsed from −5 to 15 V after the bias test. Herein, the intensities for HK0, HK4, and Z1/2 centers in Fig. 3(a) are multiplied by five for clear presentation.

found for HK0 and HK4 centers. Therefore, we exclude Z1/2, HK0, and HK4 centers as the reason for degraded V_{BD} performance after HTRB stress, and thus, emphasize the broad and significant $E1$ trap.

In both fresh and stressed devices, the $E1$ peak is located at the same maximum position, indicating a similar activation energy (E_T) from the conduction-band edge. Meanwhile, its intensity significantly grows after the HTRB test, i.e., the concentration of electron traps is increased by bias stress. Because the density of dislocation or stacking faults in SiC are usually in the order of 10^3–10^4 cm^{-2} [35,36], extended defects in the drift layer are ruled out as the origin for this trap. As mentioned above, this DLTS peak may result from either point defects in the bulk or SiC/SiO_2 interface defects in the JTE area. To identify the nature of the broad peak, isothermal measurements are performed at 550 K by varying t_p from 1 μs to 1 s and keeping V_R and V_P at 15 V and −5 V, respectively. The recorded DLTS signal $b1$ is plotted as a function of t_p and is shown in Fig. 3(b). Herein, $b1$ is the coefficient for the Fourier transformation of transient capacitance (ΔC) as a function of time and is proportional to ΔC. It is found that the DLTS signal increases proportionally to $\ln(t_P)$ in the range of 10^{-6} to 10^{-4} s, i.e., exhibiting trap-filling kinetics characteristic of extended defects, rather than point defects [37]. Therefore, the electron trap $E1$ in Fig. 3(a) is inferred from the SiC/SiO_2 interface defects in the JTE area. Furthermore, the DLTS amplitude saturates at a t_P value of approximately 500 μs, meaning complete trap filling in the present DLTS measurements, where t_P is selected as 20 ms. This is 3 orders of magnitude lower than the saturated filling time for NITs (≥600 ms) [38]. The associated border traps in SiO_2 may exchange carriers with SiC via an inelastic tunneling process and undergo relaxation between carrier capture and emission, thereby stabilizing the charge state of the NIT trap requires much longer times [38]. In the present DLTS spectra, NITs from border traps in SiO_2 are not detected. According to the reported DLTS characterization, it should be located at 300 to 80 K [39], where no signal is found.

The method of deriving the activation energy, E_T, for interface defects is well established using the Arrhenius plot of e_n/T^2 versus $1/T$ [40–42] and is expressed as

$$E_T = E_C - kT\ln(\sigma_n V_{\text{th}} N_C \tau) \tag{4}$$

where e_n is the hole emission rate, E_C is the conduction-band edge, k is the Boltzmann constant, T is the temperature, σ_n is the capture cross section for electrons, V_{th} is the electron velocity, N_C is the effective density of state of an electron, and τ is the emission rate constant that equals $1/e_n$. τ varies with temperature scanning and can be determined from the capacitance transient curve at each temperature in DLTS measurements. The capture cross sections for electrons in fresh and stressed samples are assumed to be energy independent, with values of 3.2×10^{-18} and 4.5×10^{-18} cm^{-2}, respectively, which are determined from the intercept of the Arrhenius plot of e_n/T^2 versus $1/T$. Following Eq. (4), the emission rate constant, τ, at a certain temperature T in DLTS is then converted into E_T and shown in Table I. In fresh and stressed samples, the interface defects both give rise to deep energy bands, ranging from E_C −0.60 eV to E_C −1.33 eV, with a maximum interface-state density at E_T = 1.06 eV (1.08 eV) corresponding to the DLTS peak temperature. Meanwhile, the density of SiC/SiO_2 interface defects is enlarged by bias stress at 150 °C, as shown in the DLTS spectra [Fig. 3(a)].

Figure 4 shows the change in capacitance-voltage (C-V) characteristics of the anode-cathode before and after the HTRB test. Under this positive bias, only the gate-drift diode is in the depletion mode; therefore, the applied voltage V_{AC} mainly drops between G and D diodes. It can be

TABLE I. Transformed activation energy E_T for SiC/SiO_2 interface defects from the DLTS spectra shown in Fig. 3(a).

	E_T	Peak energy (eV)	σ_n (cm^{-2})
Fresh sample	E_C −0.63 eV to E_C −1.33 eV	1.06	3.2×10^{-18}
Stressed sample	E_C −0.60 eV to E_C −1.31 eV	1.08	4.5×10^{-18}

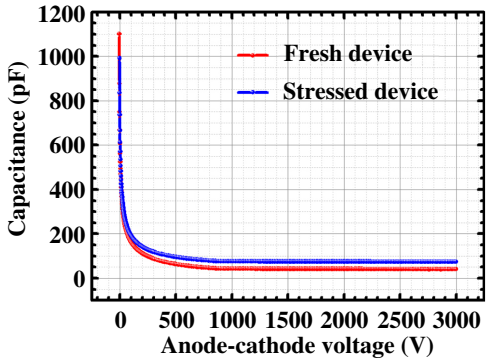

FIG. 4. *C-V* characteristics at frequency of 10 kHz between anode and cathode before and after HTRB test.

seen that C is slightly increased after the test. The measured C is the sum of the termination-area capacitance (C_{TM}) and the active-area capacitance of diodes (C_{GD}). Matsushima *et al.* found that the bias-stress-induced capacitance change (ΔC) remains unchanged with the varying device size, and thus, confirms that ΔC is caused by C_{TM} rather than C_{GD} [43]. Therefore, the change in measured C after the test can be ascribed to C_{TM}. From the increased C after stress, it is inferred that the net negative charge is accumulated in the JTE area. In other words, carrier trapping occurs at the SiC/SiO_2 interface defects of the JTE region. Based on the observed $E1$ trap from interface defects, a simple physical model for charge formation is proposed here. Under a bias stress of $V_{AC} = 4.4$ kV, electrons are injected into the SiC/SiO_2 interface, due to the vertical electric field pointing from SiO_2 to SiC, and are then trapped by interface defects therein. Consequently, HTRB stress leads to an enhanced generation of negatively charged interface defects, showing as the promoted formation of $E1$ defects in Fig. 3. From this aspect, the detected $E1$ SiC/SiO_2 interface defect is suggested to be negatively charged, which is validated below.

Next, TCAD simulation is performed to investigate the influence of charge accumulation at the SiC/SiO_2 interface on V_{BD} after HTRB stress. Figure 5(a) shows the simulated V_{BD} as a function of positively and negatively interface charge density. It can be seen that V_{BD} is greatly affected by the negative interface charge, while it is insensitive to the positive charge. This further confirms that electron trapping by the SiC/SiO_2 interface defects plays a dominant role in the deteriorated blocking characteristics after bias stress, rather than the positive mobile ions, such as sodium ions in SiO_2. This shows good agreement with results in Fig. 4. Additionally, the leakage current begins to increase after a stress time of >3 h. It is far larger than that of the diffusion time for mobile ions moving to the interface, which only needs several minutes [44]. With the increase of the applied stress time, the SiC/SiO_2 interface defects continuously capture electrons due to the direction of the electrical field pointing from the anode to the cathode, thus leading to the promoted formation of negatively charged defects. As a result, V_{BD} is reduced and the relevant leakage current increases, as observed in Fig. 2(a). Figure 5(b) shows the electric field distribution along the SiC/SiO_2 interface at three typical negative charge densities under $V_{AC} = 5.2$ kV. The simulated maximal electric field (E_{max}) is observed at the innermost ring of the JTE region ($x = 100\,\mu$m) in Fig. 5(b), which is labeled as a red dot in Fig. 1. Under the assumption of no interface charges (N_{eff}), the value of E_{max} is 1.65 MV/cm. When the density of negative charge increases, the position of E_{max} remains constant, but its value is significantly increased, reaching 3.9 MV/cm at a N_{eff} value of -1×10^{13} cm^{-2}. In other words, a strong electric field crowding effect is easily formed under the extremely negative N_{eff}, and thus, leads to the V_{BR} reduction. Additionally, the degraded on-state characteristics after HTRB stress shown in Fig. 2(c) can

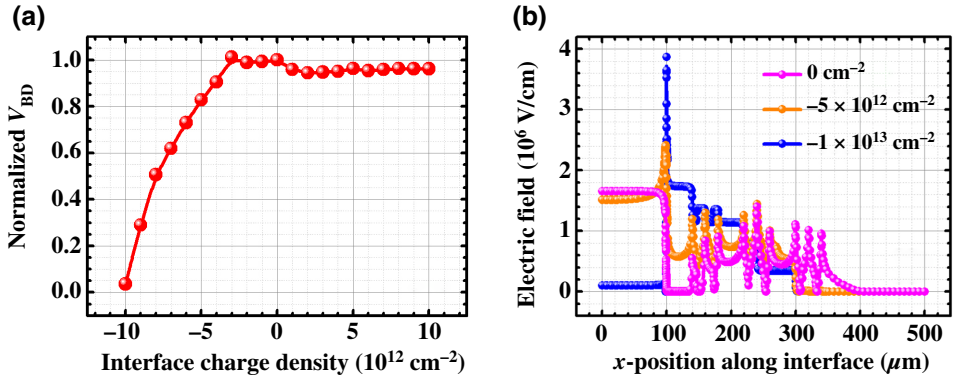

FIG. 5. (a) Simulated V_{BD} as a function of net SiC/SiO_2 interface charge density in the JTE structure. (b) Electric field distribution along the SiC/SiO_2 interface under $V_{AC} = 5.2$ kV at 0, -5×10^{12}, and -1×10^{13} cm^{-2} interface charge densities. Herein, $x = 0$–100 μm and $x = 100$–340 μm correspond to the cell and JTE structure, respectively. Electric field peak is located at the innermost ring of the JTE region ($x = 100\,\mu$m), which is labeled as a red dot in Fig. 1.

also be ascribed to the enhanced formation of negatively charged interface defects. On one hand, they prompt carrier recombination, and thus, reduce the carrier lifetime and associated carrier modulation effects in the SiC drift layer. On the other hand, they may also act as carrier scattering centers and thereby lead to a decrease of carrier mobility in SiC [45].

C. Atomic nature of $E1$ SiC/SiO_2 interface defects

To further clarify the atomic and electronic structures of the SiC/SiO_2 interface trap, we analyze the possible types of defects in the interface by combining HRTEM observations and DFT calculations. Figure 6(a) shows the cross-section STEM image for the SiC/SiO_2 interface taken along the [$1\bar{1}00$] direction. Three distinct zones are revealed from the top down: amorphous SiO_2, the transition layer, and crystalline 4H-SiC. Linear scans of O : Si and C : Si ratios across the SiC/SiO_2 interface shown in Fig. 6(b) imply that the transition layer is about 9 nm thick and presents Si-O-C phases with variable atomic contents. Transition-layer A exhibits a distinctly darker contrast band, which is usually ascribed to structural degradation or partial amorphization [46]. However, transition-layer B presents invisible contrast and is distinguished from the O : Si and C : Si ratio profiles. As seen in Fig. 6(b), a small hump for the C : Si ratio is observed in a few atomic layers underneath the SiC surface, indicating an excess of C in the SiC near the interface, while no obvious carbon incorporation into the SiO_2 film is detected. Consequently, it is inferred that the interface trap detected by DLTS is possibly associated with excess-carbon-related defects on the SiC side of the interface. Zheleva *et al.* also reported that a Si : C ratio peak as high as 1.3 was observed at the SiC side of the 4H-SiC/SiO_2 interface [46]. The excess carbon

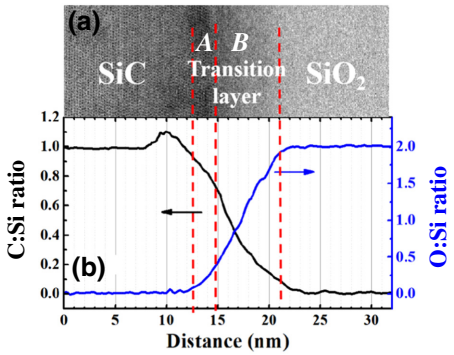

FIG. 6. (a) STEM image of the SiC/SiO_2 interface. (b) Profiles of O : Si and C : Si ratios across the SiC/SiO_2 interface.

density is estimated to be approximately 3×10^{14} cm^{-2} from the small hump for the C : Si ratio shown in Fig. 6. This is an order of magnitude larger than that of the typical interface defect density [47], which is usually attributed to the C-related clusters with different C coordinate numbers. This difference may be associated with the generation of a C-rich Si-C phase during oxidation, as proposed by Biggerstaff *et al.* [48].

Although TEM observation implies that the interface defects may be related to excess-carbon-related defects at the SiC sides, it does not effectively clarify the atomic level structure of these interface defects. Therefore, DFT calculations are performed for this reason. As the absence of NIT traps in DLTS spectra and insignificant carbon incorporation into SiO_2 film shown in Fig. 6(b), the interface models are concentrated at the SiC side of the interface and built with the method in Sec. II D. A typical interface model between amorphous SiO_2 and SiC is shown in Fig. 7(a). The band-gap transition follows that of the

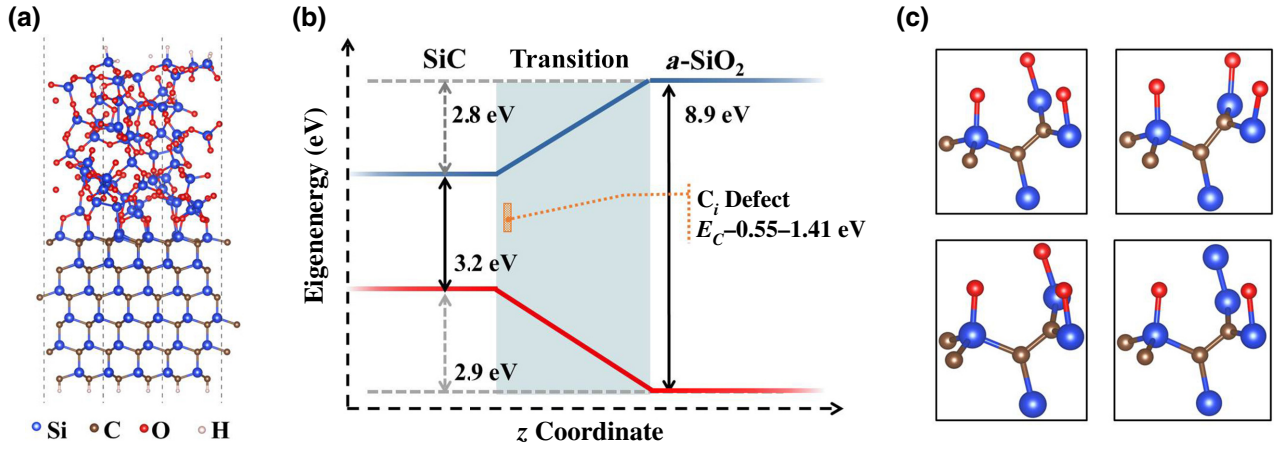

FIG. 7. (a) Interfacial structure and defects in SiC/SiO_2. Blue, brown, red, and white balls represent Si, C, O, and H atoms, respectively. (b) Schematic diagram of band edge as a function of z coordinate. Location and calculated energy levels of interstitial carbon defects are shown in the orange region. CBM and VBM are colored blue and red, respectively. Transition region is colored light green. (c) Detailed structures of several typical interstitial carbon defects with different bond lengths and bond angles.

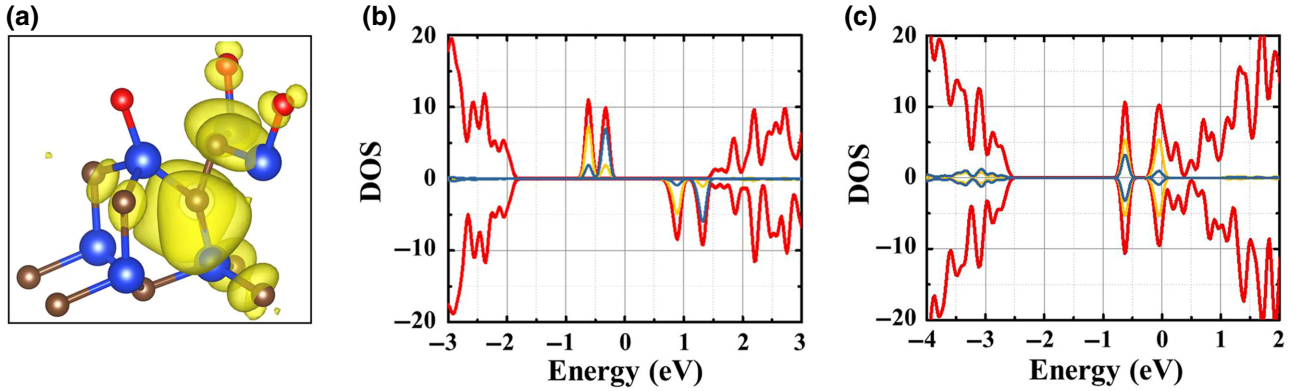

FIG. 8. (a) Charge density, location, and structure of the C_i defect. Blue, brown, and red represent Si, C, and O atoms, respectively. Density of states (DOS) of neutral (b) and negatively charged (c) C_i defects (C_i^{2-}). Total DOS is colored red, and atom-projected DOS of defect C atoms are colored blue and yellow, respectively.

Si oxidation state, where the band gap increases gradually across the transition region. The VBM and CBM are calculated by aligning the average electrostatic potential of the SiC (or SiO_2) layers to that of the bulk material and using the GGA and experimental band-edge offsets, as shown in Fig. 7(b). The band gaps of SiC and a-SiO_2 are 3.26 and 8.90 eV, respectively. The band offsets of the CBM and VBM are 2.74 and 2.90 eV, respectively.

The interstitial C (C_i) defects [Fig. 7(c)] are created in interfacial models by inserting a C atom near a C atom at the unoxidized monolayer of the SiC side, and the two C atoms share one site. Because of the amorphous nature of the transition region, the specific local structure can fluctuate from site to site, and the local structure of C_i defects is not unique. The bond lengths, bond angles, and local environments around the defect will also change. The distance between the two C atoms is about 1.35 Å, and the distance between the C atom and neighboring O and Si atoms ranges from 1.80 to 1.83 Å. In the negatively charged state (−2), the distance between the two C atoms increases (∼1.41 Å) and the distance between the two C atoms and the surrounding Si atoms shortens (∼1.75–1.79 Å). We calculate the defect levels of 11 negatively charged C_i defects in amorphous and crystal interfaces. The calculated energy levels range from $E_C - 0.55$ eV to $E_C - 1.41$ eV [Fig. 7(b)], which is consistent with the experimental results ($E_C - 0.60$ eV to $E_C - 1.33$ eV). As shown in Fig. 8, the C_i defects in both neutral and negative (−2) charge states can induce the midgap states in the SiC band gap. Under a negative electric environment, the neutral C_i defect is nonmagnetic, and their spin-degenerated defect level is located at 1.91 eV above the VBM. Therefore, we assign the interface defect observed in experiments to the negatively charged excess split-interstitial carbon at the interface, which shares a carbon site with a lattice atom in the topmost bilayer of SiC. This shows good agreement with the failure analysis shown in Sec. III B, which assigns the negatively charged interface defects as the main cause for V_{BD} reduction after HTRB stress.

IV. CONCLUSIONS

We systematically investigate the electronic and atomic structure properties of SiC/SiO_2 interface defects in the JTE region and their underlying physical mechanisms on V_{BD} degradation under HTRB stress. SiC/SiO_2 interface defects with an energy distribution of $E_C - 0.60$ eV to $E_C - 1.33$ eV are observed in both fresh and stressed devices by DLTS characterization, and their formation is significantly enhanced by electron capturing during bias stress, although no hole trapping from interface defects is detected. Hence, the negatively charged SiC/SiO_2 interface defect is generated after stress, which easily leads to a strong electric field crowding effect, and thus, V_{BD} reduction, as confirmed by TCAD simulation. Based on the detected excess carbon underneath the SiC interface by TEM and D_{it} distribution, DFT calculations further clarify the atomic structures of this SiC/SiO_2 interface trap, and this can be assigned to negatively charged excess split-interstitial carbon at the interface, which shares a carbon site with a lattice atom in the topmost double layer of SiC.

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