

Hard-Gap Spectroscopy in a Self-Defined Mesoscopic InAs/Al Nanowire Josephson Junction

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Superconductor-semiconductor-nanowire hybrid structures can serve as versatile building blocks to realize Majorana circuits or superconducting qubits based on quantized levels such as Andreev qubits. For all these applications, it is essential that the superconductor-semiconductor interface is as clean as possible. Furthermore, the shape and dimensions of the superconducting electrodes need to be precisely controlled. We fabricated self-defined InAs/Al core-shell nanowire junctions by a fully *in-situ* approach, which meet all these criteria. Transmission electron microscopy measurements confirm the sharp and clean interface between the nanowire and the *in-situ* deposited Al electrodes that are formed by means of shadow evaporation. Furthermore, we report on tunnel spectroscopy, gate, and magnetic field-dependent transport measurements. The achievable short junction lengths, the observed hard gap, and the magnetic field robustness make this hybrid structure very attractive for applications that rely on a precise control of the number of subgap states, like Andreev qubits or topological systems.

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I. INTRODUCTION

Over the last decade, superconductor-semiconductor-nanowire hybrid structures have experienced growing interest as building blocks in circuits based on various novel physical phenomena. In superconducting transmon quantum bits Josephson junctions featuring a semiconductor-nanowire weak link between two superconducting electrodes allow for gate control instead of flux control as employed in conventional Josephson junctions [1–4]. This makes the circuit layout much more compact. In addition, one can also make use of the relatively large Fermi wavelength in the semiconductor being comparable with the nanowire dimensions. As a consequence, well-distinguished quantized levels are formed, which might be used to realize an Andreev quantum bit [5–8].

One of the most exciting properties of such nanowire-superconductor hybrid structures is the access to the mesoscopic regime, in which the behavior of the realized Josephson junction is fully determined by the coherent

bound states inside the semiconductor. Because of the presence of spin-orbit coupling in III-V semiconductor nanowires, it is also possible to observe exotic phenomena beyond the classical Andreev spectrum [6,7,9–11]. After the first observation of signatures of Majorana fermions in nanowire-superconductor hybrid structures [12–15], the interest extended towards realizing topological quantum bits [16,17]. One reason is that, owing to the nonlocal nature of Majorana states, topological quantum circuits are less prone to errors [18].

The performance of nanowire-based Josephson junctions depends to a large extent on the properties of the superconductor-semiconductor interface. In most cases, the superconductor is deposited *ex situ* after the growth of the nanowire. This makes it necessary to carry out some surface cleaning steps, e.g., wet chemical etching or Ar⁺ sputtering, before superconductor deposition [19]. However, this procedure often results in a nonideal interface. In order to circumvent this problem, efforts were undertaken to deposit the superconductor *in situ*, i.e., without breaking the vacuum after the growth of the nanowires [20–24]. Another crucial issue is the length of the weak

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link junction, since it determines the number of Andreev levels involved in the Josephson supercurrent. The conventional method to define a junction in an *in-situ* deposited superconducting shell wire has been to use electron beam lithography and wet chemical etching [1], which puts constraints on the minimum attainable junction length due to the isotropic nature of chemical etches. In order to tackle this issue, very recently, alternative fabrication schemes were developed where the junction length is geometrically defined by shadow evaporation [23,25,26].

We fabricate fully *in-situ* InAs nanowire-based Josephson junctions, utilizing shadow evaporation of Al to define the closely spaced superconducting electrodes. In this processing scheme the shadow mask is provided by a nanowire crossing an underlying nanowire in close proximity. The structural properties of the InAs/Al core-half-shell nanowires are investigated using transmission electron microscopy. In the transport experiments, we are able to tune the junction from the fully depleted regime, i.e., Coulomb blockade, to a well-developed Josephson supercurrent range by biasing a lithographically defined bottom gate finger. Furthermore, we present voltage-driven measurements, which are sensitive to the density of states in the nanowire and the structure of the superconducting gap. Finally, we present an analysis of the junction behavior for externally applied magnetic fields parallel to the nanowire axis and out of plane.

With the fabrication scheme established here, our junctions are very well suited for various applications. Since the junction length is determined by the nanowire diameter, very short junctions with a low density of states in the semiconductor can in principle be realized. This allows access to the regime where the supercurrent is carried by only one (or a few) Andreev bound states, which is an important prerequisite for Andreev qubits. Furthermore, the clean InAs/Al interface makes our structures very interesting for realizing Majorana states.

II. GROWTH AND DEVICE FABRICATION

The fully *in-situ* Josephson junctions are fabricated using the following procedure. In order to achieve adjacent Si(111) surfaces, anisotropic etching is employed with tetramethyl ammonium hydroxide on a prepatterned Si(100) substrate with arrays of $3\ \mu\text{m}$ squares. The resulted tilted planes have an angle of 54.7° with respect to the unetched Si(100) surface. These Si(111) facets form the basis for the subsequent InAs nanowire growth by means of catalyst-free molecular beam epitaxy (MBE).

Before the NW growth, a 23 nm thick SiO_2 layer is formed on the Si substrate by thermal oxidation. Then, 80 nm wide holes are defined in the oxide layer over adjacent Si(111) facets using electron beam (EB) lithography, reactive ion etching ($\text{CHF}_3 + \text{O}_2$), and wet chemical etching (HF). The holes are positioned so that the grown NWs

cross each other closely, but do not merge. The InAs NWs are grown in two steps. First, at a substrate temperature of $480\ ^\circ\text{C}$ with an In growth rate of $0.08\ \mu\text{m}/\text{h}$ (determined as the growth rate of In(100) planar layers) and an As_4 beam equivalent pressure (BEP) of approximately 4×10^{-5} mbar for 10 min to sustain an optimal growth window and then decreasing the substrate temperature to $460\ ^\circ\text{C}$ with an In growth rate of $0.03\ \mu\text{m}/\text{h}$ and an As_4 BEP of approximately 3×10^{-5} mbar for 3.5 h, resulting in $4\text{--}5\ \mu\text{m}$ long and 80 nm wide NWs. After the growth of the InAs nanowires, the substrate undergoes an arsenic desorption at $400\ ^\circ\text{C}$ for 20 min and at $450\ ^\circ\text{C}$ for 5 min. By doing so, we suppress the formation of parasitic heterostructures like AIAs during the deposition of the Al, which ensures a pristine interface without any barriers. Subsequently, the sample is transferred to the metal MBE and is cooled down to $-6\ ^\circ\text{C}$, followed by the evaporation of a 25 nm thick layer of Al onto the nanowires at this temperature [20,22]. During the metal evaporation process, an elevated angle of 87° is maintained between the metal flux and the nanowire axis, which ensures that the metal

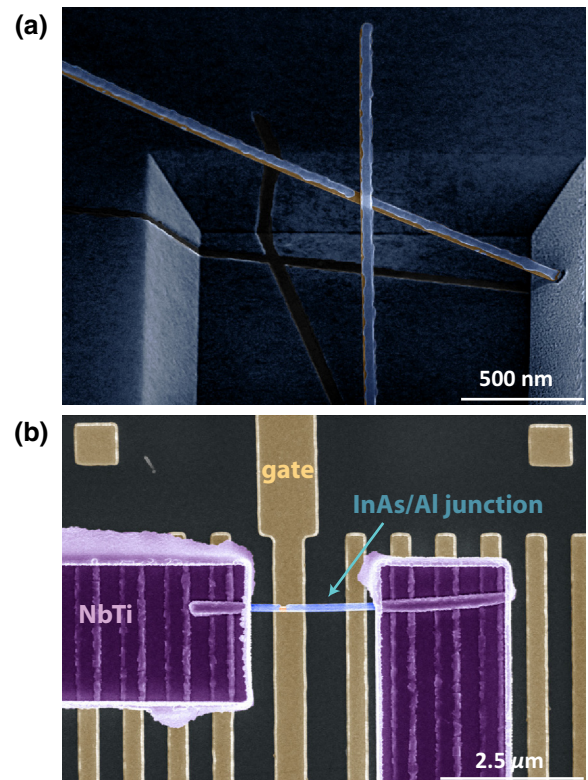


FIG. 1. (a) False-color scanning electron beam microscopy image of the as-grown InAs nanowires (orange) covered with an Al half-shell (blue). The *in-situ* junction is formed due to the shadow imposed by the upper nanowire. (b) A single InAs/Al nanowire junction contacted by NbTi electrodes. The junction is placed on a Ti/Au bottom gate electrode by means of a micromanipulator. A stack of $\text{Al}_2\text{O}_3/\text{HfO}_2$ is used as the gate dielectric.

deposition is smooth and highly crystalline. In Fig. 1(a), a scanning electron beam microscopy (SEM) image of an as-grown *in-situ* InAs/Al-nanowire Josephson junction with a junction length of approximately 80 nm is shown. It can be clearly seen that the junction length is directly related to the diameter of the upper nanowire, which acts as the shadow mask.

The devices are fabricated on commercially available highly resistive Si substrates ($\rho > 100$ k Ω cm). All etching and metal-deposition steps are realized using standard EB lithography techniques. The sample layout can be found in Appendix A. At first, a single Ti/Au (5 nm/10 nm) gate electrode surrounded by a set of electrically unconnected metal stripes for mechanical support are deposited, together with a small bonding pad and a single lead between the gate and the pad. This is followed by another Ti/Au deposition (60 nm/70 nm) to form a larger bonding pad on top of the smaller one as well as additional, positive EB markers. The whole substrate is subsequently covered by an 3 nm/12 nm thick Al₂O₃/HfO₂ dielectric layer by means of atomic layer deposition. As the circuits are intended to work for both ac and dc measurements, we use a transmission line to form the source contact of the device. The latter is terminated by an on-chip bias tee, consisting of an interdigital capacitor and a planar coil. All three elements, together with the surrounding ground plane, are fabricated out of reactively sputtered titanium nitride (80 nm thick, deposited at room temperature).

Subsequently, the nanowires are then transferred onto the electrostatic gates by means of a SEM-based micro-manipulator setup. To ensure an ohmic coupling between the contacts, made out of NbTi, and the Al shell, we used a combination of a 5 s long wet chemical etch in Transene-D, followed by an *in-situ* Ar⁺ dry etch. The contact separation is chosen to be at least 1.5 μ m in order to reduce the effect of the wide-gap superconductor NbTi on the actual junction characteristics. In Fig. 1(b) we show one of the final Josephson junctions on top of a bottom gate electrode (yellow).

III. RESULTS

A. Structural characterisation

The structural properties of the InAs/Al core-half-shell nanowires are examined using STEM. For this, the nanowires are transferred to holey carbon Cu grids by simply sweeping the arrays with the grid. The InAs nanowires grown by the current catalyst-free method showed polytypic crystal structure containing thin, defective wurtzite (WZ) and zinblende (ZB) segments.

In Fig. 2(a), we show a low-magnification image of a core-half-shell nanowire. The Al layer is uniform along the nanowires and has a smooth surface with no significant faceting [20]. Cross sections prepared by focused ion beam revealed that the Al thickness is not uniform

around the half-shell, as shown in Fig. 2(b). The balling up is related to the relative high deposition temperature (-6°C). A similar tendency, although less pronounced, is observed at -30°C (see the supplementary information of Ref. [20]), and only by decreasing the temperature even more, -120°C in Ref. [23], a conformal deposition can be obtained. The maximum thicknesses of the Al layers in these nanowires are between 30–50 nm. The Al half-shell is formed of large grains (greater than 25 nm) with different orientations. These differently oriented grains can be seen in the two viewing directions with grain boundaries marked by red arrows in Figs. 2(a) and 2(b). Some of the observed grain orientations include $([110]_{\text{Al}}\parallel[0001]_{\text{InAs}})_{\parallel} \times ([\bar{1}\bar{1}2]_{\text{Al}}\parallel[11\bar{2}0]_{\text{InAs}})_{\perp}$ and $([110]_{\text{Al}}\parallel[0001]_{\text{InAs}})_{\parallel} \times ([1\bar{1}0]_{\text{Al}}\parallel[11\bar{2}0]_{\text{InAs}})_{\perp}$ (using WZ notation for InAs). These orientations are different to those shown in some of the previous works [20,26,27], but consistent with some of those seen in our prior results [22]. It should also be noted that the size of the Al grains is much larger than the width of a single crystal-type region in the polytypic nanowire (which is generally less than ten monolayers), and these grains span multiple phase changes and defects. This means that a change in phase of the nanowire does not directly induce a change in the metal grain orientation.

The interface between the Al and InAs is analysed using the cross sections, as this viewing angle avoids simultaneous contribution to the projection from Al growth on multiple facets. In Fig. 2(c), we show a falsely colorized higher-magnification image of the InAs/Al interface from a nanowire cross section [different to Fig. 2(b)]. It can be seen that the interface is sharp and smooth with no amorphous material in-between crystalline InAs and Al, as a result of fully *in-situ* deposition of the electrodes and absence of processing steps such as Ar⁺ sputtering. Edge dislocations that have previously been attributed to AIAs formation [20,22] are observed in the side view of these nanowires. Dislocations are placed approximately 2.5 nm from the interface within InAs. Evidence supporting an AIAs layer as thick as 2.5 nm is not seen in energy dispersive x-ray (EDX) data or lattice spacings of high-resolution images, although a smaller lattice spacing ($d_{(11-20)}$) is observed between the edge-most lattice planes in some nanowire facets, accounting for a possible AIAs or (Al, In)As formation of thickness less than 0.5 nm. This shows that almost all of the As on the entire nanowire surface has been desorbed prior to Al deposition, which is consistent with transport measurements (shown later) that show no evidence for the presence of a significant intermediate AIAs layer. In Fig. 2(d) we show an annular dark-field image and the corresponding EDX map of an InAs/Al junction. A clear sharp gap in the Al layer is formed in the shadowed region with a junction width of 75 nm. A few small, oxidized, and isolated droplets of Al that appear to have formed during its deposition are seen within

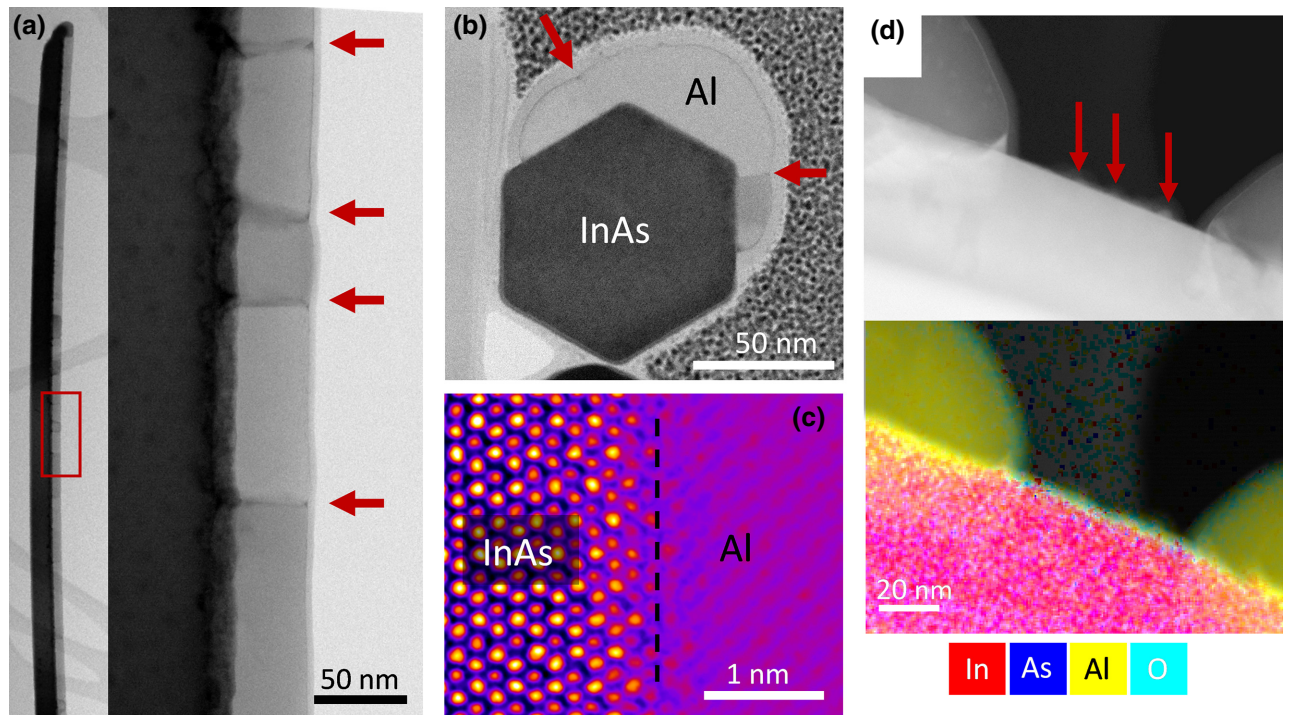


FIG. 2. (a) A low-magnification bright-field (BF) scanning transmission electron microscope (STEM) image from the region indicated in the core-half-shell nanowire shown in the inset. Zone axis for imaging is WZ $\langle 11\bar{2}0 \rangle$ (ZB $\langle 110 \rangle$ equivalent) of InAs and the red arrows mark the grain boundaries. (b) A BF STEM image of a nanowire cross section along the WZ InAs $\langle 0001 \rangle$ (or ZB $\langle 111 \rangle$) direction showing the Al half-shell and red arrows indicating the grain boundaries. (c) A false-color high-magnification cross-sectional image of the InAs/Al interface. The broken line marks the interface from a different nanowire to (b). (d) An annular dark-field (ADF) STEM image and the corresponding EDX map of an InAs/Al junction showing the elemental distribution. The red arrows in the ADF image indicate the isolated oxidized Al droplets within the gap. The zone axis for (d) is WZ InAs $\langle 1\bar{1}00 \rangle$ (ZB $\langle 112 \rangle$).

the junction (indicated by red arrows in the ADF image). However, these seem to get etched off during the subsequent device processing steps as no evidence of parallel metallic bypass is observed in the transport measurements.

B. Basic junction characteristics

All presented measurements are performed in a ^3He - ^4He dilution refrigerator at a base temperature of 15 mK equipped with a superconducting magnet coil. I - V traces are measured using a current bias supplied from a battery-powered current source and measured using a battery-powered differential voltage amplifier. The measurement lines within the refrigerator are heavily filtered with thermocoax, low-temperature copper powder filters, and custom low-pass filters in addition to room temperature “pi” filters.

The efficiency of the gate response is one of the key properties of a nanowire junction. Therefore, we measure the conductance of the junction in a voltage-biased configuration. In Fig. 3(a) a gate sweep for one of the *in-situ* devices is shown. For these measurements, a constant source-drain voltage V_{SD} of 400 μeV is maintained across the junction, i.e., above the induced proximity gap.

Depending on the applied gate voltage V_g , four different regimes can be distinguished. For gate voltages below -6.7 V, the nanowire is completely pinched off. Above this value, the current is mediated by single electron transport through an intrinsic quantum dot. For gate voltages larger than -5 V, the nanowire opens up, but the conductance is still limited by a low-transparency tunnel coupling to the electron reservoirs in the contacts. This results in a conductance increase of just $2e^2/h$ over a gate voltage range of 2 V and just a weakly pronounced superconducting branch. For the last regime, i.e., voltages above -3 V, the current-voltage characteristics show a classical Josephson junction response [cf. the inset of Fig. 3(a)] with a clear supercurrent. In addition, signatures of subharmonic gap structures are found in the differential resistance [28,29].

In Fig. 3(b), we show a set of I - V curves at three different gate voltages within the Josephson-junction regime. It can be seen that the switching current of the device can be tuned between 3 and 10 nA. The additional constant-voltage sections are related to self-induced Shapiro steps, caused by the transmission-line circuit on the sample. At $V_g = -0.5$ V we obtain a critical current of $I_c = 11$ nA and a normal-state resistance of $R_N = 6.33$ k Ω , which results in an $I_c R_N$ product of 70 μV . We stress

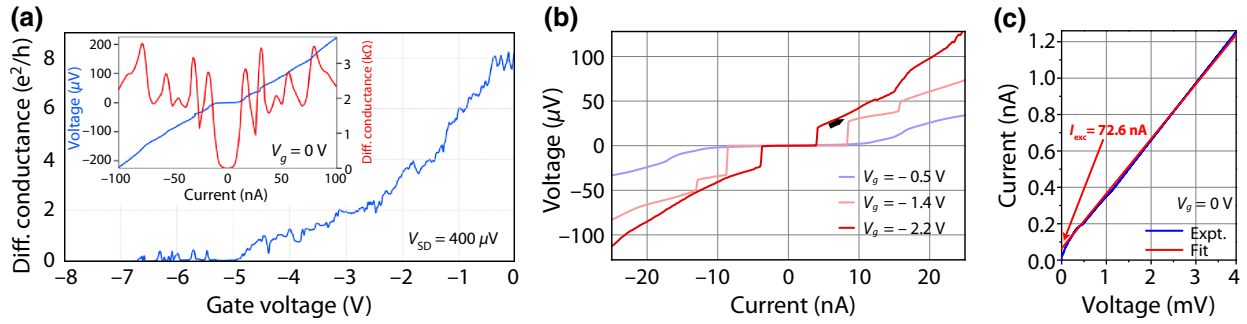


FIG. 3. Conductance G versus gate voltage measured in a voltage-driven setup with a constant source-drain voltage V_{SD} of 400 μeV . Four different transport regimes can be distinguished (negative to positive gate voltage): pinch off, Coulomb blockade, tunnel-dominated transport, and classical Josephson junction behavior. The inset shows the current-voltage (I - V) characteristics at zero gate voltage, with a supercurrent of approximately 21 nA and signatures of subharmonic gap structures in the differential resistance. (b) I - V curves at gate voltages of -0.5 , -1.4 , and -2.2 V, respectively. The black arrow indicates the sweep direction. The small asymmetry can be attributed to thermal effects, e.g., overheating, or an underdamped junction behavior. (c) Current-voltage characteristics at $V_g = 0$ V up to large bias voltages. By fitting and extending the linear and ohmic behaviors of the normal state, an excess current I_{exc} of 72.6 nA is extracted.

that the presented $I_c R_N$ value just holds for the given gate voltage. For the other two I - V curves, we obtain $I_c R_N(-1.4\text{V}) = 72 \mu\text{V}$ and $I_c R_N(-2.2\text{V}) = 75 \mu\text{V}$ with $R_N = 8.7 \text{ k}\Omega$ and $11.8 \text{ k}\Omega$, respectively. Although the normal-state resistances are quite different for the three gate voltages, the $I_c R_N$ product varies only slightly. Similar behavior has been observed in nanowire-based Josephson junctions [30,31]. Here, it was found that the critical current changes essentially in the same way as the normal-state conductance. Owing to the mesoscopic nature of nanowire bridging, the superconducting electrodes R_N are affected by interference effects such as universal conductance fluctuations. As indicated in Fig. 5(c), by extrapolating the current-voltage characteristics at the normal state in the range $V > 400 \mu\text{V}$, a finite excess current I_{exc} of 72.6 nA is extracted. The excess current can be used to obtain an estimation of the dominating type of transport within the channel by comparing the $I_{exc} R_N$ product with the superconducting gap Δ . Following the framework of the corrected Octavio-Tinkham-Blonder-Klapwijk theory [28,29], we obtain a ratio of $eI_{exc} R_N / \Delta = 1.31$ at zero gate voltage. This value can be converted to the barrier strength parameter $Z = 0.38$ and a corresponding contact transparency $\mathcal{T} = 0.88$ [29,32]. This transparency is comparable to values obtained for hydrogen cleaned superconductor-nanowire junctions, i.e., Al/InSb [23] or Nb-Ti-N/InSb [15].

C. Hard-gap spectroscopy and Yu-Shiba-Rusinov states

The second benchmark of a superconductor-semiconductor hybrid structure is the hardness of the induced proximity gap, i.e., the coupling strength between the nanowire and the metal shell, in the single-channel or tunneling limit. Previous experiments on similar systems used tunnel

spectroscopy between one superconducting and one normal conducting contact to detect the strong change in the density of states of the device close to the gap edge [21]. Even though our structure is slightly different in terms of the contact setup, we can obtain comparable conditions by applying a negative gate voltage that sets the device into the tunnel-limited regime [19]. In Fig. 4, we show a typical spectroscopylike measurement of a self-defined InAs/Al nanowire Josephson junction. As indicated in the figure, four pronounced peaks are identified. Feature (1) is thereby related to the superconducting state, while (2) and (3) correspond to subgap structures. Finally, the dominating peak (4) marks the edge of the induced proximity gap $2\Delta = 380 \mu\text{eV}$. Similar to the tunneling experiments of Chang *et al.* [21] the density of states in the nanowire segments underneath the superconducting electrodes is probed

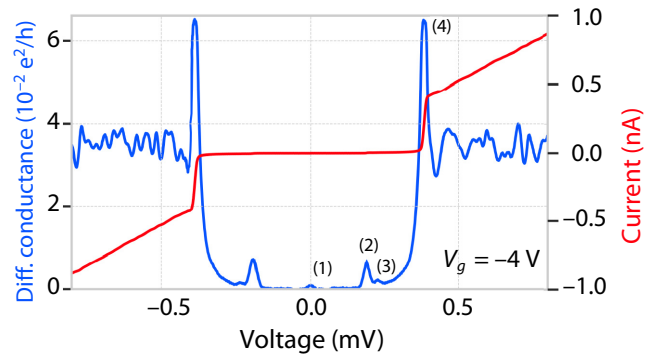


FIG. 4. Voltage-driven tunnel spectroscopy measurement of an InAs/Al nanowire junction at $V_g = -4$ V: current as a function of voltage (red) and the corresponding differential conductance in units of e^2/h (blue). The four peaks correspond to (1) the superconducting state, (2),(3) subgap structures, and (4) the induced proximity gap.

by our measurements. Because of the proximity effect an induced gap is created in the InAs nanowire. However, in our structure two proximitized nanowire segments are separated by tunnel barriers forming the quantum dot; therefore, 2Δ is measured. The value of Δ is close to the bulk Al gap ($\Delta_{\text{Al}} = 200 \mu\text{eV}$), indicating a good coupling between Al and InAs. An important figure of merit is the ratio of the conductance for in- and out-of-gap transport, i.e., G/G_N . Between (4) and (2), the conductance drops to $G/G_N \approx 0.02$, with a further reduction between (2) and (1) to $G/G_N < 0.001$. Such a strong decrease of the conductance is an indication that our devices host a so-called hard gap [19,21,26].

As already shown in Fig. 3, the actual junction behavior is strongly correlated with the applied gate voltage. Thus, we perform a gate batch measurement between -8 and 0 V in steps of 29 mV, which covers both the tunnel-limited regime as well as the range in which the transport is dominated by multiple Andreev reflections. In Fig. 5(a), we show the stability diagram of the junction for gate voltages between -8 and -4 V. Here, the transport is dominated by single electron tunneling, which results in pronounced Coulomb diamonds. By mapping out the size of the diamonds in terms of their individual gate and bias voltage, we obtain a lever arm $\alpha = 0.095$ and charging energy $E_c = 11.6$ meV for the large diamond in Fig. 5(a) and

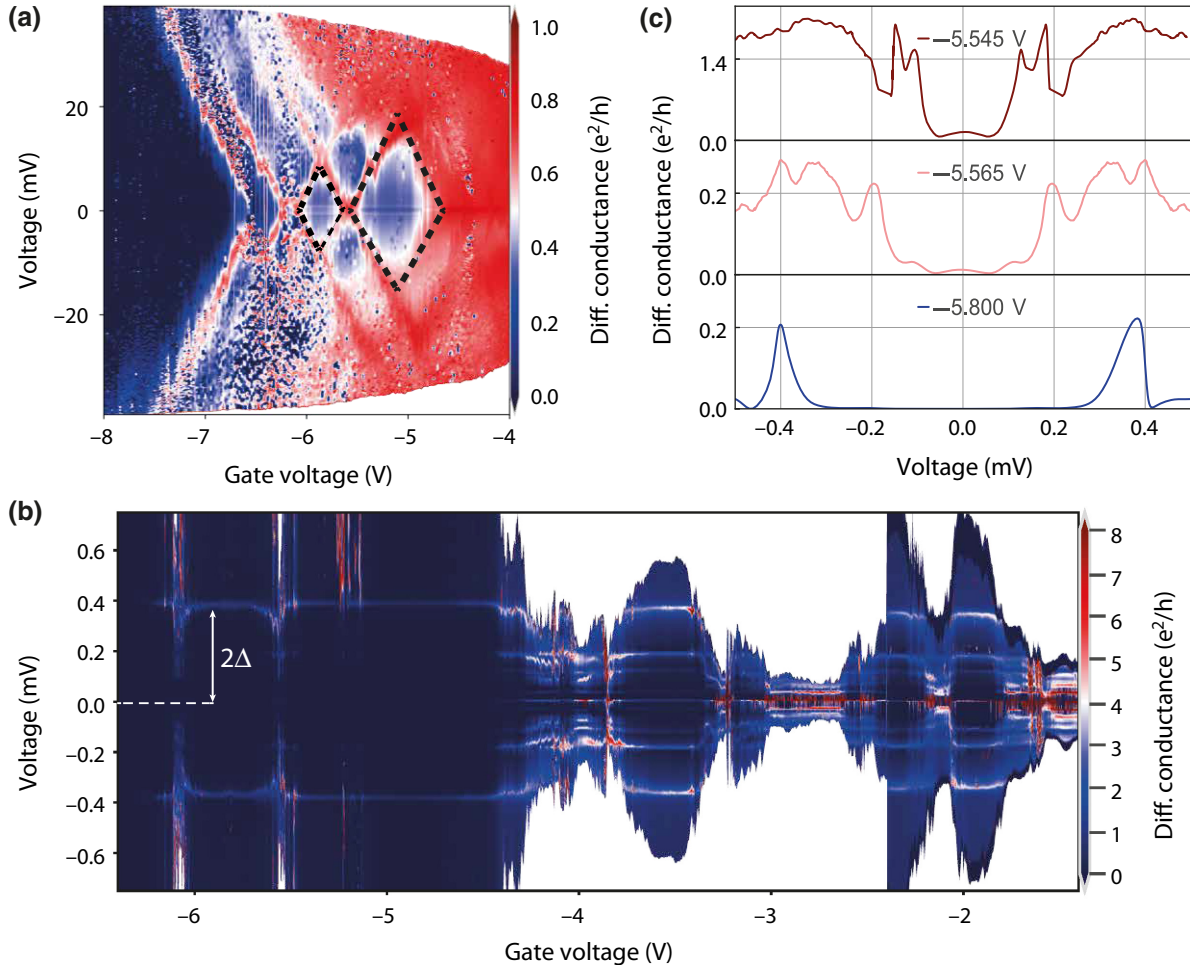


FIG. 5. (a) Full gate response for gate voltages between -8 and -4 V, showing a set of Coulomb diamonds (indicated by the black dashed lines) that are related to a single quantum dot, with charging energies of $E_c = 11.6$ meV $\approx 60\Delta$ and $E_c = 8.5$ meV $\approx 44\Delta$, respectively. (b) Differential conductance versus bias voltage measurements with a high-resolution gate voltage stepping for $V_g = -6.4, \dots, -1.4$ V. The measurement covers the in- and interdiamond sections as well as the open-junction regime. Within the Coulomb diamonds found in the range of $V_g < 5.5$ V, the only visible feature is related to the edge of the proximity gap. However, for voltage values close to the section in which the quantum dot is open, Yu-Shiba-Rusinov states are observable. (c) Differential conductance versus bias voltage traces at different gate voltages, depicting the evolution of the subgap structure in and out of the Coulomb diamonds. For -5.8 V (dark blue), there are only two peaks that are related to the edge of the proximity gap. At -5.655 V (light red), multiple subgap states become visible. For -5.545 V (dark red), the spectrum completely changes, ending up in a trace with a 7 times larger conductance and a pronounced peak at zero energy. We attribute this behavior to a mixture of both multiple Andreev reflections and Yu-Shiba-Rusinov states.

$\alpha = 0.021$ and $E_c = 8.5$ meV for the small diamond. The large values of E_c indicate that the corresponding quantum dot has to be rather small and is most likely caused by twinning defects or lattice-type changes in the nanowire junction area. Based on these values, especially due to $\Delta < E_c$ [33], we assume that the transport, in the sections in which the quantum dot is open, is mediated by Yu-Shiba-Rusinov states rather than by conventional Andreev bound states [34–36].

In order to probe the actual state structure, we perform differential conductance versus bias voltage measurements at a high-resolution gate voltage stepping in the range of -6.4 to -1.4 V, which is shown in Fig. 5(b) [37]. We can distinguish between three different regimes. For less negative gate voltages, i.e., values above -4.3 V, (multiple) subgap states arise. However, for more negative gate voltages and, especially inside of the Coulomb diamonds, the subgap transport is completely suppressed. Nevertheless, the edges of the induced proximity gap are still present, represented by two straight light-blue lines at a constant voltage of ± 375 μ V. On the other hand, for certain gate voltage ranges, in which the quantum dot is open, several subgap features arise. In Fig. 5(c) three exemplary curves in the range around -5.7 V are shown. For a gate voltage of -5.8 V, the junction characteristics exhibit a clear hard gap without any subgap features. If the voltage increases, i.e., up to -5.565 V, a single state moves into the gap and additional peaks appear, which are probably related to coherent reflection events of the same state. For a gate voltage of -5.545 V, the state reaches zero energy, which, together with the onset of single electron tunneling, results in a 4 times increase of the in- and out-of-gap conductances as well as the emergence of a pronounced zero bias peak, probably caused by the interplay of multiple Andreev reflections and a single Yu-Shiba-Rusinov state. Based on the strong gate asymmetry, as well as due to the relatively large charging energy of $E_c \approx 60\Delta$, this behavior could be an indication for a quantum phase transition from a singlet into a doublet state, which effectively changes the nature of the junction from “0” to “ π ” [11,38–40]. However, due to the fact that the junction does not carry a real, nondissipative current in this specific gate voltage range and is not embedded in a phase-sensitive device like a superconducting quantum interference device, there is no direct way to probe the resulting reversal of the supercurrent. Nevertheless, these states could still offer some advantages for devices based on mesoscopic Josephson junctions by adding an additional energy tunability of the states besides the superconductor-semiconductor interface transparency.

D. In-plane and out-of-plane magnetic field transport measurements

The common requirement for all devices based on Andreev bound states is the manipulation of the phase

across the junction in order to move along the dispersion relation and set the system to a fixed operational point. This is normally achieved by means of a superconducting loop connecting the junction and applying a small external out-of-plane magnetic field that generates a flux-induced phase shift. In the case of semiconductor nanowires, and more specifically for materials like InAs or InSb, the strong spin-orbit coupling as well as the large g factor can be used as an additional way to manipulate the state structure both in energy and momentum space. Here, an additional in-plane field is required to induce a Zeeman splitting, with field values that can easily overcome the bulk critical field of Al by one or two orders of magnitude. Both things together make the magnetic field sustainability the second key benchmark of a nanowire Josephson junction.

In order to probe the magnetic field stability of the *in-situ* junctions, we perform voltage-driven measurements at a gate voltage of -4.3 V, i.e., close to, but outside of the regime that is dominated by the quantum dot. In Figs. 6(a) and 6(b), we show the conductance versus bias voltage for an out-of-plane field as well as for a magnetic field that is applied parallel to the nanowire axis, respectively.

As can be seen, both measurements show the typical damping and smearing out effect of the gap edge peaks, which is related to the continuous closing of the induced proximity gap if the magnetic field is increased. The field-induced changes in the normal-state conductance are most likely related to quantum fluctuations in the nanowire, i.e., the previously mentioned universal conductance fluctuations, induced by the superposition of multiple, flux-penetrated scattering loops. However, these should just affect the background conductance rather than the transport below the superconducting gap. By using the first derivative of the differential conductance, it is possible to extract the actual gap width for each trace. Even though this method underestimates the gap width for small magnetic fields, it makes it possible to find reliable values when the actual gap edge peaks are already completely suppressed. In Fig. 6(c), we summarize the field-dependent gap width in terms of energy for both the in-plane (blue) as well as the out-of-plane (red) fields. For the latter, we obtain a critical field of $B_c = 130$ mT, while the former is almost 2 times larger, with $B_c = 250$ mT. These comparably small values of B_c with respect to other works can be attributed to the much thicker Al shell of 25 nm in our case [20,41]. Additionally, both traces shown in Fig. 6(c) deviate from the conventional Bardeen-Cooper-Schrieffer (BCS) behavior, resulting in a much weaker field dependency of Δ . However, we stress that the closing of the gap is not necessarily coupled to a softening of the gap, as can be seen in Fig. 6(d) (for a logarithmic depiction of the conductance, see Appendix B). Here, we analyse the change of the ratio between the averaged field-dependent zero bias conductance $G_S(B_0)$ and the conductance above B_c , $G_N(B_0)$, as a function of fractions of the critical field.

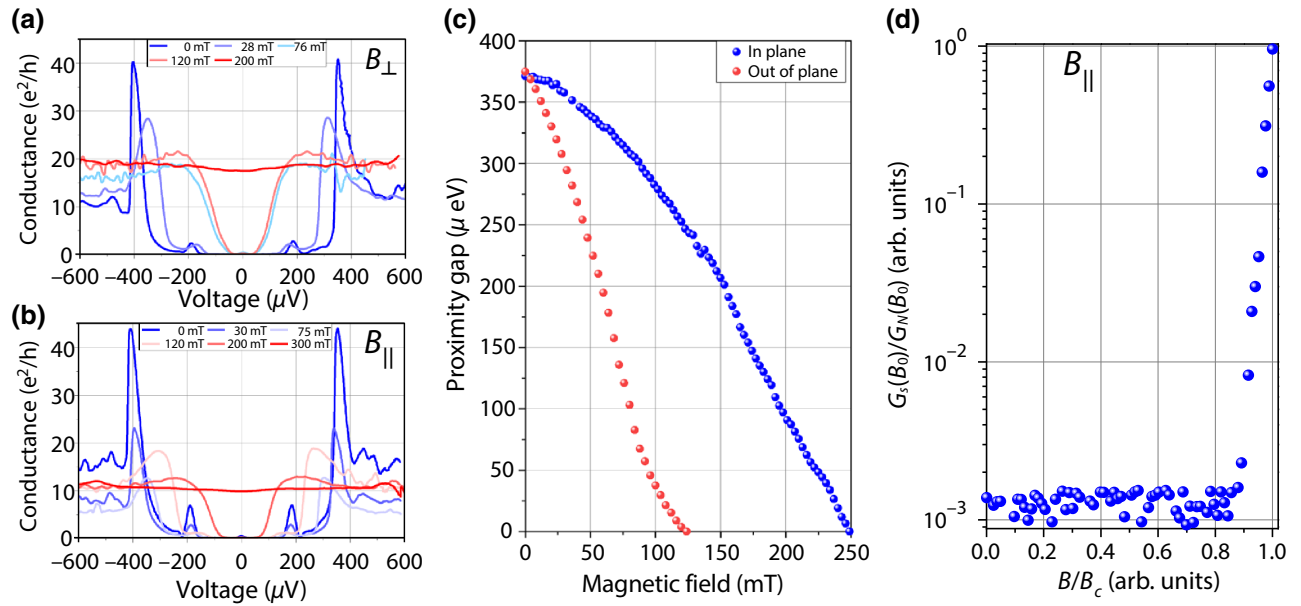


FIG. 6. Differential conductance traces as a function of bias voltage for various magnetic fields both perpendicular (a) and parallel (b) to the nanowire axis. For larger field values, the peaks corresponding to the edge of the proximity gap are damped and move closer to zero energy. (c) Width of the proximity gap 2Δ for an increasing magnetic field between 0 and 250 mT. The energies are extracted using the first derivative of the differential conductance. For an out-of-plane orientation, we find a critical field of $B_c = 130$ mT, while for the in-plane field, we obtain $B_c = 250$ mT. (d) Ratio of the averaged in-plane-field-dependent zero bias conductance relative to the conductance above the critical field. As long as the field is less than 90% of the critical field, the zero bias conductance is mainly determined by the noise floor of the system, without any parasitic subgap states, which is further proof for the hard-gap behavior of the junction.

As long as the applied in-plane field is smaller than $0.9B_c$, $G_S(B_0)$ is mainly limited by the noise floor of the system. However, above this value, the conductance increases continuously, until it reaches $G_N(B_0)$. We interpret this as another proof for the hardness of the induced proximity gap in our system, which is not disturbed by parasitic subgap states even for comparably large magnetic fields.

Finally, we present differential conductance measurement where the gate bias is set to zero, i.e., the nanowire bridge is conductive and no tunnel barrier is present. In Fig. 7(a) the differential resistance versus bias voltage is measured as a function of a parallel magnetic field. The conductance modulations for bias voltages in the range of $\pm 300 \mu\text{V}$ can be attributed to subharmonic gap structures due to multiple Andreev reflections [28,29,32]. The differential conductance trace at zero magnetic field is shown in Fig. 7(b). We assign the feature found at about $280 \mu\text{V}$ to $2\Delta/e$. The value for Δ extracted here is smaller than the bulk gap of Al. We attribute the lower value to the fact that instead of the bulk gap of Al the induced proximity gap in InAs is relevant. In contrast to the previously discussed measurements in the tunneling regime, here the induced gap is probably weakened toward the center of the junction, since no tunnel barrier is blocking the diffusion of carriers. In addition to the structure at $2\Delta/e$, higher-order subharmonic gap structures are also identified, i.e., at

$2\Delta/ne$ with $n = 2, 3$, and 4. We attribute the sharp feature at around $500 \mu\text{V}$ to some parasitic junction in series, presumably at the boundary between the NbTi contact fingers and the Al shell. Upon increasing the magnetic field, the positions of the subharmonic gap structures move towards zero bias, reflecting the decrease of the superconducting gap with increasing field. At the critical field of 250 mT, the subharmonic gap structures vanish. The critical field found here is in accordance with the value determined from the measurements in the tunneling regime.

In order to find out how the magnetic field orientation affects the junction characteristics, the differential conductance as a function of bias voltage is recorded for a full rotation of the magnetic field within the plane defined by the nanowire axis and the normal to the substrate [cf. Fig. 7(c)]. Here, the magnitude of the magnetic field is fixed at 100 mT. The trace of the differential conductance at 0° , parallel to the nanowire, is indicated by the orange line in Fig. 7(a). When rotating the magnetic field out of plane and perpendicular to the wire, the sequence of subharmonic gap features shift towards zero bias. This can be attributed to the fact that the gap of the Al film is more strongly suppressed for a perpendicular magnetic field than for a field aligned along the thin superconducting layer. The positions of these features scale with the superconducting gap.

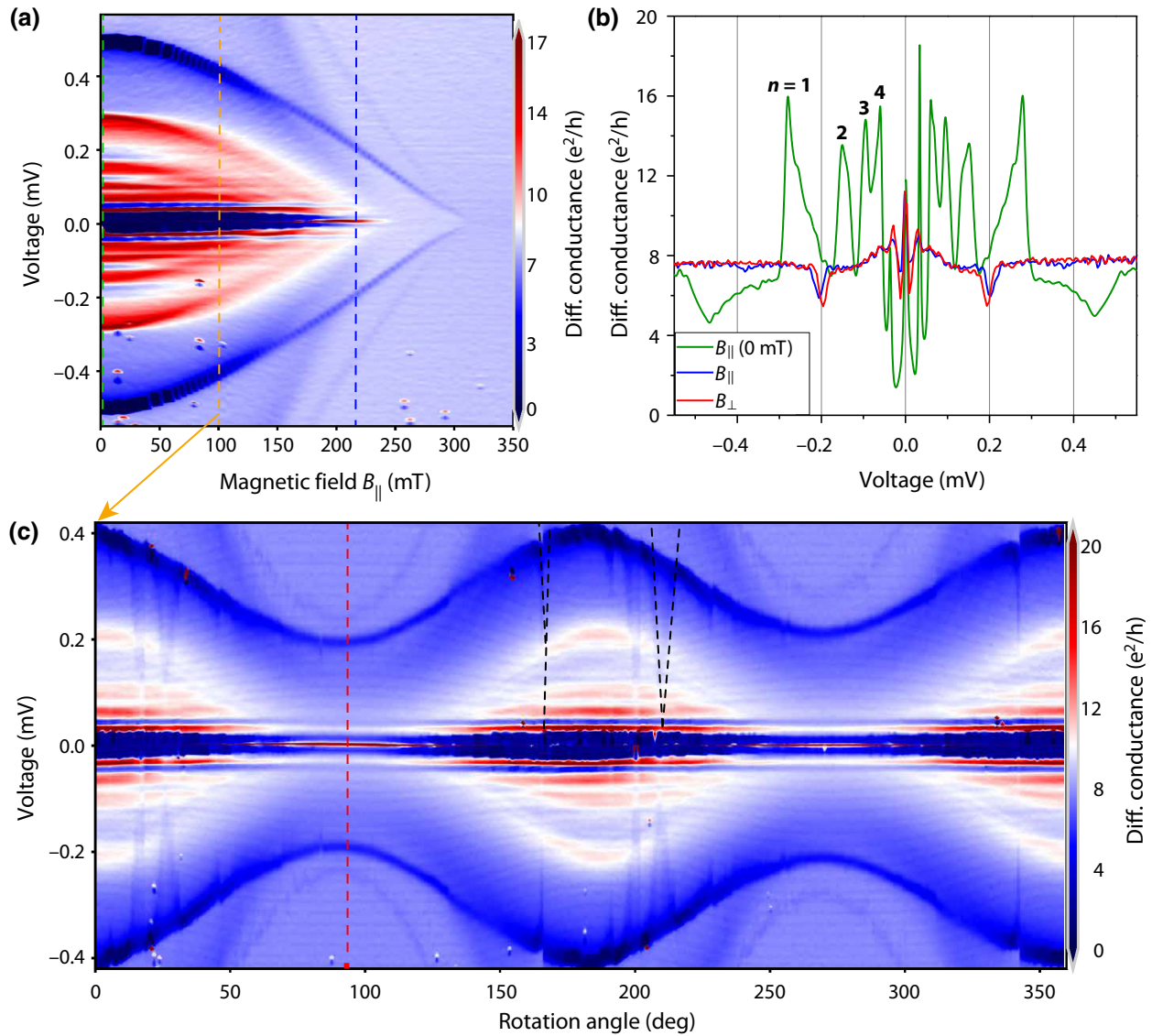


FIG. 7. (a) Differential conductance as a function of bias voltage and magnetic field at zero gate voltage. The field is oriented in plane and parallel to the nanowire axis. The data along the orange dashed line correspond to the data at 0° in (c). (b) Traces of the differential conductance versus bias voltage. The green curve shows the differential conductance at zero field. The red curve corresponds to the data along the red line in (c) for $B_{\perp} = 100$ mT, while the blue trace corresponds to the differential conductance along the blue dashed line in (a) at $B_{||} = 215$ mT. The curves are chosen so that the gap energies match. (c) Differential conductance as a function of bias voltage and of the magnetic field orientation. The magnitude of the magnetic field is kept fixed to 100 mT and the gate voltage is set to zero. Zero angle corresponds to a magnetic field orientation along the nanowire axis. At 90° the field is perpendicular to the substrate. The dashed black lines border some irregular features observed in the differential conductance.

To find out whether the magnetic field orientation changes the pattern of the differential conductance tracks, we compare the characteristics at a perpendicular field (90°) with the curve at a parallel field (0°) at correspondingly higher field strengths [cf. dashed blue line in Fig. 7(a)] to provide the same superconducting gap energy. As can be seen in Fig. 7(c), both curves match very well, no significant difference is observed.

Although the general conductance pattern varies smoothly with the magnetic field direction, some distinct

features are found, as indicated by the dashed black lines in Fig. 7(c). These features are reproducible since they appear again after a field rotation by 180° . So far, we have not yet been able to assign the exact cause of these structures. However, we speculate that they are related to magnetic-field-dependent states moving in and out of the superconducting gap, e.g., controlled by an angle-dependent g factor [42] or are induced by the orientation-dependent vortex dynamics within the NbTi or Al layer.

IV. CONCLUSION

We demonstrate that mesoscopic Josephson junctions based on nanowires with shadow-mask-defined weak links show state-of-the-art properties in terms of gap hardness, gate tunability of the switching current, interface transparency, and magnetic field resilience. In fact, in contrast to conventional nanowire junctions with epitaxial Al full or half-shells, they provide much more flexibility for the usable superconductors due to the avoidance of a wet or dry chemical etching step. Additionally, caused by the coupling between the actual junction length and the nanowire diameter, they ease the fabrication of short junctions, i.e., systems with just a single Andreev bound state. Thus, these junctions can potentially act as a building block for quantum devices based on excitations, like the Andreev qubit or topological systems with Majorana zero modes, which require a precise control of the internal state structure of the junction. Last but not least, our fabrication scheme can also be employed for more complex junction structures, e.g., for a sequence of Josephson junctions by using multiple wires as shadow masks or for the formation of Josephson junction networks by means of merged nanowires (some examples are given in Appendix C).

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APPENDIX A: CIRCUIT LAYOUT

A schematic illustration of the device layout of the circuit for dc and rf measurements is depicted in Fig. 8. The circuit is fabricated on a high-resistive Si substrate. For

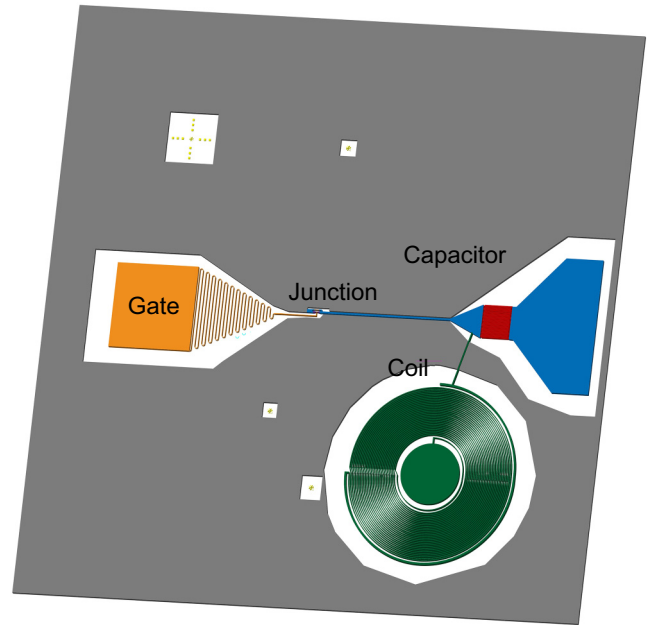


FIG. 8. Schematic overview of the device layout. The bottom gate (orange) is fabricated out of Ti/Au and ends in a single electrode below the junction. The interdigital capacitor (red) and the planar coil (green) act as a bias tee. Using this, it is possible to supply the nanowire Josephson junction with a superposition of an ac and dc signal by means of the common transmission line (blue).

the bias tee, an interdigital capacitor and a planar coil superconducting TiN is used, while for the bottom gate structure a Ti/Au layer is employed. The signal from the bias tee is transferred via a transmission line to the junction.

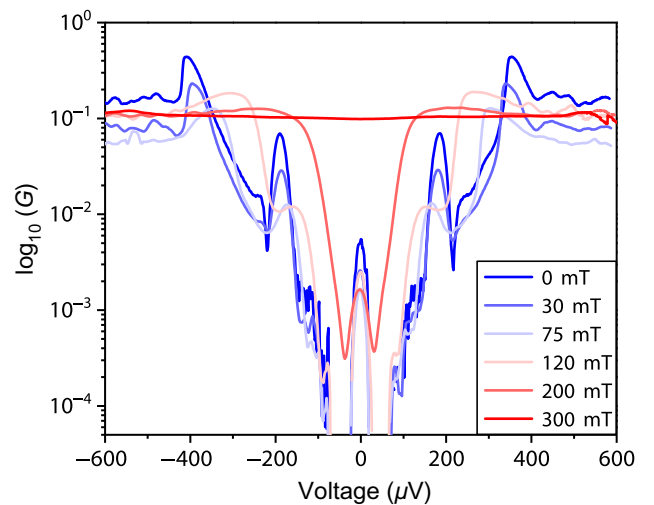


FIG. 9. Voltage-dependent and logarithmic differential conductance traces for increasing magnetic fields. The field is applied parallel to the nanowire axis.

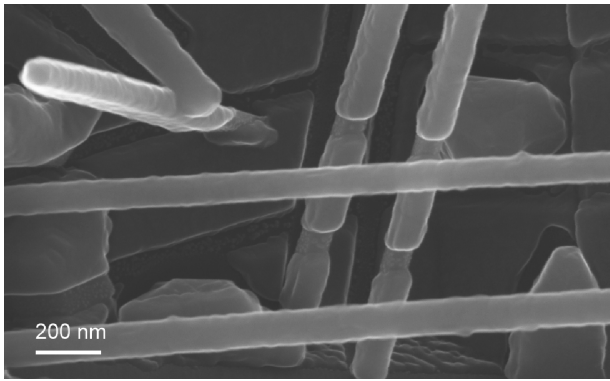


FIG. 10. Scanning electron micrograph showing an example of multiple junctions in series obtained by employing more than one nanowire for shadow evaporation.

APPENDIX B: DETERMINATION OF THE GAP HARDNESS

In order to further illustrate the gap hardness at various magnetic fields applied along the nanowire axis, the logarithm of differential conductance is plotted as a function of bias voltage in Fig. 9.

APPENDIX C: GROWTH OF MULTIPLE JUNCTIONS IN SERIES AND NANOWIRE NETWORKS

Our fabrication scheme can also be extended to more complex structures. By using the shadow of more than one nanowire crossing, underlying nanowire multiple Josephson junctions in series can be created. In Fig. 10 an exemplary scanning electron microscopy image is shown. Although in the present case parasitic growth is responsible for the presence of multiple nanowires, it is in principle possible to determine the position of the shadowing nanowires precisely by selective area growth. In that case the position of the holes on the Si(111) side facets determine the location of the junctions in the underlying wire.

In addition, it is also possible that nanowires that have been grown from two adjacent Si(111) side facets merge,

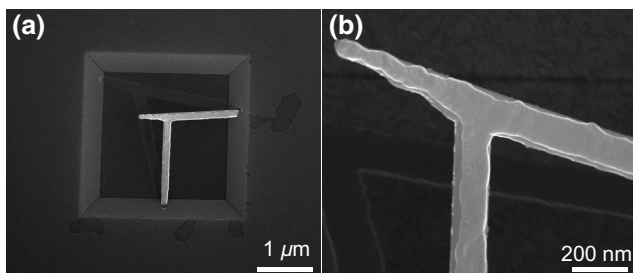


FIG. 11. (a),(b) Scanning electron micrographs showing examples for two merged nanowires.

as shown in Fig. 11. One finds that the nanowires maintain their original diameter at the crossing point rather than forming a “blob.” By this means, nanowire networks can be created with well-defined and constant dimensions. Ultimately, the formation of multiple junctions can be combined with the growth of networks, which would be very interesting for the realization for circuits for topological quantum computation based on Majorana modes.

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