Ultrascaled Double-Gate Monolayer SnS_2 MOSFETs for High-Performance and Low-Power Applications

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The shrinking of field-effect transistors (FETs) is in great demand for next-generation integrated circuits. However, traditional silicon FETs are reaching the scaling limits, and it is therefore urgent to explore alternative paradigms. Two-dimensional (2D) materials attract great research enthusiasm, owing to their abilities to suppress short-channel effects. Herein, we evaluate the electronic properties and device performance of ultrascaled 2D SnS_2 metal-oxide-semiconductor FETs (MOSFETs) via *ab initio* simulations. Specifically, the I_{on} value of the 5.5 nm monolayer SnS_2 *n*-MOSFETs is ultrahigh, up to 3400 μA/μm, as a result of the small effective masses of the conduction-band minimum of monolayer SnS_2. Until the channel length is scaled down to 4 nm, the MOSFETs can fulfill the standards of I_{on}, delay time, and power dissipation product of the International Roadmap for Devices and Systems (IRDS) 2018 goals for high-performance devices. Moreover, the 5.5 nm monolayer SnS_2 *n*-MOSFETs can also fulfill the IRDS 2018 requirements for the 2028 horizon for low-power applications. This work demonstrates that monolayer SnS_2 is a favorable channel material for future competitive ultrascaled devices.

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I. INTRODUCTION

The downscaling of field-effect transistors (FETs) to the sub-7 nm channel length is in great demand for integrated circuits in the next decade [1,2]. However, traditional silicon FETs have approached their physical limits and are suffering from the challenges of the short-channel effect, increased drain-leakage current, and unnecessary power consumption. To solve these problems, it is extremely urgent to find alternative materials to replace silicon as next-generation channel candidates. Two-dimensional (2D) semiconductors have drawn intensive research attention because of their atomic and uniform thicknesses, outstanding gate electrostatic controlling ability, and free-dangling-bond structures [3–8]. Numerous efforts have been devoted to studying FETs based on several 2D materials, such as silicene, 2D MoS_2, black phosphorene, 2D InSe, and 2D Bi_2O_2Se [9–24].

Recently, atomic-layer 2D SnS_2 has been successfully synthesized by mechanical exfoliation and chemical vapor deposition [25–29]. The controllable growth of large-sized and good-uniformity 2D SnS_2 has been realized. Furthermore, high-quality 2D SnS_2-based FETs have been experimentally fabricated [29]. Importantly, FETs based on SnS_2 with a lateral size of 410 μm have exhibited an ultrahigh on:off current ratio of about 10^8, which is higher than that of black phosphorene [11], 2D Bi_2O_2Se [17], tellurene [18], and other 2D material FETs. However, when the channel length of FETs is reduced to sub-10 nm, and even shorter, can 2D SnS_2 FETs continue to maintain the prominent device performance and simultaneously meet the requirements of the International Roadmap for Devices and Systems (IRDS) [30]?

Here, we theoretically evaluate the potential performance of double-gated (DG) monolayer SnS_2 metal-oxide-semiconductor FETs (MOSFETs) in future ultrascaled technology. We first adopt the density-functional theory (DFT) method to investigate the intrinsic electronic properties of monolayer SnS_2. Then, based on *ab initio* quantum transport simulations, the transfer characteristics in two directions of the monolayer SnS_2 MOSFETs are investigated, focusing on the main critical device properties, including *on*-state current (I_{on}), on:off ratio, delay time,

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and power-delay product (PDP). In particular, the monolayer SnS_2 *n*-MOSFET presents an ultrahigh I_{on} (up to 3400 μA/μm in 5.5 nm channel length), which greatly surpasses reported FETs based on other 2D materials [31–34]. The SnS_2 *n*-MOSFETs outperform the standard of I_{on}, delay time, and PDP given by the IRDS 2018 requirements for high-performance (HP) devices, even when the channel length is reduced to 4 nm. Moreover, the 5 nm monolayer SnS_2 *n*-MOSFETs can also fulfill the requirements of the IRDS for low-power (LP) applications. The outstanding device performance of the monolayer SnS_2 MOSFETs endows it with great potential for future competitive HP and LP digital applications.

II. SIMULATION METHOD

Geometrical optimization and electronic states of monolayer SnS_2 are calculated by using DFT method as implemented in the Vienna *ab initio* simulation package (VASP) code. Ion-electron interactions are expressed by projector augmented wave pseudopotential [35]. The exchange-correlation function is described based on the generalized gradient approximation (GGA) in the form of Perdew-Burke-Ernzerhof (PBE) parameterization [36–38]. The cutoff energy of the wave function is set to 500 eV. The structures are relaxed until the energy tolerance is less than 1×10^{-5} eV and the force tolerance is less than 0.01 eV/Å^{-1}. The Brillouin zone is sampled by $15 \times 15 \times 1$ Monkhorst-Pack *k*-point mesh for geometrical optimization and $21 \times 21 \times 1$ for electronic states [39]. To avoid interactions between periodic images, a 20 Å vacuum space is set to monolayer SnS_2 [40].

The transport properties are simulated based on the DFT method combined with the nonequilibrium Green's function formalism, using the Atomistix ToolKit 2019 package [41]. The drain current, I_{DS}; at a given bias voltage, V_b; and gate voltage, V_g, is calculated through the following Landauer-Bűttiker formula [42,43]:

$$I_{DS}(V_b, V_g) = \frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E,\ V_b, V_g)[f_S(E-\mu_s) - f_D(E-\mu_D)]\}dE,$$

where $T(E, V_b, V_g)$ represents the transmission coefficient; μ_S/μ_D and f_S/f_D represent the electrochemical potentials and the Fermi-Dirac distribution functions, respectively, of the source and drain. The transmission coefficient, $T(E)$, is the average of *k*-dependent transmission coefficients $T_{k//}(E)$ over different *k* points in the 2D Brillouin zone, where the reciprocal lattice vector $k_{//}$ is perpendicular to the transport direction. The *k*-dependent transmission coefficient is expressed by

$$T_{k_{ll}}(E) = Tr[\Gamma^S_{k_{ll}}(E)G_{k_{ll}}(E)\Gamma^D_{k_{ll}}(E)G^\dagger_{k_{ll}}(E)],$$

where $G_{k_{ll}}(E)$ and $G^\dagger_{k_{ll}}(E)$ represent the retard and advanced Green functions, respectively; $\Gamma^{SD}_{k_{ll}}(E) = i(\Sigma_{SD} - \Sigma^\dagger_{SD})$ is the broadening width originating from source and drain in the form of self-energy Σ_{SD} [44].

The exchange-correlation interaction is also described by the GGA together with PBE parameterization. We choose the double-zeta polarized basis set. The real-space mesh cutoff is set to 75 hartree. The temperature is taken as 300 K. In the FET device, the *x* and *y* directions represent the two transport $M\Gamma$ and MK directions (Fig. S1 within the Supplemental Material [45]), respectively. For the FETs along the $M\Gamma$ direction, the *k* mesh (k_x, k_y, and k_z) is set to $50 \times 1 \times 1$ and $50 \times 1 \times 50$ for the central region and the electrode region, respectively. For the FETs along the MK direction, the *k* mesh (k_x, k_y, and k_z) is set to $1 \times 50 \times 1$ and $1 \times 50 \times 50$ for the central region and the electrode region, respectively.

III. RESULTS AND DISCUSSION

First, we carry out DFT simulations to examine the atomic and electronic properties of monolayer SnS_2, which are the cornerstones of device performances. The equilibrium atomic structure of monolayer SnS_2 is shown in Fig. 1(a). Monolayer SnS_2 occurs in a CdI_2-type structure with $P\bar{3}m1$ space group, where each Sn is bonded to six S and each S is bonded to three Sn. One Sn and two S atoms are located in the hexagonal unit cell, with an optimized lattice parameter ($a = b$) of 3.70 Å to construct the S-Sn-S trilayer structure.

To study the electronic properties of monolayer SnS_2, we calculate the band structure along the high-symmetry path (K-M-Γ-K) in Brillouin zones [Fig. 1(b)]. As shown in Fig. 1(c), monolayer SnS_2 has an indirect gap of about 1.59 eV, which is an appropriate value for the channel material of MOSFETs. The CBM is located at the M point and the VBM is located between the M and Γ points. To obtain a deeper insight into the electronic structure of monolayer SnS_2, we calculate the band-decomposed charge-density distributions corresponding to CBM and VBM, as illustrated in Figs. 1(d) and 1(e). Combined with the analysis of the partial density of states (PDOS) in Fig. S2 within the Supplemental Material [45], it is found that the CBM of monolayer SnS_2 is contributed by the $3p$ orbitals of S atoms and $5s$ orbitals of S atoms, whereas the VBM is only dominated by the $3p$ orbitals of S atoms. Additionally, monolayer SnS_2 exhibits a much higher density of states near the valence-band edge than that of the conduction-band edge. The large disparity between the charge density and distributions of the VBM and CBM of monolayer SnS_2 could impact on the transport properties in *p*-type or *n*-type devices [46].

Inspired by the suitable electronic properties, we then investigate the DG MOSFETs, with intrinsic monolayer

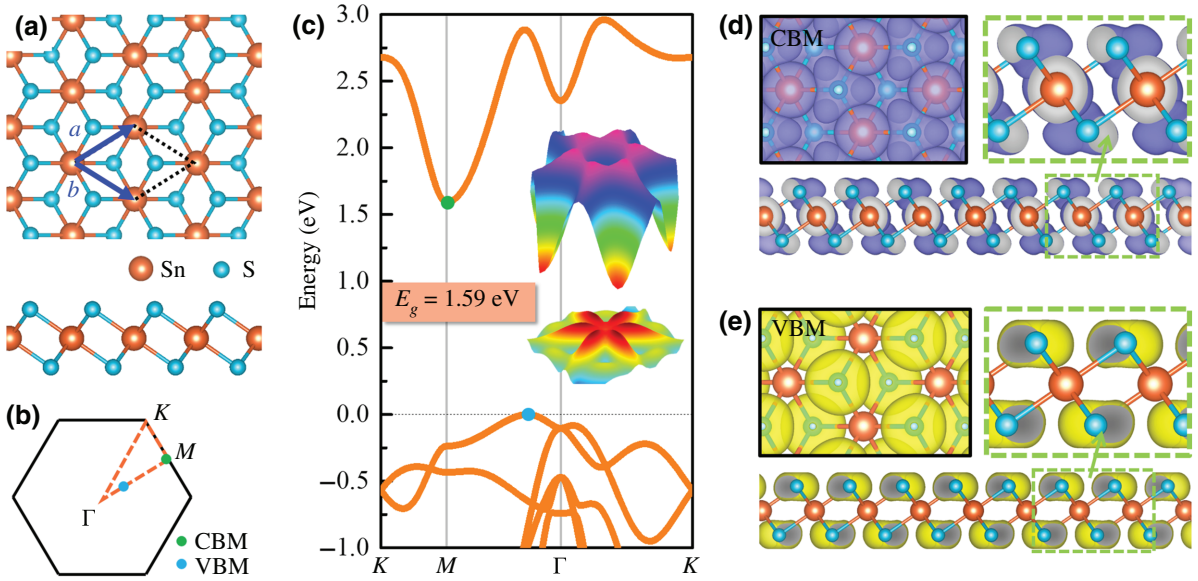

FIG. 1. (a) Top and lateral views of the atomic structure of monolayer SnS_2. Lattice parameter ($a = b$) is 3.70 Å. (b) Schematics of Brillouin zones for monolayer SnS_2. (c) Band structure of monolayer SnS_2 by PBE functional. Inset: three-dimensional band structure near the Fermi level. Band-decomposed charge-density distributions corresponding to (d) conduction-band minimum (CBM) and (e) valence-band maximum (VBM) of monolayer SnS_2. Isovalue is 0.003 e/bohr^3.

SnS_2 as the channel embedded in the top and bottom SiO_2 dielectrics, as shown in Fig. 2. The dielectric thickness and constant are set to 0.41 nm and 3.9, respectively. The source and drain electrodes are monolayer SnS_2 doped with acceptors and donors, corresponding to the n-type and p-type devices, respectively. The gate length (L_g) is equal to the channel length (L_{ch}) in all monolayer SnS_2 MOSFETs. Additionally, due to the anisotropic electronic

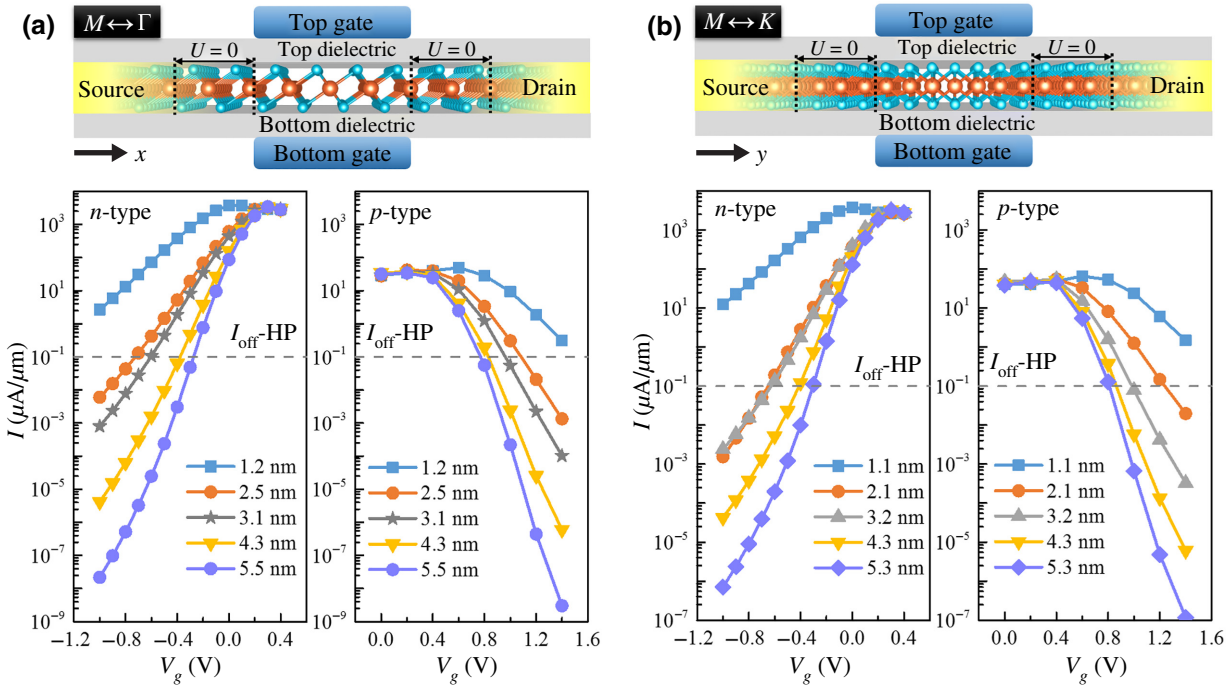

FIG. 2. Schematic view and transfer characteristics of monolayer SnS_2 MOSFETs along (a) $M\Gamma$ and (b) MK directions for HP applications, with $V_{DS} = 0.64$ V, several channel lengths (L_{ch}), U (underlap) = 0 nm, and dielectric thickness $t_{ox} = 0.41$ nm. Optimized electrode doping concentration is 5×10^{13} cm^{-2}.

structure of monolayer SnS_2, we consider two transport directions ($M\Gamma$ and MK) when constructing the FET. The transfer characteristics as a function of the channel length from 5.5 to 1.1 nm are shown in Fig. 2, with an optimized electrode doping concentration of 5×10^{13} cm^{-2}.

The device simulation results demonstrate that *n*-type monolayer SnS_2 MOSFETs have high I_{on} and on:off ratio that can satisfy the IRDS 2018 requirements for HP applications for the year 2028 until the channel length shrinks to 4.3 nm. I_{on} is a vital figure of merit for a logic-switch device, especially for HP devices, because the high *on*-state current signifies the fast operating speed. I_{on} is defined as the largest current driven by the transistor at a gate voltage V_g (on) $= V_g$ (off) $+ V_{dd}$, where V_{dd} ($V_{dd} = V_{DS}$) is the supply voltage and V_g (off) is the gate voltage corresponding to the *off* state. We obtain the *off* -state current (I_{off}) according to the IRDS requirements. For the *n*-type FETs along the $M\Gamma$ direction, at $L_g = 5.5$ nm, I_{on} reaches up to 3.4×10^3 μA/μm, which far exceeds the IRDS goal of 923 μA/μm for HP applications. When L_g is scaled down to 4.3 nm, I_{on} maintains a high value of 2.8×10^3 μA/μm. A similar high I_{on} can also be observed in *n*-type MOSFETs along the MK direction [Fig. 2(b)], which is 3.2×10^3 μA/μm at $L_g = 5.3$ nm and 2.8×10^3 μA/μm at $L_g = 4.3$ nm. If we continue to reduce the channel length ($L_g = 1$–3 nm), the source-drain tunneling rapidly degrades and fails to meet the IRDS requirement. Furthermore, the counterpart *p*-type monolayer SnS_2 MOSFETs present a very low I_{on} (less than 100 μA/μm), in both the $M\Gamma$ and MK directions. The reason for the performance difference between the *n*-type and *p*-type monolayer SnS_2 MOSFETs is systematically investigated and discussed later in this paper.

From the transfer characteristics, we can also obtain another key figure of merit, subthreshold swing (S_{sub}), to describe the gate-control ability of devices. S_{sub} is defined as the required gate voltage to change the current by one decade and can be expressed by $S_{sub} = \partial V_g / \partial Lg I_{DS}$ [47]. Smaller S_{sub} means better gate-control ability and the limiting value of S_{sub} at room temperature is 60 mV/dec [48]. We calculate the S_{sub} values of the *n*-type monolayer SnS_2 MOSFETs, as summarized in Table SI within the Supplemental Material [45]. The S_{sub} of 5.5 nm *n*-type MOSFET along the $M\Gamma$ direction is 83 mV/dec. When the channel length is shortened to 4.3 nm, the S_{sub} increases to 112 mV/dec. For the MK transport direction, the S_{sub} values of 5.3 and 4.3 nm FETs are 90 and 103 mV/dec, respectively.

To reveal the gate-modulation mechanism in different channel lengths, we calculate the position-resolved local density of states (LDOS) and the spectral current of the *n*-type monolayer SnS_2 MOSFETs in the $M\Gamma$ direction, as shown in Fig. 3. The energy barrier, Φ_B, which is defined as the energy difference between the source and the lowest value of the channel CBM, can demonstrate the difficulty of electrons at the CBM being transported from source to drain. For 5.5 nm L_g, an energy barrier of 0.14 eV appears at $V_g = -0.3$ V, indicating the *off* state in Fig. 3(a). This effective energy barrier is able to suppress the transport of electrons from the source to the drain, which corresponds with the fact that the total current is supplied by both the thermal current, I_{therm}, and tunneling current, I_{tunnel}. When V_g is increased to 0.34 V (the device is then in the *on* state), the energy barrier becomes 0 eV and I_{therm} dominates the total current in Fig. 3(b). For the FET with 3.1 nm L_g at $V_g = -0.3$ V, the energy barrier is quite small due to the short-channel effect, indicating that it is difficult to realize the *off* state at this gate voltage. Hence, the total current at $V_g = -0.3$ V is mainly contributed to by thermal current I_{therm} and is higher than that of the FET with 5.5 nm L_g.

We further analyze the conduction and valence bands of monolayer SnS_2 to understand the transfer characteristics of the *n*-type and *p*-type monolayer SnS_2 MOSFETs. First, we calculate the energy contour plots of the CBM and VBM and the effective masses along two transport directions of monolayer SnS_2 in Fig. S3 within the Supplemental Material [45]. Because the CBM is located at point M and the VBM is located at the point between Γ and M, there are three CB valleys and six VB valleys in the first Brillion zone of monolayer SnS_2. The three valley degeneracies and light electron effective masses indicate a high I_{on} of the *n*-type monolayer SnS_2 MOSFETs, which are found in other 2D channel materials [46,49].

For the VB, the six valleys and several heavy hole effective masses of monolayer SnS_2 determine its ultrahigh density of states (DOS), which would influence the transmission and current of *p*-type FETs [50]. To explore the transmission properties of the *n*-type and *n*-type MOSFETs, we calculate the transmission spectra in a homogeneous setting without any potential difference in Fig. 4. Under an electrode doping concentration of 5×10^{13} cm^{-2}, the transmission of the VB in the *p*-type device is farther from the Fermi level than that of the CB of the *n*-type. Hence, the *p*-type device has a lower hole transmission than that of the *n*-type and a lower hole current. Moreover, if the doping concentration is increased, the transmission of the VB in the *p*-type device is shifted more difficultly than that of the CB in the *n*-type device. When the doping concentration is increased to 2×10^{14} cm^{-2}, the transmission of the *p*-type device is still very low. These *p*-type transmission properties are deterministic by the ultrahigh VB DOS of monolayer SnS_2 (Fig. S2 within the Supplemental Material [45]) [50].

Furthermore, we employ the transmission eigenstates at (E, k) to reflect the relationship between the CBM or VBM orbitals and the carrier transport at the *on* state. As shown in Fig. S4 within the Supplemental Material [45], the energy value of the spectral current peak is selected as the E of the transmission eigenstates, and the valley

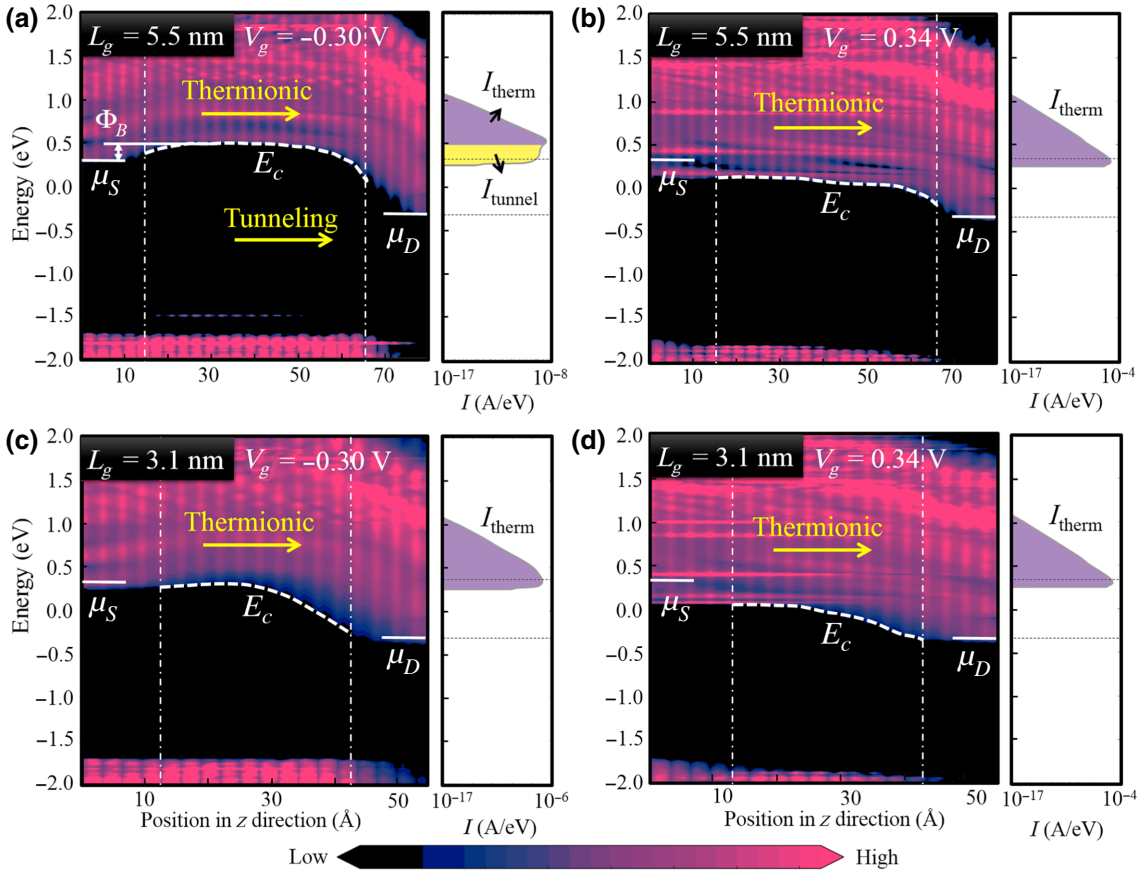

FIG. 3. Comparison of LDOS and spectral current of the *n*-type MΓ-direction monolayer SnS_2 MOSFETs under $V_{DS} = 0.64$ V. 5.5-nm-channel-length FETs at (a) $V_g = -0.3$ V for *off* state and (b) $V_g = 0.34$ V for *on* state. 3.1-nm-channel-length FETs at (c) $V_g = -0.3$ V and (d) 0.34 V. In the LDOS, μ_S and μ_D represent the electrochemical potential of the source and drain, respectively, and are marked by the gray dotted line in the spectral current. Yellow arrows imply thermionic and tunneling electron transport, white dotted line is the conduction-band edge (E_c), and Φ_B is the energy barrier for electrons.

of the CBM or VBM is folded as the k point. Therefore, the electron or hole wave functions of the corresponding transmission eigenstates can be considered to be largely contributed by the CBM or VBM of monolayer SnS_2. As shown in Figs. S5(a) and 5(b) within the Supplemental Material [45], at the *on* state, the incoming wave functions can pass through the channel from the source to reach the drain in both *n*-type and *p*-type monolayer SnS_2 MOSFETs. For the n-type device in Fig. S5(a) within the Supplemental Material [45], the electron wave functions are localized over Sn and S atoms, illustrating that the incident state can transport by hopping between the orbitals of S and Sn atoms. For the *p*-type device in Fig. S5(b) within the Supplemental Material [45], the hole wave functions are localized over the S atoms and the incident state can only transport by hopping between the p orbitals of S atoms. The weaker orbital overlap in the *p*-type FETs would influence the hole transport and limit the hole current, to a certain extent. These results are in agreement with the charge-density distributions of CBM and VBM in Figs. 1(d) and 1(e).

To better evaluate the I-V performance of the monolayer SnS_2 MOSFETs, we compare I_{on} of the MOSFETs with diverse 2D material channels from previous reports in Fig. 5(a) while I_{off} is set to 0.1 μA/μm, according to the IRDS 2018 goals for the year 2028 for HP applications. For data compatibility, we select channel lengths from 4 to 7 nm. When the channel length is reduced to sub-7 nm, the monolayer SnS_2 MOSFETs along two transport directions both possess obviously higher I_{on} values than those of other reported 2D MOSFET materials, for example, MoS_2, Bi_2O_2Se, phosphorene, arsenene, and tellurene [31–34,46,51,52].

In addition to the I_{on}, intrinsic delay time (τ) and PDP are another two essential metrics of transistors. The value of τ corresponds to the upper limit of switching speed in a logical circuit, which is defined as $\tau = (Q_{on} - Q_{off})/I_{on}$, where Q_{on} and Q_{off} represent the channel charges at the *on* and *off* states, respectively [54]. The PDP signifies the power consumption in a single switching system and is obtained by PDP $= (Q_{on} - Q_{off})V_{DS}$. Figure 5(b) demonstrates PDP versus τ of the monolayer SnS_2 MOSFETs

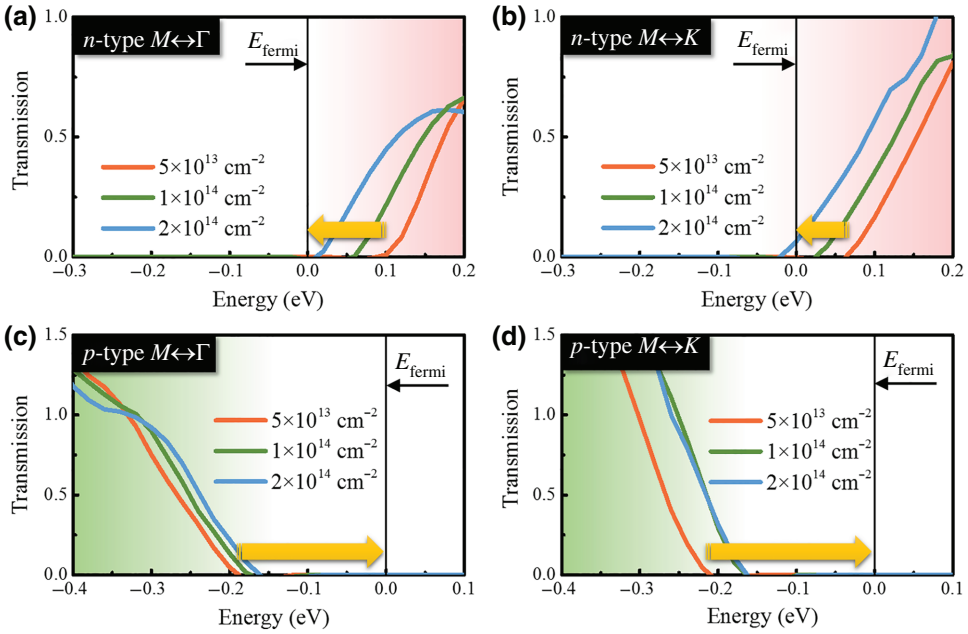

FIG. 4. Transmission spectra of monolayer SnS_2 MOSFETs under $V_{DS} = 0$ V, with 5.5 and 5.3 nm channel lengths at $V_g = 0$ V, with different electrode doping concentrations (N_e).

and a comparison with other 2D materials, with the IRDS 2018 requirements labeled in cyan. Based on the above-mentioned definitions, it is important to obtain low τ and PDP. Hence, data in the bottom-left corner indicate superior performance. Notably, τ and PDP of all monolayer SnS_2 MOSFETs surpass those of the IRDS 2018 requirements for HP applications, even obviously lower than those of black phosphorene [46], MoS_2 [53], Bi_2O_2Se [52], and tellurene [34]. The τ and PDP values of all monolayer SnS_2 MOSFETs can be found in Table SI within the Supplemental Material [45].

To further evaluate the potential of monolayer SnS_2 as channel materials of LP applications, we test other electron doping concentrations. Under a doping concentration of 3×10^{13} cm^{-2}, the n-type monolayer SnS_2 MOSFETs with the 5.5 nm channel along the $M\Gamma$ direction can fulfill the I_{off} requirement of IRDS 2018, as shown in Figs. 6(a) and 6(b). According to the IRDS 2018 requirement for LP applications, I_{off} is intended to be 1×10^{-4} μA/μm, to reduce static energy consumption (Table SII within the Supplemental Material [45]). For the $M\Gamma$-direction FET at $L_g = 5.5$ nm, I_{on} is about 700 μA/μm and the I_{on}/I_{off}

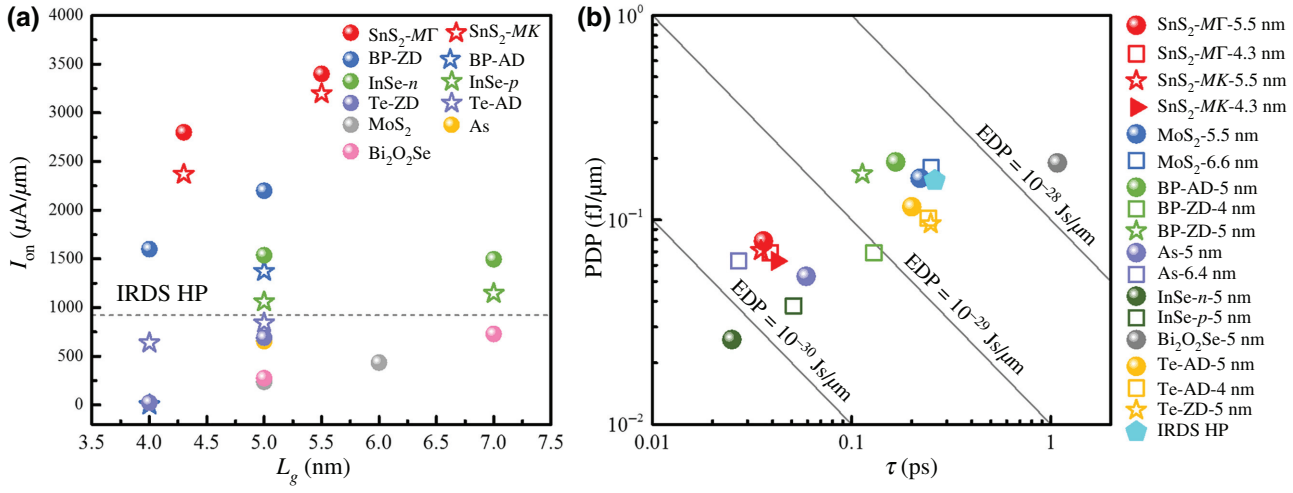

FIG. 5. (a) Optimal *on*-state current (I_{on}) versus gate length (L_g) around 5 nm for monolayer SnS_2 and other 2D MOSFETs materials in HP applications [31–34,46,51,52]. Gray dashed line at $I_{on} = 923$ μA/μm corresponds to represent IRDS 2018 requirements for HP applications for the year 2028. (b) Power-delay product (PDP) versus intrinsic delay time (τ) for monolayer SnS_2 and other 2D MOSFET materials in HP applications [32–34,46,52,53]. Gray solid lines represent specific energy-delay product (EDP).

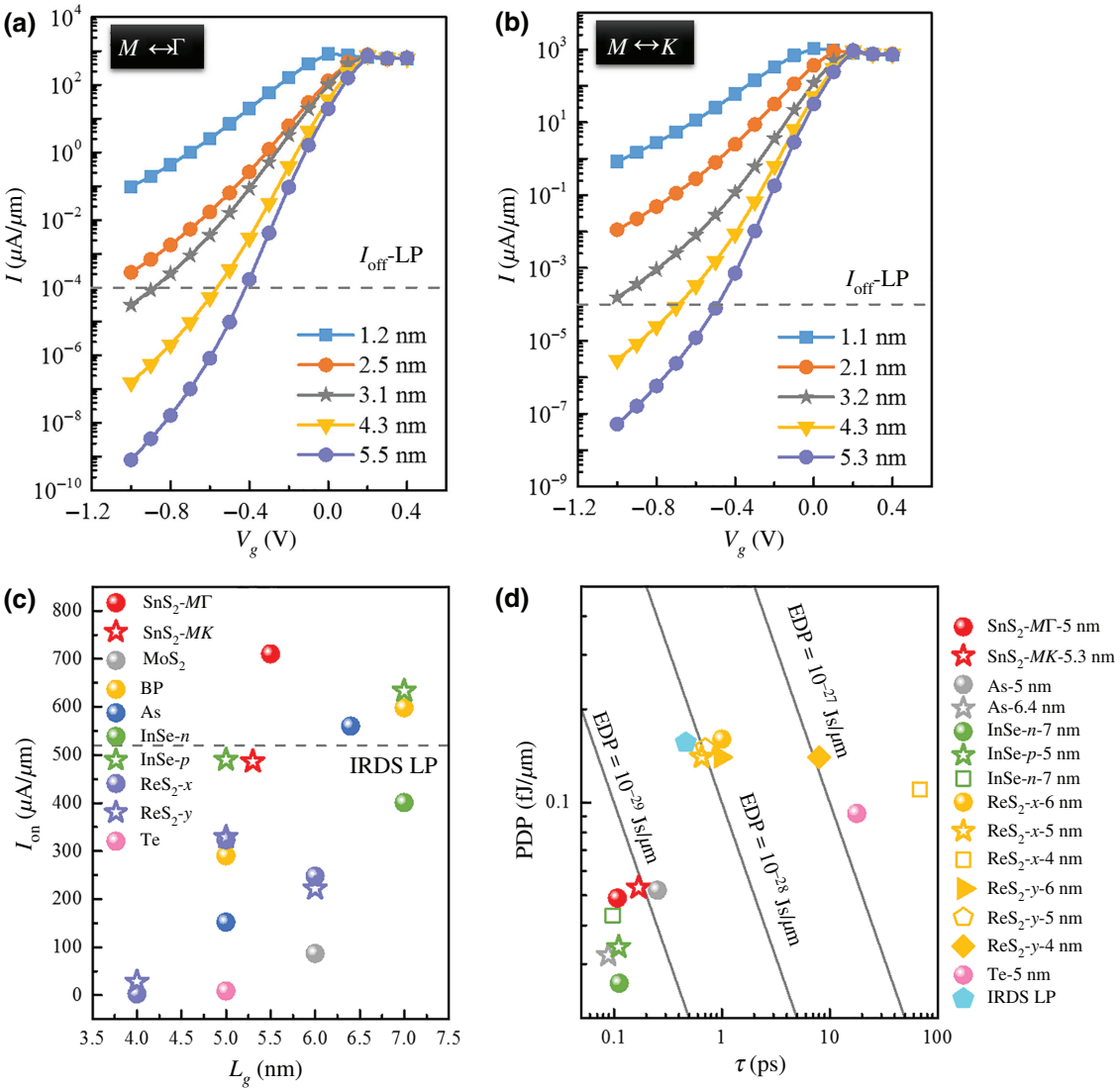

FIG. 6. Schematic view and transfer characteristics of monolayer SnS_2 MOSFETs along (a) $M\Gamma$ and (b) MK directions for LP applications, with $V_{DS} = 0.64$ V, several channel lengths, and $t_{ox} = 0.41$ nm. Optimized electrode doping concentration is 3×10^{13} cm^{-2}. (c) Optimal I_{on} versus L_g around 5 nm for monolayer SnS_2 and other 2D MOSFET materials in LP applications [31–34,55,56]. Gray dashed line at $I_{on} = 520$ μA/μm corresponds to IRDS 2018 requirements for LP applications for the year 2028. (d) PDP versus τ for monolayer SnS_2 and other 2D MOSFETs materials in LP applications [32–34,56]. Gray solid lines represent specific EDP.

value is close to 7.1×10^6, which is sufficient for LP processing. Furthermore, the difference in I_{on} between two transport directions in the LP monolayer SnS_2 MOSFETs is obviously larger than that in HP devices. The LP device focuses on subthreshold characteristics, whereas the HP device mainly focuses on superthreshold characteristics, as shown in Fig. S6 within the Supplemental Material [45]. The larger electron effective mass of valley 1 (Fig. S3 within the Supplemental Material [45]) along the $M\Gamma$ direction than that along the MK direction brings about a smaller leakage tunneling current along the $M\Gamma$ direction, leading to a higher I_{on} and on:off ratio. Nevertheless, due to the ultrashort-channel transport studied here, similar to ballistic transport, the electron effective mass difference has a smaller impact on superthreshold characteristics [57]. Hence, the I_{on} value of the HP devices along two transport directions presents a smaller difference. For shorter channel lengths ($\leq$5.3 nm), source-to-drain tunneling degrades I_{off} and the on:off ratio, which falls below the standard for LP applications.

As shown in Fig. 6(c), the I_{on} value of monolayer SnS_2 MOSFETs with a 5.5 nm channel along the $M\Gamma$ direction is comparable to those of other 2D materials, such as black phosphorene, 2D InSe, and arsenene [32–34,56]. In particular, I_{on} of 5.5 nm along the $M\Gamma$ direction reaches 137% of the requirement of IRDS 2018. The calculated values of

τ and PDP of the 5.5 nm monolayer SnS_2 MOSFETs in Fig. 6(d) can also fulfill IRDS 2018 requirements for LP applications.

IV. CONCLUSION

Here, we investigate the intrinsic electronic properties and ultrascaled device performance of a 2D monolayer SnS_2 material. The electronic band structure of monolayer SnS_2 is described by the DFT method, exhibiting a 1.59 eV indirect band gap and distinct charge distributions around the CBM and VBM. The *n*-type monolayer SnS_2 MOSFETs present a much higher I_{on} than that of the *p*-type MOSFETs. It is shown that the monolayer SnS_2 *n*-MOSFETs can meet the IRDS targets for HP devices, in terms of I_{on}, delay time, and PDP, even when the channel length is scaled down to 4.3 nm. In particular, the SnS_2 *n*-MOSFET with 5.5 nm L_g offers an ultrahigh I_{on} of up to 3400 μA/μm, exceeding most reported 2D materials. Additionally, the 5.5 nm SnS_2 *n*-MOSFET shows excellent device performance that can meet the IRDS 2018 requirements for LP processing. Hence, the outstanding properties of the monolayer SnS_2 MOSFETs endow them with great potential for future competitive HP and LP digital applications.

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