Deep-Level Transient Spectroscopy of GaAs Nanoridge Diodes Grown on Si Substrates

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Monolithically integrated GaAs *p-i-n* diodes are demonstrated on 300-mm Si (001) substrates using a nanoridge-engineering approach. Deep-level transient spectroscopy (DLTS) is used to perform defect analysis for nanoridge and planar GaAs diodes. The point defect, EL2 with $N_T \simeq 3 \times 10^{14}$ cm^{-3}, is observed for nanoridge *p-i-n* diodes. A methodology is developed to extract the surface-state density (N_{SS}) directly from the DLTS spectrum. GaAs nanoridge diodes show $N_{SS} \simeq 2 \times 10^{13}$ cm^{-2} compared to planar diode approximately 6.5×10^{12} cm^{-2}. A clear correlation is observed between dark current and defect density. An investigation on the impact of an *in situ* and *ex situ* passivation layers on the leakage current reduction is performed for GaAs *p-i-n* diodes.

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I. INTRODUCTION

III-V-based semiconductor materials have several advantages such as higher mobility, breakdown voltage, conversion efficiency, and a direct band gap compared to silicon, conventionally used for CMOS devices. These benefits have led to an increased interest, in the last few decades, in their application in logic and high-frequency devices [1,2], light-emitting diodes [3,4], hybrid lasers [5, 6], photodetectors [7,8], and solar cells [9,10]. However, current III-V technologies utilize expensive native substrates for device fabrication, which are not a cost-effective solution for high-volume production requirements.

The monolithic integration of III-V materials on silicon allows a direct combination of the unique properties of advanced compound semiconductors with highly scalable and cost-effective commercial CMOS technology.

Unfortunately, direct epitaxial growth of III-V materials, such as GaAs on standard Si (001) is challenging and has an impact on device performance [11,12]. This is due to the significant 4% lattice mismatch between GaAs and Si, as well as the 60% difference of their thermal expansion coefficients. Moreover, direct nucleation of GaAs on Si poses the threat of undesirable antiphase domain formation.

These challenges can be addressed by the use of different engineering approaches such as direct wafer-to-wafer bonding [13,14], strain-relaxed buffer engineering [15, 16], and three-dimensional (3D) stacked flip-chip packaging [17,18]. Recently, a method of controlling the defect density in epitaxially grown layers is demonstrated for Ge [19,20] and III-V materials [21–23]. In this so-called aspect-ratio trapping (ART) approach, the selective area growth of III-V materials in highly confined patterns directly on a Si (001) wafer allows for efficient control over defectivity in the device structure. Using this method, the monolithic integration of III-V devices with low defect density on Si is finally possible as relaxation defects are trapped at the pattern side walls close to the III-V/Si interface. Nanoridge engineering (NRE) is based on ART but adds the advantage that an engineered nanoridge (NR) acts as the device region, which is clearly separated from the defective area of the strain relaxation. The monolithic integration starts with the growth of GaAs inside a trench pattern with high aspect ratio for efficient defect trapping and is continued outside of the trenches. The shape of the nanoridges, which evolves on top of the trench pattern, can be controlled by the applied growth parameters. Due to a pronounced increase in III-V volume together with a low defect density these NRs are very suitable for recent III-V device architectures on Si. The potential of NRE for III-V device integration on Si is emphasized by the demonstration of nanoridge-based laser diodes and heterojunction bipolar transistors (HBTs) [24,25]. More details about NRE are reported in Refs. [26–28].

Another challenge related to III-V-based devices is the presence of surface states located at an unpassivated

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region such as mesa side walls, whose density depends upon the fabrication and, in particular, precleaning and passivation methods. For GaAs devices, the values of the surface-state density (N_{SS}), reported by different authors are between 5×10^{11} $cm^{-2}\,eV^{-1}$–7×10^{12} $cm^{-2}\,eV^{-1}$ [29–31], whereas Si/SiO_x has a value of 1×10^{10} $cm^{-2}\,eV^{-1}$ [32]. The high surface-state density causes many harmful effects such as high leakage current, loss of efficiency, and reliability issues. These problems create a requirement for better III-V surface-passivation methods.

In this work, we report a deep-level transient spectroscopy (DLTS) study of the bulk and surface traps in vertical GaAs nanoridge diodes heteroepitaxially grown on Si substrates compared with homoepitaxial planar diodes deposited on GaAs substrates. We show that by careful control of defect density and fabrication process, NR diodes can achieve performance similar to the classical planar diodes fabricated on native GaAs substrates. We focus on the correlation between defect density, in particular, bulk and surface traps, and leakage current. A methodology for extracting the surface-state density of *p-i-n* diodes is proposed and used to compare structures with different passivation and mainly to study the impact of N_{SS} on leakage current.

II. EXPERIMENTAL METHODS

A. Sample fabrication

All GaAs diodes are grown by MOVPE. A planar GaAs *p-i-n* diode (sample A), which is deposited on a 2-inch highly *n*-doped GaAs substrate, is used as a homoepitaxial reference device to be compared with two different NR diode structures (samples B and C) grown on the trench-patterned Si substrates. The narrow trenches with about 80 nm width are processed in a 300-nm-thick SiO_2 layer on a 300-mm Si (001) substrate. The top Si layer is highly *n* doped and the trench formation is based on a standard shallow trench isolation (STI) process. The Si surface inside of the trenches is wet etched with tetramethylammonium hydroxide (TMAH) in order to expose two {111} facets to avoid the formation of antiphase disorder in GaAs. Sample B represents a standalone NR diode, which suffers sidewall deposition of all doped layers around the NR but also enables the growth of an *in situ* $In_xGa_{1-x}P$ passivation layer around the complete NR structure. To explore the impact of such an *in situ* passivation, a 20-nm-thick undoped $In_xGa_{1-x}P$ layer is deposited *in situ* after the growth of the GaAs diode layers. Details about the NR growth can be found in previous publications [26–28]. Sample C is a NR diode integrated in a second template oxide. As the *n*-doped GaAs NR touches the second template oxide, no side wall deposition of the *p*-doped layer is observed. Additional growth details are reported in Ref. [25]. In order to also add an $In_xGa_{1-x}P$ passivation to sample C, the second template oxide is removed by wet etch and the $In_xGa_{1-x}P$ layer is added in a regrowth step loading the wafer a second time into the epitaxy chamber. The planar GaAs *p-i-n* diode (sample A) is deposited under comparable MOVPE conditions as the GaAs NR diodes. The diode-layer sequences, which count from the oxide STI, and doping concentrations of samples A, B, and C are summarized in Table I. Figure 1 holds several images to explain the different device layouts as well as the metal contacting approach. The defect density in the GaAs NR diodes is expected to be below 5×10^5 cm^{-2} as reported in Ref. [28].

After the NR growth, sample B gets a thick SiO_2 planarization deposition step, which is formed by plasma-enhanced atomic layer deposition (PEALD) and high-aspect-ratio process (HARP) atmospheric chemical vapor deposition (CVD), followed by the chemical mechanical polishing (CMP) process. The details of the process flow for sample C with the second template oxide can be found in the previous publication [25]. Sample C with the additional *ex situ* $In_xGa_{1-x}P$ passivation is subsequently processed in the same way as sample B as the second oxide removal leads to standalone NR again. For the fabrication of electrical contacts, a combination of the wet etching and sputtering of Ti/TiN/Al or Ti/Mo/Al is used for NR diodes. The devices are biased using contacts to the top p^+-GaAs layer and n^+-Si substrate. The device length of the NR diodes, L_{NR}, is around 100 μm. In the case of NR diodes, the metal contacts are located around 5 μm away from the ends (edges) of the nanoridge. It is known in NR growth that different NR facets evolve at the trench ends [33]. Therefore, the thickness of the different diode layers changes and might influence the diode behavior. In order to check the impact of a passivation layer on the device performance, several *ex situ* passivation layers

TABLE I. Structure of the fabricated GaAs *p-i-n* diodes.

Layer	Sample A	Sample B	Sample C
p^+	100 nm, 3×10^{19} cm^{-3}	40 nm, 9×10^{18} cm^{-3}	200 nm, 9×10^{18} cm^{-3}
p	200 nm, 1×10^{18} cm^{-3}	130 nm, 2×10^{17} cm^{-3}	...
n^-	400 nm, 5×10^{16} cm^{-3}	400 nm, 2×10^{17} cm^{-3}	400 nm, 2×10^{17} cm^{-3}
n^+	200 nm, 1×10^{19} cm^{-3}	200 nm, 1×10^{19} cm^{-3}	200 nm, 1×10^{19} cm^{-3}
Substr	2-inch GaAs	300-mm Si	300-mm Si

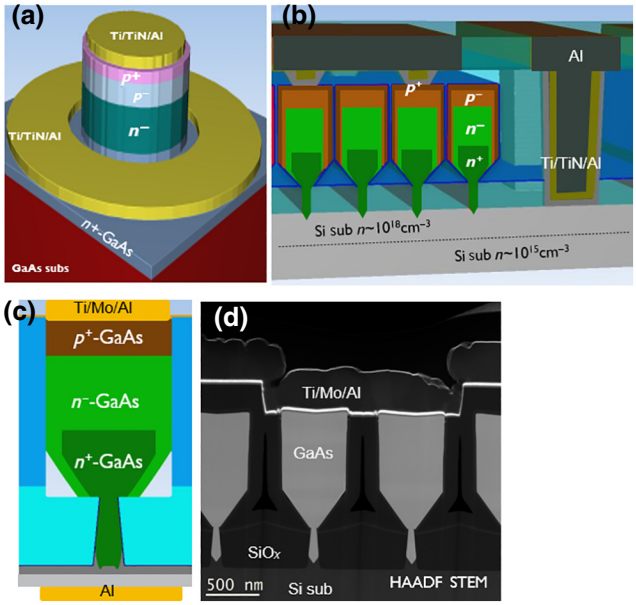

FIG. 1. (a) Planar GaAs *p-i-n* diode (sample A), (b) standalone NR diode (sample B), (c) NR buried in second oxide to avoid side-wall deposition (sample C), and (d) high-angle annular dark-field scanning TEM (HAADF STEM) image for sample C.

are applied to sample A. AlO_x and HfO_x are added by atomic layer deposition (ALD) and SiO_x is deposited by CVD. If not mentioned explicitly in this work, no additional passivation layer is used. The mesa diameter of the planar diode (sample A) is 200 μm and in the case of NR diodes, 100–220 nanoridges are connected in parallel.

DLTS is performed on *p-i-n* diodes with a Semilab DLS-83D tool using a capacitance bridge operating at 1 MHz. The diodes are mounted in a vacuum chamber and a closed-cycle helium cryostat from Lake Shore can be used to cool samples even below 77 K. During the DLTS measurements, the temperature varies between approximately 10 and 400 K, additionally, a bias is periodically applied from V_R (quiescent reverse bias) to V_P (pulse bias) to the top contact of the *p-i-n* diodes. This helps to fill the deep levels in intrinsic region of the *p-i-n* diode with majority carriers ($V_P < 0$) or minority carriers (holes) when $V_P > 0$. The pulse duration is denoted by t_p and the emission-rate window, determined by a lock-in integrator, is represented by t_w. The sensitivity of the capacitance compensator is 10 pF, and the integration time of the lock-in integrator is 3 s.

B. Methodology to distinguish and estimate the density of bulk and surface defects

Traditionally, the characterization of bulk defects and surface states can be achieved by DLTS, which has been widely used for GaAs [34–37], InP [35], GaN [38], or InGaAs [39,40] MOS capacitors and *p-n* diodes. By using Arrhenius plots and carefully changing measuring conditions, DLTS can be used to extract defect levels and to differentiate between various types of defects, respectively. Especially for such monolithic III-V integration approach and NR architecture, distinguishing between bulk defects introduced by the epitaxial growth or surface defects induced by device processing becomes critical. Separating these bulk- and surface-related defects allows for a better understanding of the origin of the leakage current observed in the GaAs diodes.

Differences between the DLTS response of bulk traps such as point defect or extended defects (e.g., misfit, threading dislocation) and surface states have been intensively studied and can be summarized as follows.

(1) At lower electrical field (small reverse bias) during trap emission: in the case of bulk traps with a discrete energy level, the emission rate at a given temperature is constant regardless of the pulse voltage V_P, the peak temperature of DLTS signal ΔC versus T plot does not change with V_P. This is in contrast to the significant shift observed for a distribution of the density of states (DOS), that is intrinsic to the surface state type of defects.

(2) Localization of surface states has a delta function-like spatial distribution at the interface independent on the energy distribution.

(3) For the surface potential near the trap energy $E_T(\tau_0)$, the emission threshold is broadened by surface-potential fluctuations, thereby leading to a broadening of the DLTS spectrum, which is characteristically different from the narrow and sharp peak of point defects (FWHM is approximately 20–50 K depending on temperature).

(4) In the case of an extended defect, the DLTS signal increases logarithmically with the pulse duration t_p and reaches saturation at very long t_p [41].

Bulk trap concentration (N_T) is calculated from individual DLTS peak heights, accounting for the depletion region volume where each particular trap state is modulated by the applied biases, or the so-called "λ-effect," for maximum accuracy. This is related to the presence of a free-carrier tail at the edge of the depletion region. Traps are filled in the region between $W_R - \lambda_R$ and $W_P - \lambda_P$ [42] can be expressed as

$$\frac{N_T(W_m - \lambda_m)}{N_D(x)} = 2\frac{\Delta C}{C_R}\left[\frac{1}{\left(1 - \frac{\lambda_R}{W_R}\right)^2 - \left(\frac{W_P - \lambda_P}{W_R}\right)^2}\right], \quad (1)$$

where $\lambda_R = \sqrt{2\epsilon_o\epsilon_s(E_F - E_T)/q^2N_D}$ is the distance from the crossing point of the Fermi level E_F with the trap level E_T and the edge of the depletion region [43], shown

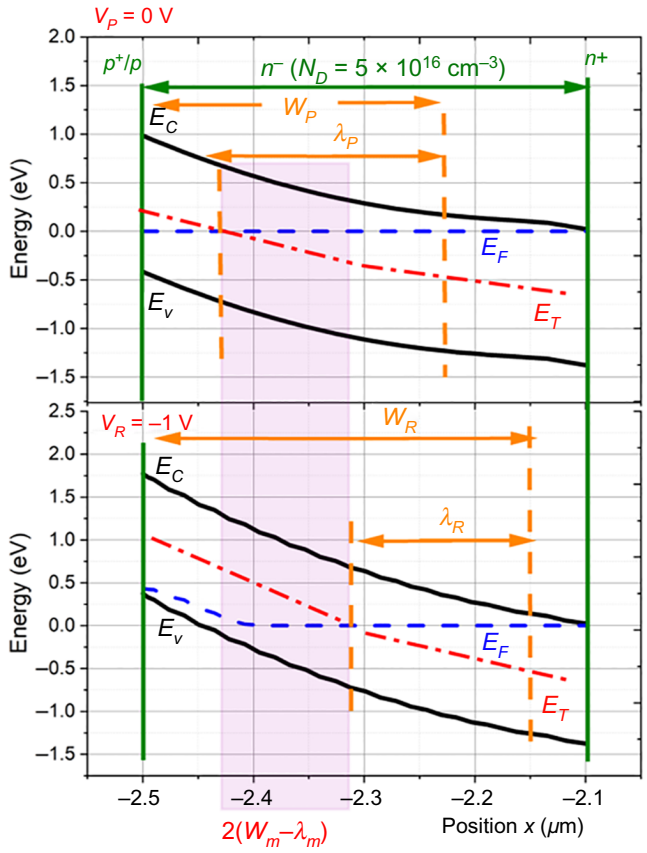

FIG. 2. Pictorial description of "λ-effect" for sample A at $V_R = -1$ V and $V_P = 0$ V.

in Fig. 2. C_R is the capacitance at reverse bias, $N_D(x)$ is the doping concentration spatially dependent profile of the measured layer, ΔC is the capacitance transient amplitude, W_R is the depletion depth under reverse bias, and $W_m - \lambda_m = 0.5\,[(W_R - \lambda_R) + (W_P - \lambda_P)]$.

On the other hand, the density of surface states in the case of MOS capacitors is extracted by using the following expression [34,44,45]:

$$D_{it} = \frac{\epsilon_o \epsilon_s A N_D \Delta C C_{\rm ox}}{\beta k_B T C_R^3}, \tag{2}$$

where A is the area of the depleted region, factor β is derived from the FWHM of a typical FFT DLTS peak and defines the energy resolution and $C_{\rm ox}$ is the oxide capacitance for MOS devices. However, in the case of planar and NR diodes, this correlation has the following limitations.

(1) The surface orientation of the side wall of a p-i-n diode is different from (100) orientation of the MOS interface. This difference in the orientation can induce a significant error in the defect density extraction.

(2) The side wall of the p-i-n diode undergoes various processing-related damage during the fabrication, hereby leading to a rougher and more defective surface as compared to interface of a MOS capacitor. This can lead to additional discrepancies in the above correlation.

(3) The nonuniform and complicated $C_{\rm ox}$ caused by a nonvertical electrical field to the surface passivation layer makes this expression (2) difficult to apply.

Therefore, a mathematical calculation is required to be able to directly extract the density of surface states at the side wall of a diode from the DLTS spectrum. This improves not only the accuracy of the surface-state characterization, but also increases the application range of the DLTS technique. In this work, we show a methodology for the surface-state density extraction at the side wall of p-i-n diodes.

The main advantage of this methodology is the ability of the DLTS technique to differentiate the response of surface and bulk defects. Assuming the DLTS response of the surface states is identified, the measured ΔC corresponds to the charge trapped by surface states. This charge equality approximation can be written as [46]

$$q \times N_D \times \Delta W_d \times A_{\rm bulk} = q \times N_{\rm SS} \times \Delta f_s \times A_{\rm surf}, \tag{3}$$

where the left-hand side of Eq. (3) represents the corresponding change in the depletion width ΔW_d due to the trap charge ($W_d N_T/2$ if $N_D \gg N_T$ in DLTS) and the right-hand side represents the negative of the charge at the side-wall surface, both as charge per unit area. $N_{\rm SS}$ is the density of surface states (having unit of cm^{-2}) assumed to be uniformly distributed across the band gap, $A_{\rm surf}$ corresponds to the effective side-wall generation-recombination (GR) area of GaAs p-i-n diode and $A_{\rm bulk}$ is the p-n-junction area of the diode. Δf_s is the fraction of levels of surface states between V_P and V_R, and can be derived from [46]

$$f_s = \frac{F_n - E_i - eV(1 - f_b)}{E_g}, \tag{4}$$

where f_b is the occupational probability of the surface states, F_n is the quasi-Fermi-level, E_i is the charge neutrality level, V is the applied bias, and E_g is the band gap of the material under investigation. F_n can be represented as $F_n = F + eV/2$, where F is an average of quasi-Fermi-levels.

The change in the depletion layer charge, $N_D \times \Delta W_d$, can be associated with the capacitance transient ΔC (per unit area) measured in DLTS by using the following equation [47] ($N_D \gg N_T$):

$$N_T = \frac{\Delta C}{C_R} \times 2N_D \times W_d. \tag{5}$$

By substituting Eqs. (4) and (5) in Eq. (3), we can obtain

$$N_{SS} = \frac{\Delta C}{C_R} \times N_D \times W_d \times \frac{A_{bulk}}{A_{surf}} \times \left[\frac{E_g}{\Delta F_n - e\Delta V + [V_P f_b(V_P) - V_R f_b(V_R)]} \right], \quad (6)$$

where $A_{bulk} = W_{n^-} \times L_{NR}$ and $A_{surf} = 2 \times t_{n^-} \times L_{NR}$ for nanoridge p-i-n diodes, where L_{NR} is the length of nanoridge, W_{n^-} is the width and t_{n^-} is the thickness of low-doped n layer, which are equal to 0.6 μm and 0.4 μm, respectively. The above set equations can be solved for N_{SS} by using the successive approximation method. In this way, the density of surface states can be extracted from the measured DLTS spectrum.

III. RESULTS AND DISCUSSION

A. Electrical characteristics

Figure 3 shows the I-V characteristic of the fabricated p-i-n diodes. The ideality factor and series resistance for sample A are found to be in the range of $n = 1.5$–2 and $R_s = 12\ \Omega$. The extracted threshold voltage, V_{th} is 1.2 V as expected for GaAs-based diodes. In comparison to the planar structure (sample A), NR diodes (samples B and C) show an ideality factor of $n = 2$ and $R_s = 32$–41 Ω. The difference in R_s can be related to additional resistive parts such as the NR trench region, the GaAs/Si interface, and the highly doped Si region, which are absent for sample A.

The leakage current, extracted at a fixed reverse bias of −1 V, shows a higher dark current for samples B and C than for sample A. To extract the individual contribution of the leakage mechanisms, I-V measurements are performed at different temperatures. The planar GaAs diode (sample A) has $E_{act} \sim E_g/2$, which corresponds to a Shockley-Read-Hall- (SRH) based generation-recombination component. The activation energy of the NR diodes (inset in Fig. 3) is in the range 0.1 eV $< E_{act} < E_g/2$, indicating the presence of another leakage mechanism like band-to-band tunneling (BTBT) or trap-assisted tunneling (TAT) [48,49].

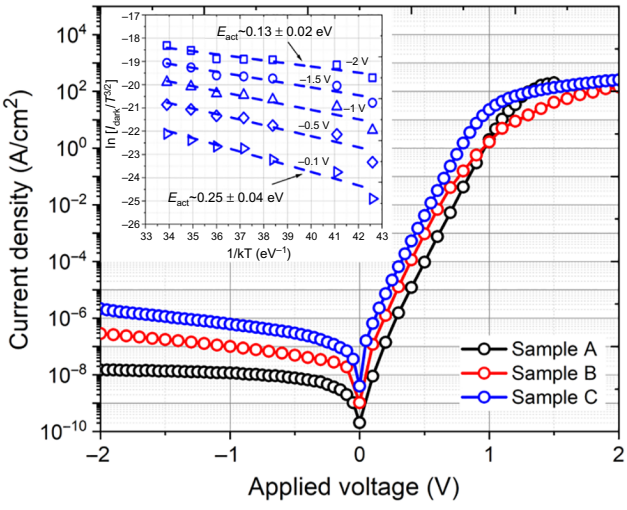

FIG. 3. I-V characteristic for GaAs p-i-n diodes. The inset shows Arrhenius plot for NR diodes at different reverse voltages.

Defects, such as threading dislocations (TD), are well-known contributors to the leakage current of a diode. In the ART and NRE crystal-growth methods, the TDD can be controlled by the optimization of the width and height of the trenches in the STI oxide. To estimate the TDs in our samples, we perform their characterization by the electron-channeling contrast imaging (ECCI) and TEM methods. No threading dislocations can be found within the field of view of ECCI (scan area). The extracted threading dislocation density is in the range of 10^5–10^6 cm^{-2} [28] for GaAs NR diodes. This is to be compared with 5×10^3–5×10^4 cm^{-2} TDD, observed for GaAs diodes fabricated on the native substrate. This indicates that nanoridge engineering is an effective tool in suppressing the TDD and consequently reducing dark current for III-V diodes grown directly on Si. Nevertheless, it should be noted that an impact of the NR edges requires further investigation.

Such TDD determines the effective trap density, which can be derived as [50,51]

$$N_T = f_{max} \times \text{TDD} \times \alpha, \quad (7)$$

where TDD is the measured (from ECCI) value of threading dislocation density (cm^{-2}), α is the line density of the traps at one dislocation (cm^{-1}), f_{max} is the maximum filling factor, and N_T is an effective trap density (cm^{-3}). Therefore, N_T is 10^{11}–10^{12} cm^{-3} of threading dislocation for samples B and C, which is smaller than the extracted effective trap density of point defects. In addition, considering a TD occupation probability in the range of 0.03–0.2 [52] and DLTS sensitivity level limited to $10^{-5} \times N_D$ [47], the lowest TDD that is detectable by DLTS, lies in the range of 3.5×10^5–2×10^6 cm^{-2} [53]. Therefore, TDD for all presented GaAs p-i-n diodes is below the detection level of DLTS. Based on the above discussion, we assume that the threading dislocations do not contribute significantly to the leakage current of the p-i-n diodes presented in this work.

In general, the total leakage current can be expressed as a sum of the bulk and surface components, $I_{tot} = I_{bulk} + I_{surf}$. In the next sections, we utilize the DLTS-based characterization technique to extract the corresponding densities of the bulk and surface defects in order to understand the difference in the leakage current observed in different samples shown in Fig. 3.

B. Bulk traps

Using the double-DLTS (DDLTS) [54] spectrum, different types of bulk defects can be differentiated by the

impact of variation of pulse bias (V_P) on the position of the peak temperature and the shape of variation of transient capacitance (ΔC) [55,56].

Figure 4 shows the DDLTS signal for GaAs *p-i-n* diodes, where the negative peak corresponds to the majority carrier electron traps and the positive peak correlates with the minority carrier hole traps. The detected bulk traps are present as deep levels in the intrinsic region of the *p-i-n* diodes. The nanoridge diode with *in situ* passivation (sample B) shows a narrow peak E1 around 350 K and a broad H1 peak at 180 K.

The capture kinetics measurements [inset in Fig. 4(a)] show a typical exponential behavior with respect to the filling pulse time for both E1 and H1 peaks in comparison to the logarithmic dependency for an extended defect. Additionally, the emission rate at 350 K (E1 peak) is constant regardless of the pulse bias V_P. As a result, the peak temperature and the shape of the signal do not change. This behavior is the characteristic of point defects, E1 peak. Moreover, the temperature position of the peak is different from the electron trap (localized ED1), associated with extend defects (TD), shown at 280 K by Gelczuk [57] and Wosinski [58]. Therefore, the E1 peak in this work is a point defect called EL2. Such point defects are observed for samples A and B. It is one of the most widely investigated native deep-level defects in the bulk of epitaxially GaAs grown by different techniques [59,60]. The importance of this defect results from the fact that EL2 controls the electrical and optical properties of GaAs [61,62]. Originally, the family of EL2 traps is attributed to a complex of As antisite and an As interstitial, which has been studied extensively in the past [59,60,63,64].

Regarding the broad H1 peak in Fig. 4(a), the capture kinetics measurement does not show the clear logarithmic dependency and the emission rate at 180 K is not constant with respect to V_P. Therefore, the H1 peak can not be associated with either a point or an extended defect. Additionally, the temperature position of the peak is different from the hole trap (HD3), which is shown in a range of 250–280 K, which is representative of an extended defect [65]. Based on these observations, we assume that the H1 peak can be associated with the DOS on the surface and is discussed in detail in the next section.

Table II shows a comparison of the bulk defects, located at $T \sim 300$–400 K, concentration and levels extracted using Eq. (1). Sample A shows the lowest point-defect density $N_T = 1.2 \times 10^{13}$ cm^{-3}, lower than that obtained for NR-based diodes. Among NR-based diodes, sample C, which is fabricated using an oxide template [25], shows a higher concentration of point defect compared with sample B.

Additionally, another peak, corresponding with EL3, located nearby 300 K, is detected for samples B and C with *ex situ* passivation and can be associated with oxygen incorporation [66] in GaAs.

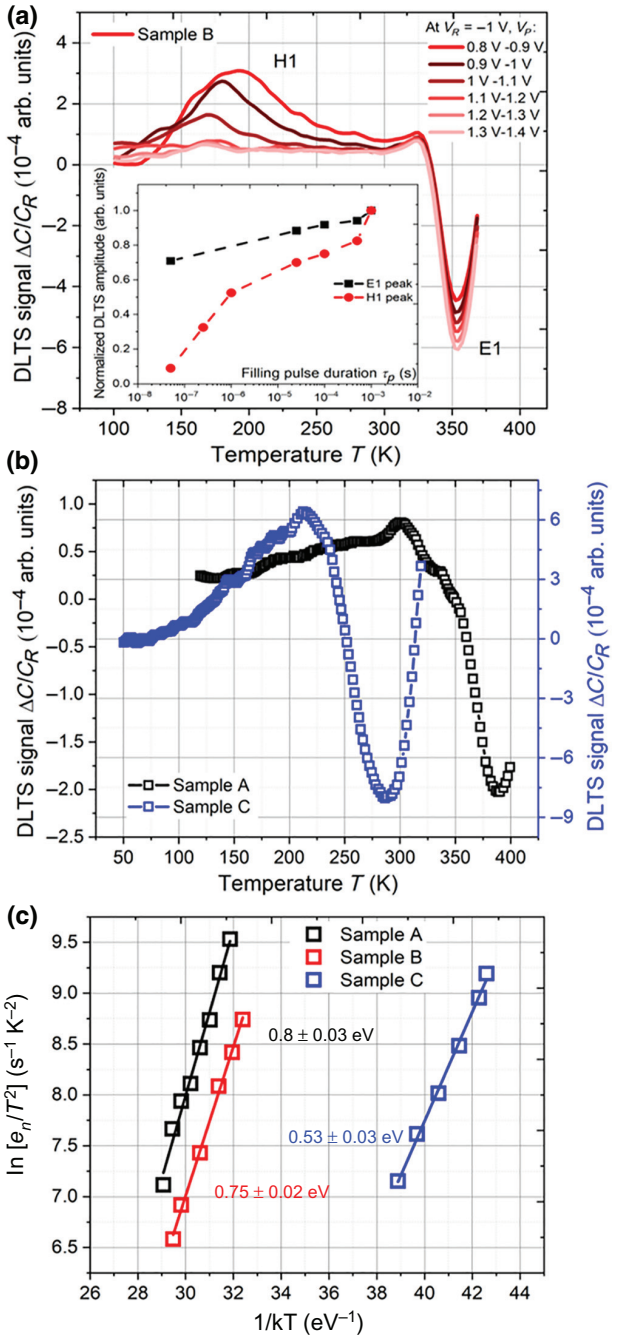

FIG. 4. (a) Double-DLTS spectrum for sample B with *in situ* passivation at reverse bias $V_R = -1$ V, the lock-in window $t_w = 51.2$ ms, pulse amplitude between $V_P = 0.8$–1.4 V, and pulse duration $t_p = 1$ ms. The lower inset shows dependence of the DLTS-peak shape of the E1 and H1 traps on the filling pulse time at 350 K for E1 and 180 K for H1. (b) DLTS spectrum for sample A at $V_R = -1$ V, $t_w = 100$ ms, $V_P = 1.4$ V, and $t_p = 1$ ms and sample C at $V_R = 0$ V, $t_w = 80$ ms, $V_P = 1$ V, $t_p = 1$ ms. (c) Arrhenius plot corresponding to EL2 and EL3 for GaAs diodes.

Defect structures and energy levels dedicated to substitutional O_{As} have also been shown by theoretical studies [63,66], which are associated with two donor levels

TABLE II. Summary of bulk-defectivity levels for GaAs *p-i-n* diodes.

	N_T, cm^{-3}	$(E_C - E_T)$, eV	Type
Sample A	$1.2 \pm 0.2 \times 10^{13}$	0.8 ± 0.03	EL2
Sample B with *in situ*	$2.8 \pm 0.5 \times 10^{14}$	0.75 ± 0.02	EL2
Sample B	$5.8 \pm 0.5 \times 10^{14}$	0.52 ± 0.02	EL3
Sample C with *ex situ*	$7.2 \pm 0.4 \times 10^{14}$	0.53 ± 0.03	EL3

at 0.57 eV (E_A) and 0.14 eV (E_B) below the conduction band [67]. In detail, the electron occupation is described as

$$\frac{dn_{\mathrm{EL2}}}{dT} = \frac{1}{a}\left(-A_{\mathrm{EL2}} + B_{\mathrm{EL2}}\right), \tag{8}$$

where $a = dT/dt$ is a constant heating rate, and A, B correspond to the transition rates of two-electron states. It has been suggested that during the excitation process all states of the O_{As} are occupied, but after the excitation the free carriers recombine at the ionized EL2$^+$ centers, and the other part of the excited carriers are captured in both energy levels $E_{A,B}$ of O_{As}. Samples B and C show an unidentified EL3 defect level, corresponding to the $E_C - 0.57$ eV two-electron level of O_{As}. As shown in Table II, samples B and C have a more than 20× higher point-defect density as compared to sample A.

The higher oxygen incorporation into the GaAs NRs and the increased point-defect densities of samples B and C in comparison to the planar diode can be related to the selective area growth of the NRs on top of an oxide pattern. In addition, the III-V material is in contact with SiO_2 side walls. The larger III-V/SiO_2 contact area of sample C versus sample B during growth can also explain the higher bulk-defect density in Table II. Further epitaxial growth experiments are needed to explore the origin of the higher bulk-defect density, also considering a possible impact of the NR ends on the electrical response.

Leakage current strongly depends on the energy level $(E_C - E_T)$ and concentration, N_T of the point defects [52]. In order to estimate the impact of these parameters on I_{bulk}, SRH GR model is used. The leakage current due to bulk defects, with energy level E_T in the band gap, is given by [52]

$$I_{\mathrm{def}} = \frac{qn_i(x,T)\sigma_{n,p}\nu_{n,p}}{\exp\left(\dfrac{|E_T(x) - E_i(x)|}{k_B T}\right)} N_T, \tag{9}$$

where $\nu_{n,p}$ is the thermal velocity for electrons (n) and holes (p), respectively, $\sigma_{n,p}$ is (minority carrier) capture cross section (in cm^{-2}), E_i is the intrinsic energy level, and n_i is the intrinsic carrier concentration. The leakage current for GaAs *p-i-n* diodes calculated using E_T and N_T, extracted from DLTS, is shown in Fig. 5. The difference between the measured and calculated currents shows that an additional leakage mechanism exists, for example, current through surface states, which also contributes to the leakage.

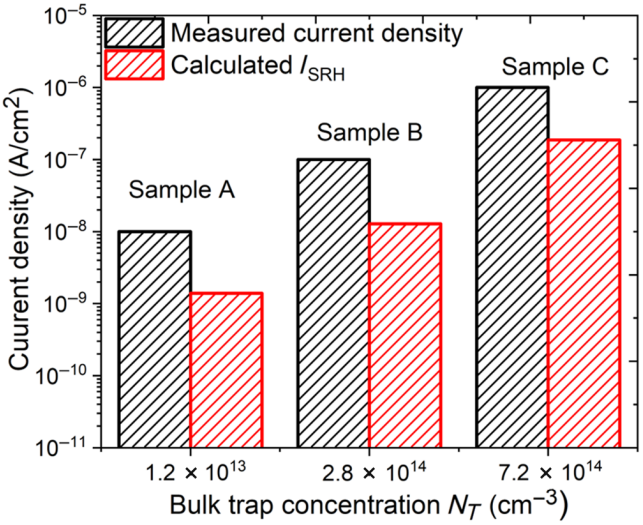

FIG. 5. Comparison of the leakage current due to bulk defects calculated using Eq. (9) with measured current extracted at −1 V.

C. Surface-state density

Several authors have reported the trap level with activation energy around $E_g/2$ for *n*-GaAs MOS structures to be related to Fermi-level pinning at the GaAs/oxide interface [68–70]. This indicates the presence of dangling bonds at the GaAs surface. The mesa side wall of the GaAs *p-i-n* diode also represents such a surface. As these density of states can act as strong generation-recombination centers, they play an important role in the dark current and ideality factor of *p-i-n* diodes.

In contrast to the point defects, the DLTS spectrum of DOS shows a broader peak and corresponding temperature peak shifts with V_P variation as discussed in Sec. II B.

Figure 6 shows the DLTS spectrum of the reference planar diode (sample A) and NR-based diode (sample B). In all spectra, the low-temperature signals appear around 180–200 K. From the shift in the peak, the change of the pulse voltage V_P, and the spatial localization at the interface, it is confirmed that the H1 peak belongs to surface states with $E_T - E_V = 0.4 \pm 0.03$ eV trap level with small capture cross section $\sigma_e \sim 1 \times 10^{-20}$ cm^2. The similar level is detected for sample B with and without *in situ* passivation, as shown in Fig. 6(b). The defect level thus obtained can be attributed to the dangling bonds created by Ga vacancies on the surface or additional impurities.

Using Eq. (6), the surface-state concentration and level for GaAs *p-i-n* diodes are calculated in Table III. The same H1 peak as observed for sample A, at

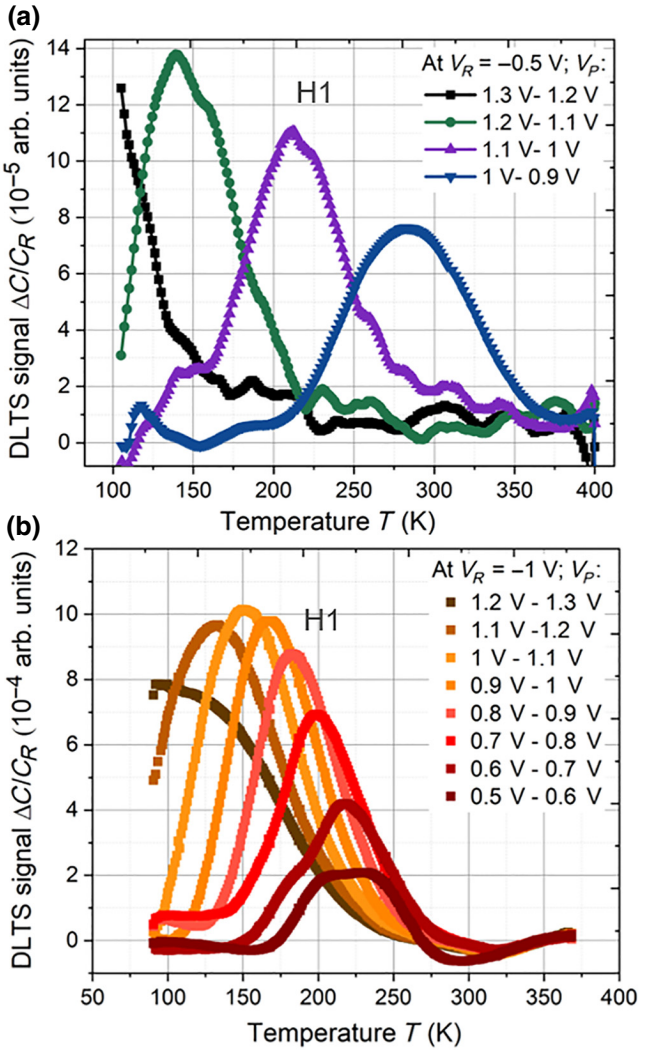

FIG. 6. Double-DLTS spectrum obtained with reverse bias $V_R = -0.5$ V in (a) and -1 V in (b), the lock-in window $t_w = 51.2$ ms and pulse duration $t_p = 1$ ms for sample A (a) and sample B (b).

$E_T - E_V = 0.41 \pm 0.02$ eV and $E_T - E_V = 0.58 \pm 0.03$ eV is detected for samples B and C, respectively. Based on the gate capacitance and transconductance measurements by Ozeki [71], the activation energy for n-GaAs/SiO_x has been reported around 0.62 eV, for n-GaAs/SiN_x is 0.44 eV and for n-GaAs/AlN_x is around 0.27eV. A theoretical model proposed by Jin [72] shows an explanation for $E_{act} = 0.4$–0.65 eV through the "band tail" concept and the steady-state surface potential distribution. In addition, sample C without any passivation, shows another defect level at $E_T - E_V = 1.1 \pm 0.04$ eV, which can be associated with Ga dangling bonds [68,73].

TABLE III. Summary of defectivity levels and concentration of N_{SS} for GaAs p-i-n diodes.

	N_{SS}, cm^{-2}	$(E_T - E_V)$, eV
Sample A	6.5×10^{12}	0.4 ± 0.03
Sample B	2.3×10^{13}	0.41 ± 0.02
Sample B with *in situ*	1.6×10^{13}	0.5 ± 0.05
Sample C	1.2×10^{14}	1.1 ± 0.04
Sample C with *ex situ*	2×10^{13}	0.58 ± 0.03

The surface-state density can also be extracted by using the perimeter component of total dark current, which is given by

$$J_{tot} = J_{bulk} + P/A \times J_{per}, \tag{10}$$

where P/A is the perimeter to area ratio of p-i-n diode, where $P = 2\pi R_{junc}$, $A = \pi R_{junc}^2$ for sample A, and R_{junc} varies from 37.5–150 μm. Regarding the nanoridge diodes, $P = 2 \times (W_{n^-} + L_{NR})$ and $A = W_{n^-} \times L_{NR}$. Based on TEM results, width of low-doped n layer, W_{n^-}, is around 0.6 μm and length of the nanoridge, L_{NR}, is 100 μm. The impact of surface states on J_{per} can be

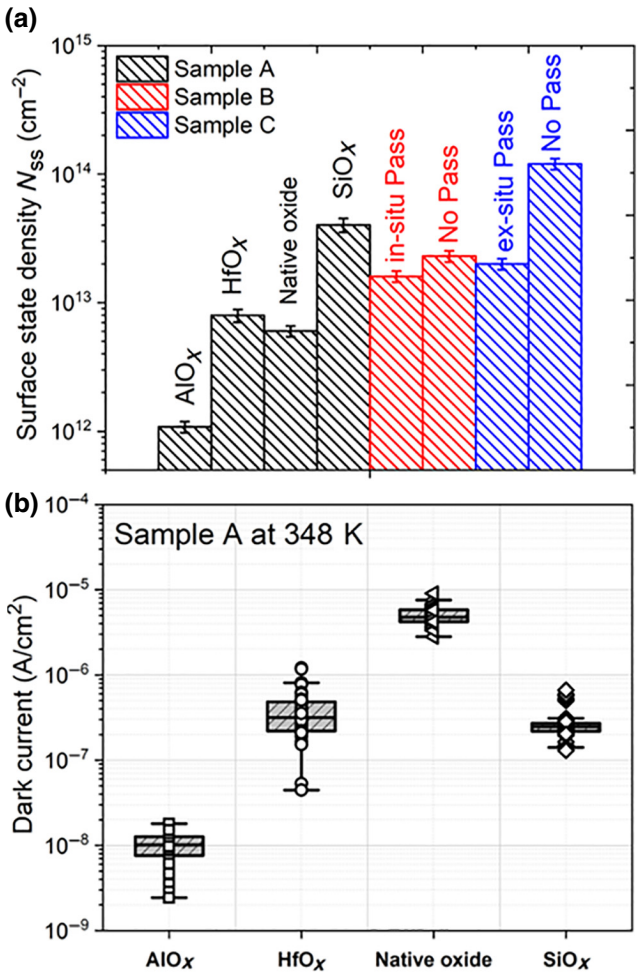

FIG. 7. Estimated DOS for GaAs p-i-n diodes (a) and leakage current dependency at 348 K for sample A at reverse bias -1 V.

expressed by [74]

$$J_{\text{per}} = qn_i\sigma_n v_n N_{\text{SS}} L_s \exp\left(\frac{eV}{2k_B T}\right), \tag{11}$$

where $L_s = f(E, T)$ is the surface diffusion length. Equation (11) requires extraction of J_{per} from the total dark current. As P/A ratio is fixed for samples B and C, this method can not be applied to NR diodes. Therefore, the N_{SS} extraction using J_{per} is done for sample A with different passivation layers shown in Fig. 7(a). The value of N_{SS} extracted using Eqs. (6) and (11) are found to be similar, further confirming the adequacy of the proposed methodology in Eq. (6).

Adding an $In_xGa_{1-x}P$ passivation layer to samples B and C leads to a decrease in N_{SS} to $1.6–2 \times 10^{13}$ cm^{-2} in comparison to NR diodes without passivation $N_{\text{SS}} \sim 10^{14}$ cm^{-2}. It is clear from Table III and Fig. 7(a) that both *in situ* and *ex situ* passivation can help in reducing surface states and, as a result, improve the device performance. A pronounced reduction in carrier recombination at the surface by adding an $In_xGa_{1-x}P$ passivation layer around a NR is also observed in time-resolved photoluminescence measurements [75].

Various surface treatments and/or passivation techniques such as sulfur treatment [76], SiN_x [77], HfO_x [78, 79], ALD AlO_x [30], and LaON [80] are investigated in order to reduce the surface-state concentration and Fermi-level pinning at the surface for GaAs.

In order to check the efficiency of some of the above-mentioned passivation techniques, several *ex situ* passivation layers are studied in this work on sample A. Figure 7(b) shows the impact of passivation on leakage current at bias voltage −1 V measured at 348 K.

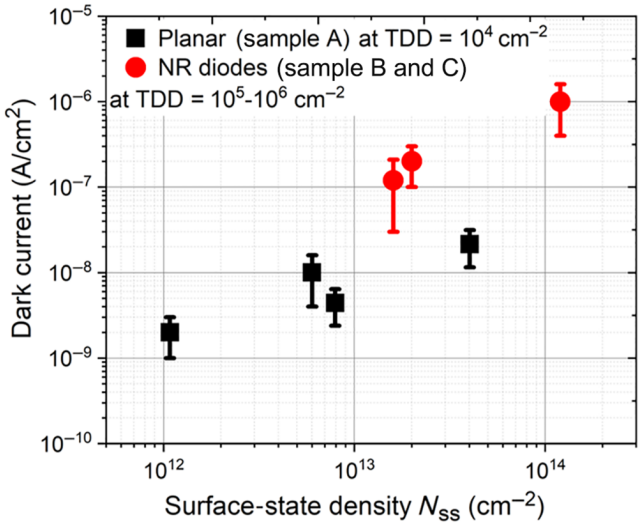

FIG. 8. Impact of N_{SS} and TDD on dark current for GaAs *p-i-n* diodes, extracted at −1 V.

As the leakage current for some samples is below the noise level of the measurement tool, *I-V* measurements are performed at higher temperatures. In general, all passivation layers seems to improve the dark current of the GaAs *p-i-n* diode. AlO_x, in particular, shows a significant positive impact on leakage current. The N_{SS} concentration extracted from *I-V* measurements confirms the above observation.

Figure 8 depicts the impact of surface states and TD density on the dark current measured in GaAs *p-i-n* diodes in this work. In general, a 10× reduction in N_{SS} leads to similar change in the dark current for the same TDD. Moreover, the above trend remains the same at different TDD. This also further signifies that for very low TDD, the surface states start to play a dominant role in the leakage current of GaAs *p-i-n* diodes. Based on leakage current and N_{SS} correlation, further research and development of side-wall passivation are necessary for NR technology.

IV. CONCLUSION

The electrical characterization of GaAs nanoridge *p-i-n* diodes, based on the recent technology of III-V on 300-mm Si, is reported. A methodology is developed, in order to analyse the defects present in the diode structures and it is used to extract the surface-state density and bulk traps from the DLTS spectrum. The defects, thus investigated, are used to establish their correlation with the device performance.

The NR material exhibits point defects introduced during the epitaxial growth (EL2, EL3) whose trap concentration and nature depend on the presence of oxygen indicating its dependence on the selective area growth of NR diodes on Si. Trap energy level and concentration of point defects have strong exponential and linear dependence on J_{bulk}, respectively, however this is not a dominant mechanism of the leakage for the presented *p-i-n* GaAs diodes. The difference between experimental and calculated dark current can be due to other mechanisms such as TAT and/or surface states.

Furthermore, the impact of surface passivation on N_{SS} and hence, on the leakage current is studied. It is found that passivation, in general, and AlO_x, in particular, provides a significant reduction of dark current, more than 2 orders of magnitude, for the GaAs *p-i-n* diode. In addition, an approximately linear correlation is observed between N_{SS} and dark current for the same TDD.

The defect analysis and methodology, presented in this work, are helpful in the development of more efficient and cost-effective III-V *p-i-n* diodes for future applications. This work demonstrates that through efficient bulk and surface engineering, III-V nanoridge devices monolithically integrated on Si substrates can perform as well as their planar counterparts.

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