Characterizing Quantum Devices at Scale with Custom Cryo-CMOS

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We make use of a custom-designed cryo-CMOS multiplexer to enable multiple quantum devices to be characterized in a single cooldown of a dilution refrigerator. Combined with a packaging approach that integrates cryo-CMOS chips and a hot-swappable parallel-device test platform, we describe how this setup takes the standard wiring configuration of a dilution refrigerator as input and expands the capability for batch characterization of quantum devices at milli-Kelvin temperatures and high magnetic fields. The architecture of the cryo-CMOS multiplexer is discussed, and its performance is benchmarked using few-electron quantum dots and Hall mobility mapping measurements.

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I. INTRODUCTION

Developing large-scale quantum machines brings new and distinct challenges not apparent in early demonstration experiments with single devices or few-qubit systems [1–3]. Although many fundamental scientific barriers stand in the path to scale up, significant progress is likely if engineering methodologies [4,5] can be leveraged to establish processes that reliably and repeatedly produce devices and subsystems with high-yield and deterministic performance. Key to such approaches is the ability to fabricate and characterize statistically significant numbers of devices, a major challenge when electrical measurements must be performed at milli-Kelvin temperatures in the presence of high magnetic fields.

Standard techniques for electrical test, such as the use of wafer-scale probe stations, are challenging to implement in the deep-cryogenic environment. These difficulties are not fundamental barriers but rather technical, for instance, the challenge of connecting room-temperature electronics to a large number of devices under test (DUT) below 1 K. A brute-force approach, in which each device is independently connected to test electronics via its own wiring, becomes problematic for large wire counts due to the thermal leak of the wiring itself [6], the footprint of bulky connectors, and the likelihood of failure that stems from using meters of cabling across large temperature gradients. Together these aspects usually lead to device characterization proceeding via serial cooldowns of a dilution refrigerator, with each cycle taking several days.

The need to perform high-throughput characterization and overcoming the challenge of multiple cooldowns has motivated previous work in realizing multiplexing devices and circuits. These include approaches that directly integrate the multiplexing switches into the quantum device as part of the same chip on which the qubit is formed [7–9]. Embedding the multiplexer in this way, however, increases the complexity of the design and fabrication process for quantum devices.

Here we describe a platform that decouples the quantum device and multiplexing circuit, fabricating a large number of multiplexer chips via tape out to a commercial CMOS foundry. This platform enables multiple quantum devices to be characterized in a single cooldown and with a standard cryostat wiring configuration. Our multiplexer (MUX) is based on commercial CMOS technology and specifically designed for operation below 100 mK. In the particular implementation reported here, 16 independent 1:5 MUX switches per die are configured by a room-temperature microcontroller. The switches are based on parallel NMOS and PMOS transistors connected

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in a transmission gate (TG) topology, allowing for full rail-to-rail voltage swing of both the inputs and outputs. Our design further allows *ad hoc* reconfiguration and daisy chaining of multiple MUX chips to suit particular device characterization needs.

Demonstrating both control of high-impedance bias lines and low-impedance transport measurements via the cryo-CMOS MUX, we tune a GaAs quantum dot to the few-electron regime and measure the Hall mobility across a 2″ InAs heterostructure wafer. By making many parallel mobility measurements in a single cooldown we are able to map the variation in mobility across a wafer, enabling fast feedback between the growth of materials and device performance, an advantage for realizing and optimizing topological quantum devices.

II. DEVICE DETAILS

A simplified schematic of a single cryo-CMOS MUX chip is shown in Fig. 1(a). The chips are fabricated on a 0.35-μm AMS CMOS process [10] and contain 16 1:5 analog multiplexing cells. The input of each 1:5 multiplexer can be connected to any of the five outputs or disconnected entirely. MUX chips are controlled by two power lines, V_{DD} and V_{SS}, which are set such that $V_{DD} - V_{SS} = 3.3$ V, and four control lines, shown on the left of Fig. 1(a). In each cell, the states of the switches are stored in a shift register, which is programmed by the Data In (D_I) and Clock In (CLK_I) pins. Following the programming of the 80 (16×5) switch states, the switches are updated in parallel when the Load (LD) pin is brought high. A global enable (EN) pin is also included which, when asserted, opens all the switches and places the chip in a shutdown state. Software control over the switching topology is provided by a microprocessor [11] located at room temperature. Crucially, as the switches are controlled via a shift register, chips may be chained together to increase the number of available MUX chips without a corresponding increase in the number of control lines that

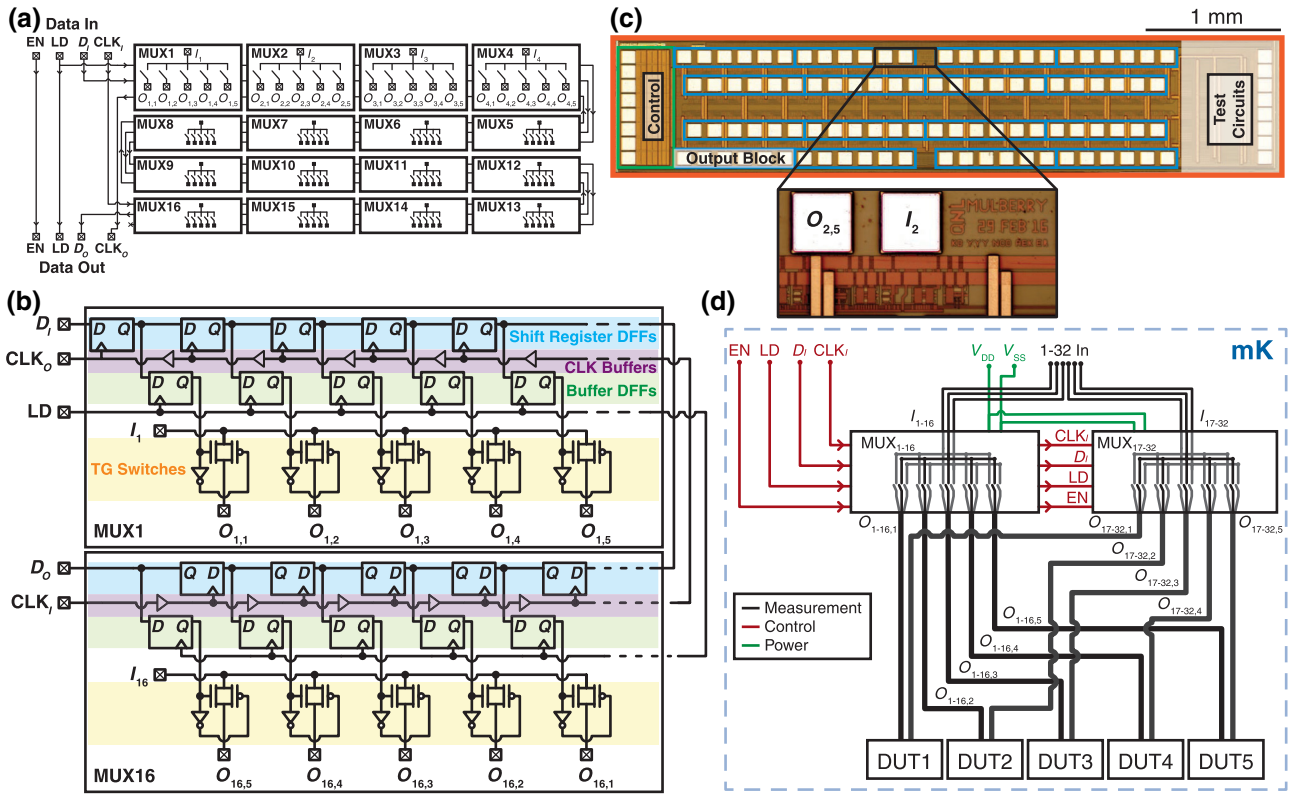

FIG. 1. (a) High-level schematic of our cryo-CMOS MUX chip. Each chip contains 16 1:5 MUX cells, each of which routes one analog input to five possible analog outputs. The switch states are controlled by a shift register that runs through each of the MUX cells in turn. Inputs and outputs are represented by crossed boxes. (b) Circuit block diagram of the first and last 1:5 multiplexing cell of the chip, showing the sequential wiring of logic signals through the chip. Analog inputs (I_N) and outputs ($O_{N,1..5}$) are shown connected to TG switches, which allow analog signals with voltages between the two power rails (V_{DD} and V_{SS}, not shown) to be multiplexed. (c) Die photo of the fabricated chip. Inset shows part of the core switching circuit with two 90×90 μm bond pads used to connect to the DUT. Test circuits on the right are used for process characterization and are not discussed in this paper. (d) A sample configuration of two MUX chips that expands the capability of the multiplexer to 32 1:5 MUX cells. Logic signals are passed through each chip in series, while the power supply is connected in parallel, thereby leaving the number of lines required to control the switches constant. In this way, five DUTs with up to 32 analog lines may be measured in a single cooldown.

must be routed down the fridge. This can be seen on the left side of Fig. 1(a), where the output connections of one chip are able to feed the input of the next chip directly [12].

A detailed circuit block diagram of the first and last MUX cell (cell 1 and cell 16, respectively) is shown in Fig. 1(b). The multiplexing switches (yellow) are of the TG topology, consisting of parallel NMOS and PMOS transistors of length 0.7 μm and width 40 μm and 120 μm, respectively. The TG switch structure allows for a maximum rail-to-rail input and output voltage swing of $V_{DD} - V_{SS} = 3.3$ V. For our initial characterization in Fig. 2, V_{DD} is set to 3.0 V and V_{SS} is set to 0 V, and are the MUX chip's high and low power supply, respectively. By appropriate choice of V_{DD} and V_{SS}, each of which may be set below 0 V, negative control voltages may be applied to the DUT, as shown in Fig. 3.

The choice of a TG switch over a single NMOS or PMOS transistor is motivated by the need to operate over the entire voltage supply range of the chip. A single transistor reduces the layout area and eliminates the need for complementary control signals, but limits the maximum output voltage swing to between V_{SS} and $V_{DD} - V_{th,n}$ if an NMOS transistor is used, or $V_{SS} + V_{th,p}$ and V_{DD} if a PMOS transistor is used, where $V_{th,n(p)}$ is the threshold voltage for NMOS (PMOS) transistors. In particular, for cryogenic applications, the output swing becomes even more limited as the devices are cooled, due to an increase in $V_{th,n(p)}$ as the intrinsic carrier density of the bulk, n_i, is exponentially dependent on temperature. n_i drops sharply at deep cryogenic temperatures (< 40 K) due to bandgap widening and bulk-carrier freeze out. This causes the bulk Fermi level to increase, resulting in an increase in $V_{th,n(p)}$ [13,14]. The shift in threshold voltage, $\Delta V_{th,n(p)}$ depends on n-doping (p-doping) concentration. For the 0.35-μm AMS process used for our devices, our measurements on transistor test structures indicate that $V_{th,n}$ increases from 0.5 to 0.75 V as the chip is cooled from room temperature to $T = 6$ K (similar to measurements reported in Ref. [15]). The shift in $V_{th,p}$ is more severe, rising from 0.8 V at 300 K to 1.35 V at 6 K. Crucially, the threshold voltage of PMOS devices in this process does not saturate at deep cryogenic temperatures but rather continues to increase as the temperature is lowered.

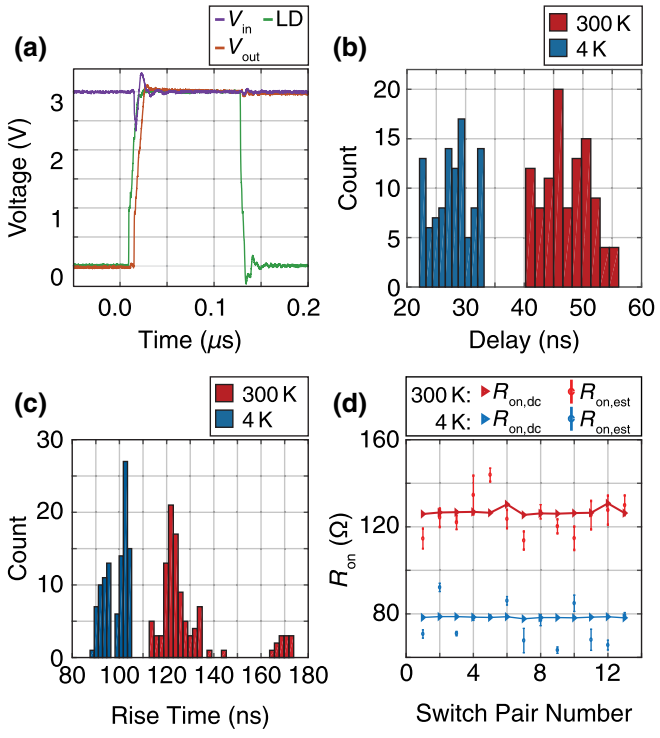

FIG. 2. Characterization of the performance of the MUX chip at $T = 300$ and 4 K. (a) Multiplexing at 4 K with a scope trace showing V_{out} connecting to $V_{in} = 3$ V when the MUX switch is turned on. (b) Delay and (c) rise time through the MUX switches at $T = 300$ and 4 K. (d) On-state resistance estimated from delay and rise time data, $R_{on,est}$, or measured directly using a lock-in amplifier, $R_{on,dc}$, at $T = 300$ and 4 K.

The shift register that forms the control interface consists of a series of edge-triggered D flip-flops (DFFs). The first row of DFFs is fed with serial data on pin D_I, either from room temperature or the D_O pin of another MUX chip, and is clocked by a buffered clock fed in on pin CLK_I [see blue regions of Fig. 1(b)]. A second row of DFFs (green) is used to buffer the switch controls allowing the new switch states to be sent without affecting the state of the outputs during configuration. Changes to the states of the switches take effect concurrently at the rising edge of an LD signal, which is fed directly to the clock input pins of the second row of DFFs. Due to the presence of long drive lines up and down the cryostat, and changes to the circuit performance as a function of temperature, it is imperative to improve the circuit's immunity to timing violation by design. Therefore, data is shifted from the left to the right of the DFF chain shown in the top of Fig. 1(b), whereas the clock is buffered between each flip-flop (purple) and passed through in the opposite direction. Though the cost of this design is extra logic gates and delay, propagating the data and clock signals from opposite directions guarantees proper logic operation because data always arrives before the rising edge of the clock. Further, the clocking events and subsequent logic changes in each flip-flop are slightly staggered. This disperses the sudden switching current from the power supply that would have otherwise occurred if all the DFFs are clocked simultaneously. This is a pragmatic design, driven by the unique challenges of cryogenic measurements that involve power supply or digital signals being fed from room-temperature instrumentation via meters of cables. In such setups, maintaining stringent delay matching and supply regulation can be difficult when compared to conventional room-temperature bench-top configurations.

The power consumption of the MUX chip is designed to be vanishingly small during static operation. In particular, as there are no dynamic elements such as an on-chip clock, power consumption is dominated by transistor leakage, which is negligible below 4 K. During the loading of the switch states, current draw is dominated by the charging capacitance of long wiring up and down the fridge. We note that the majority of this power is not dissipated at the mK stage of the cryostat, and as the MUX is designed to be operated at relatively slow speeds (up to a few kHz), the power dissipated on chip is below the threshold required to noticeably heat the cryostat. As such, during all measurements, the power consumed by the MUX chip is below the measurement resolution of our sources, and for each measurement presented below, did not affect the base temperature of the cryostat at any time, including during switching.

An optical micrograph of the die, shown in Fig. 1(c), highlights the key regions of the multiplexer. The power supply and digital control pins are placed on the left-hand side of the chip, and the multiplexing circuit and I/O pads are laid out in a symmetrical staggered arrangement taking up 3.1×0.8 mm of the core area. We note that the majority of this area is dominated by I/O pads, whose area may be further miniaturized through the use of high-density interconnect technologies such as flip-chip bonding [16]. Moving finally to the configuration of the multiplexer chip in a cryostat, we present a topology in Fig. 1(d) that chains two MUX chips together to allow the measurement of five devices under test simultaneously with up to 32 analog lines each. The power supplies are connected to each chip in parallel, while control signals are passed through each chip in turn. In a similar way, the setup of multiple MUX cells may be adapted for different measurement configurations [17]. For example, a single chip may yield a 1:80 multiplexer if all inputs are tied together. As the number of control lines is constant as more chips are added and given the negligible power consumption of a single chip, we note that the only limitations on the scaling are space restrictions within the cryostat.

The switches in the MUX chip are designed to drive both high-impedance bias lines, such as the bias gates of a quantum-dot device, as well as to probe transport phenomena through devices while maintaining a low on-state resistance ($< 200\ \Omega$, see Fig. S1 within the Supplemental Material [17]). The actual on-state resistance of the TG switch is a function of the applied drain-source voltage, V_{DS}, across the transistors. In steady-state operation, for both biasing and transport applications, the transistors in the on-state are expected to have a negligibly small $V_{DS} \ll 10$ mV, where they are designed to operate in the linear (Ohmic) region. Expanding on the source of this resistance, the on-state resistance (defined in the limit $V_{GS} - V_{th} \gg V_{DS}$, where V_{GS} is the gate-source voltage) of a single transistor can be expressed as

$$R_{on,n(p)}(T) \sim \frac{W}{\mu_{n(p)}(T) C_{ox} L [V_{GS} - V_{th,n(p)}(T)]}, \tag{1}$$

where $\mu_{n(p)}(T)$ is the carrier mobility for NMOS (PMOS) at temperature T, C_{ox} is the gate capacitance per unit area, and W and L are the transistor width and length. As the TG switch is a combination of an NMOS and PMOS transistor in parallel, the total switch resistance R_{on} is given by

$$R_{on}(T) = \frac{R_{on,n}(T) R_{on,p}(T)}{R_{on,n}(T) + R_{on,p}(T)}. \tag{2}$$

We note that as these parameters vary with the operating condition of the chip, the resistance through the device is expected to vary with supply voltage and temperature. Specifically, the competing effect of increasing V_{th} and μ with cooling causes $R_{on,n(p)}$ to vary [14,18] as the chip is cooled. Combining these two factors, the ratio γ of on resistance at $T = 300$ and 4 K for both NMOS and PMOS transistors operating in the Ohmic region can be expressed as

$$\gamma_n = \frac{\mu_n(300\ \mathrm{K})}{\mu_n(4\ \mathrm{K})} \times \frac{1}{1 - \frac{\Delta V_{th,n}}{V_{DD} - V_{in} - V_{th,n}(300\ \mathrm{K})}}, \tag{3}$$

$$\gamma_p = \frac{\mu_p(300\ \mathrm{K})}{\mu_p(4\ \mathrm{K})} \times \frac{1}{1 - \frac{\Delta V_{th,p}}{V_{in} - |V_{th,p}(300\ \mathrm{K})|}}, \tag{4}$$

where we define $\Delta V_{th,n(p)} = V_{th,n(p)}(4\ \mathrm{K}) - V_{th,n(p)}(300\ \mathrm{K})$. With cooling, the measured value of γ_p is 2.4, and γ_n is 4. Detailed measurements of transistor performance on this process were previously reported in Ref. [15]. As a result of lower μ together with higher V_{th} for the PMOS-type transistor compared to the NMOS-type transistor, the value of $R_{on,p}(4\ \mathrm{K})$ is much higher than $R_{on,n}(4\ \mathrm{K})$, however both decrease at low temperature. This effect is visible in the measured values of R_{on} for the switches in Fig. 2(d).

To experimentally verify the performance of the cryo-CMOS MUX chip at cryogenic temperatures, we wirebond the dies to a test printed circuit board (PCB) for measurement at $T = 300$ K and 4 K. The input and the first output of 13 of the 16 1:5 multiplexers are wirebonded through the cryostat to measure their performance. The supply voltages for the test are set to $V_{DD} = 3$ V and $V_{SS} = 0$ V, respectively. In addition, a pair of lines are shorted directly on the PCB and used to calibrate the fixed resistance and delay through the cryostat. A representative trace, showing the output voltage V_{out} being pulled high as the switch

is closed, is shown in Fig. 2(a). A slight delay between the LD pin being asserted and V_{out} being pulled high is visible, as well as a finite rise time, which is set by the resistance of the switch and capacitance of wiring through the fridge. Histograms of delay and rise time across multiple switches are shown in Figs. 2(b) and 2(c), respectively, at both 300 K (red), and 4 K (blue). A faster response is observed at 4 K, which we attribute to the reduction of R_{on}, leading to a faster switching time.

Finally, we measure the on-state resistance, R_{on}, of the switches in two ways. First, we directly measure the on-state resistance of the switches using conventional lock-in techniques with an 100-μV excitation through a pair of switches bonded together at the device. To find the individual switch resistance, $R_{on,dc}$, the previously calibrated resistance of the cryostat wiring is subtracted, and the result is divided by two. Second, we extract the on-state resistance from the measurement of rise time across the 13 pairs, using the measured cable capacitance and known impedance of the measurement equipment, which we denote $R_{on,est}$. The measured values across all switches are plotted in Fig. 2(d), with both techniques yielding values in good agreement with each other. At room temperature, the off-state resistance is measured to be above 10 TΩ at a 1-Hz excitation, limited by the switch capacitance of 37 fF [17]. At 4 K, the resistance is measured to be $>$ 1GΩ, limited by the noise of the measurement setup. To ensure the linearity of measurements, we note that the on-state resistance across the TG switch is measured to be constant up to 100 kHz [17], above which the capacitance of the switches begins to effect the measurement.

III. EXPERIMENTAL APPLICATIONS

A. Quantum dots

In order to determine the suitability of our multiplexer for quantum-device characterization, we connect it to the gates and Ohmic contacts of a quantum-dot device and perform transport measurements. A typical quantum-dot device has charging energies of around 100 μeV [19]. To form a well-defined quantum dot, the electrical noise and heat introduced by our proximal cryo-CMOS multiplexer must be negligible relative to the charging energy [20], thus quantum-dot measurements provide a means of determining the suitability of our MUX for interfacing with nanoscale quantum devices. The quantum-dot device is fabricated on an epitaxially grown GaAs/(Al,Ga)As heterostructure, which forms a 2DEG 91 nm below the surface. TiAu gates are patterned on the surface to define the dots, separated by a 10-nm HfO_2 dielectric. An optical micrograph of the setup is shown in Fig. 3(a), with the MUX chip highlighted in the red box and the quantum-dot device highlighted in the blue box. A false-color SEM of a similar device is shown in Fig. 3(b). The sample is mounted at the milli-Kelvin stage of a dilution refrigerator with a base temperature of 8 mK. Negative voltages are applied to the surface gates (gold) to create quantum dots (blue) containing a discrete number of electrons. The occupancy of each dot is denoted (N, M), where N (M) is the number of electrons on the left (right) quantum dot. Current is passed through the quantum dot via contacts to the 2DEG, O2, and O3, where current is only able to flow when there are available electron states in both the left and the right quantum dot. In order to allow negative bias voltages to be used, the MUX chip is operated with $V_{SS} = -2$ V and $V_{DD} = 1$ V.

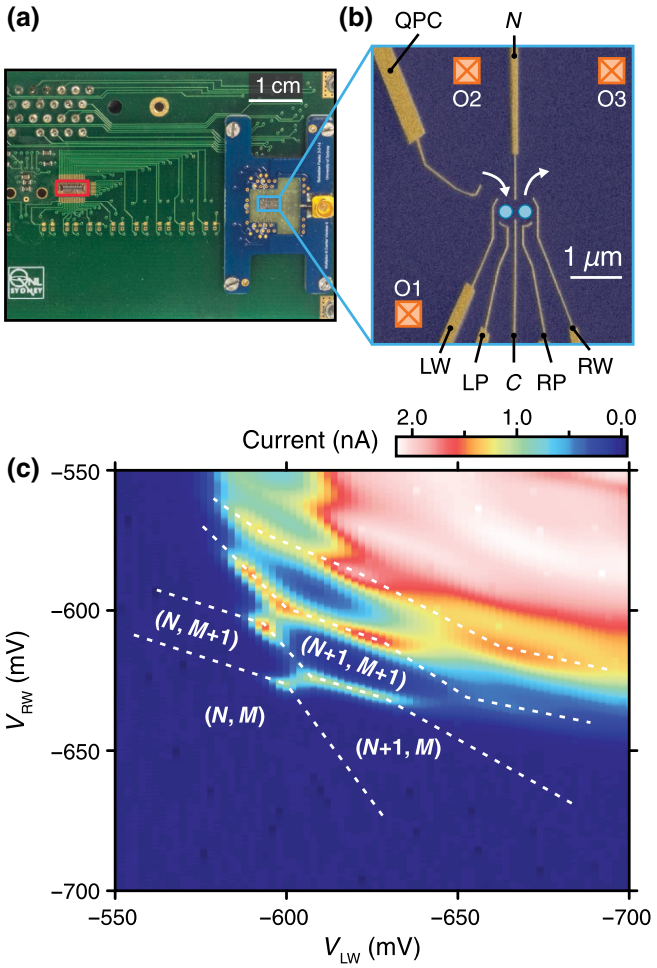

FIG. 3. (a) Photograph of the multiplexer characterization PCB showing the MUX chip (red), and a quantum dot, fabricated on a GaAs/(Al,Ga)As heterostructure, connected to filtered dc lines via the MUX chip (blue). (b) False-color SEM of an equivalent quantum-dot device. Ti/Au surface gates (gold) are used to define two quantum dots (blue). Locations of contacts to two-dimensional electron gas are indicated in orange boxes. (c) Charge stability diagram of the device showing the characteristic honeycomb pattern of a double quantum dot. White dashed lines indicate charge transitions and are a guide to the eye.

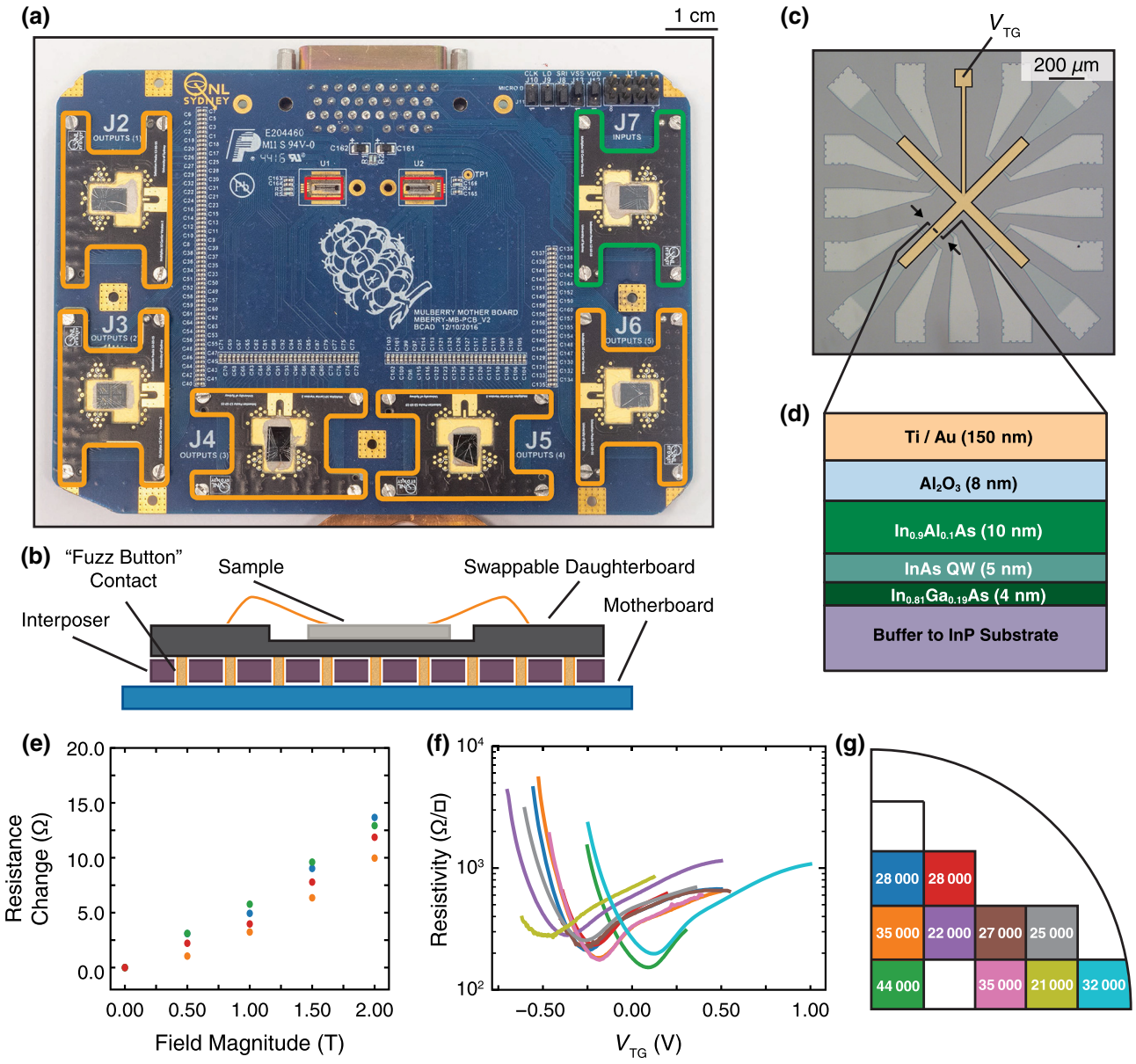

FIG. 4. (a) Photograph of multiplexed characterization PCB showing MUX dies (red) with five daughterboards (orange) allowing measurements, and an additional daughterboard (green), that has a connection to the fridge wiring bypassing the MUX chip. Cryo-CMOS MUX chips are wired in the configuration shown in Fig. 1(d). (b) Cross section of motherboard, interposer, and swappable daughterboard. (c) Optical micrograph of Hall bar device for characterizing mobility. A top gate (gold) allows for tuning of the carrier density in the device. (d) Cross section of measured InAs heterostructure. (e) Resistance of shorted MUX lines as a function of perpendicular magnetic field, measured across four separate pairs of switches. (f) Hall resistivity as a function of V_{TG} for $n = 9$ Hall bar devices, measured across two cooldowns. (g) Extracted mobility as a function of position on growth wafer.

In Fig. 3(c), the current through the quantum dot is shown, with both gates and Ohmic contacts routed through the cryo-CMOS MUX chip. Conventional lock-in techniques are used for current readout with an excitation voltage of 100 μV across the device. A honeycomb pattern characteristic of a double quantum dot is visible, with charge transitions indicated by dotted lines. Similar measurements are carried out for different gate configurations. In the steady state, we find the additional heat or noise generated by the MUX chip to be negligible, with the base temperature of the cryostat unaffected by the multiplexer.

B. Mobility characterization

Finally, we demonstrate the use of our cryo-CMOS MUX for performing batch material characterization of

InAs heterostructures, of interest for the purpose of realizing topological qubits [21]. Here we focus on determining how parameters such as the carrier mobility of the electron gas, a key metric for device performance [22], vary across a wafer as the process parameters are varied. To carry out batch-style measurements we develop a device packaging approach that allows many quantum devices to be bonded onto separate daughter PCBs [23] that are collectively mounted on a motherboard that also houses the cryo-CMOS MUX chips, as shown in Fig. 4(a). This setup allows the mounting of five dies in the dilution refrigerator, each containing four devices, in a single cooldown, with an additional sixth die configured such that its electrical connections bypass the MUX chip for verification purposes. The daughterboards are connected to the motherboard via an interposer, a cross section of which is shown in Fig. 4(b), which allows for samples to be rapidly interchanged in between cooldowns [23].

In our demonstration the heterostructure consists of an (In, Al)As/InAs/(In, Ga)As quantum well grown 10 nm below the surface on a 2″ (100) InP substrate [Figs. 4(c) and 4(d)]. An 8-nm layer of Al is deposited *in situ* to induce superconductivity in the quantum well via the proximity effect. Hall bar devices are defined across a quarter wafer of heterostructure, and the Al removed in the active area using standard wet-etching techniques. A global Al_2O_3 gate dielectric is then deposited with atomic layer deposition (ALD) with varying process parameters and treatments, followed by a Ti/Au top gate defined by e-beam lithography. Magnetoconductance measurements of the Hall bar are performed simultaneously as a function of top gate voltage in a perpendicular magnetic field using standard lock-in techniques in a dilution refrigerator with a base temperature of 9 mK. Figure 4(f) shows the extracted resistivity as a function of top gate voltage for nine samples, obtained across two cooldowns. No degradation in device performance is seen compared to devices measured without the cryo-CMOS MUX in line, and no change in base temperature between the MUX being powered on or off is observed. Using this technique, we can map out the mobility as a function of the processing of the die, as indicated in Fig. 4(g). We observe that dies coming from the edge of the wafer suffer a degradation of mobility by a factor of 2 [27 000 $cm^2/(V\ s)$] compared to dies near the center of the wafer [44 000 $cm^2/(V\ s)$]. A detailed analysis of the variation of process parameters on the mobility of the 2DEG is given in Ref. [24].

The magnetoconductance measurements also allow us to study the additional inline resistance that emerges as a function of magnetic field. As shown in Fig. 4(e), we observe an additional linear resistance of 6 ΩT^{-1} within the magnetic field range of −2 T to 2 T studied in this work. This resistance does not effect the accuracy of measurements, which are all made in a four-wire configuration.

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Note added.— Recently, a preprint describing similar work using commercial off-the-shelf CMOS multiplexing circuits has appeared [25].

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