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Vertical Transistors with Conductive-Network Electrodes: A Physical Image and What It Tells

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Vertical transistors with conductive-network electrodes composed of carbon- or metal-based nanowires or meshes are attractive because of their high current density, low operational voltage, and high degree of integration. However, the devices lack concise physical images to understand the operations and explicit design rules to achieve the necessary performance, such as sharp subthreshold swing and a large on:off ratio. Here, we develop a device theory with concise physical images, which are generally applicable for devices with organic or inorganic semiconductors. The simplified solution of Poisson's equation reveals that the electrostatic potential at the semiconductor-dielectric interface is controlled by both the gate and drain field, behaving like a plucked string. The spacing between electrodes and the capacitance ratio between semiconductors and dielectrics are critical for achieving strong gate tunability of the interfacial potential, and such gate tunability can be maximized to achieve a sharp turn-on property toward the Boltzmann limit in the subthreshold regime. Above the threshold, the conduction channels in devices with Schottky contacts can change from the "*L* type" to "*I* type", or vice versa, during scanning and the current-voltage relations can be well described by modifying classical transistor equations. The derived theories and equations agree well with the numerically simulated devices and reported experiments, revealing the physical images and providing explicit rules for designing, fabricating, and characterizing such transistors.

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I. INTRODUCTION

Vertical transistors based on semitransparent electrodes have been gaining increasing attention in recent years and several comprehensive reviews have been published [1–3]. The devices are built with electrodes from a conductive network comprising carbon nanotubes, graphene, metal nanowires, metal grids, and porous or permeable metal sheets. Differing from planar field-effect transistors (FETs) or thin-film transistors (TFTs), the conduction of the carriers in such devices occurs through vertical channels that are controlled by the gate field from the gaps between the nanowires or from the holes within the metal films [4,5]. Because of their submicron channel length, vertical transistors based on organic semiconductors (e.g., polymers or small molecules) with carbon-nanotube electrodes or metal meshes exhibit a large current density that can be used to drive light-emitting diodes [6–8]. The device structure also enables strong flexibility, in that mechanical bending will not terminate the large-area conduction channels, as shown in devices with oxide semiconductors ($InGaZnO_4$) and graphene-based electrodes [9]. The high degree of integration of such devices also allows for innovative structures and applications with various materials [10], for example, synaptic transistors with solid-state electrolytes [11] and highly sensitive photodetectors [12]. In addition, the layer-by-layer structure can be deposited by state-of-the-art printing technologies in industrial printing lines established for organic light-emitting diodes [13].

Despite encouraging progress, this type of vertical transistor still faces significant challenges in performance and lacks basic theories and clear physical images. The technical challenges primarily include difficulties in achieving sharp turn-on properties, a high on:off ratio, and saturation in the high drain voltage (V_D). For example, many studies have shown that during output scanning, that is, increasing the V_D with a fixed gate voltage (V_G), the current continuously increases superlinearly with V_D, and the output conductance continuously increases as well. Although there is a consensus on using wide-band-gap and high-mobility semiconductors [13], the mechanisms for device operation and device physics remain unclear and act as an important obstacle. Basic theory and a physical image of device operations are needed, and a simple description of the current-voltage relationship from sub- to above-threshold levels should be developed. The primary questions that need to be answered include the following: How is the

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electrostatic potential distributed? How is it controlled by the gate and drain field? How are the conduction channels formed during device operations? What are the factors that limit the turn-on properties in the subthreshold region? Could we describe the transfer and output characteristics with simple equations, as we do for planar FETs and TFTs?

To answer these questions, we explore device physics and develop device theories in this work. In the Sec. II, we briefly discuss the device concepts and main features of the conduction channels. Then, we solve the Poisson equation and obtain a simplified and explicit form of the electrostatic potential at the semiconductor-dielectric interface, which reveals key images of gate tuning and gives results that are highly consistent with the technology computer-aided design (TCAD) numerical simulations. In Sec. III, we investigate the mechanisms of device operation and the current-voltage relationships, including the sub- and above-threshold transfer and output characteristics, via theoretical derivations and numerical device simulators and compare them with the experimental results. Simplified current-voltage relationships are comparable with those used for FETs or TFTs. On the basis of the results, we further discuss how the key parameters affect the device performance and propose explicit rules for designing and fabricating the vertical transistors.

II. BASIC THEORY AND PHYSICAL IMAGES

A. Device concepts

Differing from planar FETs or TFTs with lateral channels between the semiconductor and dielectric films, the carriers injected in the vertical transistors follow the vertical channel, that is, directly from the source to the drain, and the side channel, that is, from the source along the semiconductor-dielectric interface and to the top drain electrode. We possess a general understanding of conduction channels based on the TCAD three-dimensional calculation platform (Fig. 1). The following main parameters are also illustrated: the width of cuboid electrodes is d_S; the spacing between electrodes is d_{gap}; the semiconductor layer thickness is t_{SC}; the insulator layer thickness is t_{ox}; and the injection barrier of the Schottky contacts is $q\varphi_b$, where q is the elementary charge and φ_b is the barrier height potential due to the difference between the work function of the electrodes and electron affinity of the n-type semiconductor (or valance band edge of the p-type semiconductor). In an Ohmic-contact device, the top channel is the primary conduction path [Figs. 1(a) and 1(c)] and is referred to as the "I-type" channel, according to the shape. In a Schottky-contact device, the large resistance on top of the source could exceed the sheet resistance at

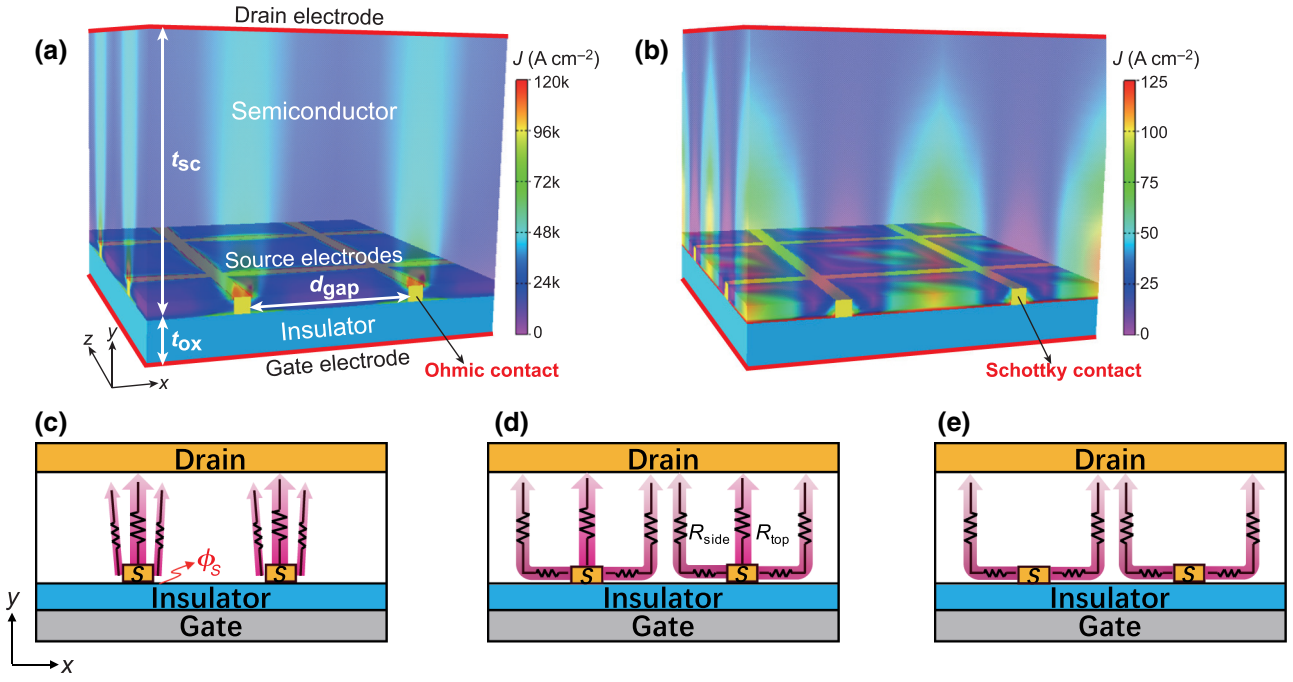

FIG. 1. Device concepts and channel positions. (a), (b) Three-dimensional simulated devices with contours of current density. Main device parameters are as follows: width of cuboid source electrodes is d_S (20 nm), spacing between electrodes is d_{gap} (200 nm), semiconductor layer thickness is t_{SC} (320 nm), insulator layer thickness is t_{ox} (50 nm), and energy offset between the work function of the electrodes and electron affinity of the semiconductor is $q\varphi_b$. Device in (a) has Ohmic contacts ($q\varphi_b = 0.0$ eV, $V_G = 1$ V, and $V_D = 10$ V), whereas that in (b) has Schottky contacts ($q\varphi_b = 0.4$ eV, $V_G = 20$ V, and $V_D = 1$ V). Current density unit is A cm^{-2}. (c)–(e) Schematic representations of the current distribution and resistances, which depend on the contact properties and operational modes.

the semiconductor-dielectric interface, and the main channel is formed with the latter [Figs. 1(b) and 1(e)], which is referred to as the "L-type" channel. The intermediate case is where both channels are contributing, which is referred to as the "LI-type" channel [Fig. 1(d)].

Such competition among the conduction paths is similar to the nonhomogeneous current distribution near the contact areas in staggered FETs or TFTs (the "current crowding effect") [14], wherein the effective injection area under the source electrode is expanded as the sheet resistance at the semiconductor-dielectric interface decreases. Importantly, during device operation, the transition of channel types can also occur because of changes in the local resistivity. The resistances are denoted as $R_{\rm top}$ and $R_{\rm side}$, as illustrated in Fig. 1(d). If $R_{\rm side}$ decreases to become much smaller than that of $R_{\rm top}$, conduction is mainly dominated by the L-type channel. When the opposite occurs, the channel changes from L type to I type. Details are discussed in the following sections. For simplicity, we use a two-dimensional (2D) simulated device in the x-y plane in the following studies. The following discussion is based on n-channel devices for convenience, but the results are also applicable to p-channel devices.

B. Electrostatic potential

The electrostatic potential determines the carrier density by the Poisson equation, the electric field by gradient, and the current by the continuity equation. In this section, the potential along the semiconductor-dielectric interface is first discussed with dispersed source electrodes (i.e., $d_{\rm gap}$ is large) and then with dense electrodes (i.e., $d_{\rm gap}$ is small). Then, the vertical screening effect in the 2D plane is briefly discussed.

1. Interfacial potential

Regarding the semiconductor-dielectric interface ($y=0$), the potential at position x, denoted as $\phi_s(x)$, is schematically shown in Fig. 2(a). This potential satisfies Poisson's equation:

$$\frac{d^2\phi_s(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_{\rm SC}}, \tag{1}$$

where ρ is the space-charge density and $\rho = q(p - n + N_D^+ - N_A^-)$ in the absence of trapping sites; p and n are the hole and electron density, respectively; N_A^- and N_D^+ are the density of ionized acceptors and donors (if any), respectively; and $\varepsilon_{\rm SC}$ is the permittivity of the semiconductor. The hole and electron density in the semiconductor bulk at thermal equilibrium are p_0 and n_0, respectively. Due to the electrically neutral condition, intrinsic semiconductors feature $p_0 = n_0$ and ionized extrinsic semiconductors feature $p_0 + N_D^+ = n_0 + N_A^-$. With the Boltzmann approximation, the electron density is related to the potential by $n = n_0 \exp[(q\phi_s - q\phi_{\rm BI})/kT] = n_S \exp(q\phi_s/kT)$, where $\phi_{\rm BI}$ is the built-in potential induced by the source electrodes, n_S is the electron density at the source interface ($x=0$), k is the Boltzmann constant, and T is the absolute temperature. The value of $\phi_{\rm BI}$ is ideally $\phi_{\rm BI} = \varphi_b - (E_c - E_F)/q$, where φ_b is the apparent injection barrier potential and E_c and E_F are the conduction-band minimum energy and Fermi energy of the semiconductor, respectively. If the Schottky barrier lowering effect is significant, the effective barrier height, $q\varphi_{b,\rm eff}$, which is smaller than that of $q\varphi_b$, is used instead to calculate $\phi_{\rm BI}$. In this study, $\varphi_{b,\rm eff}$ is used in TCAD simulations, but a constant injection barrier is used in the calculations discussed below for simplicity. The hole density is in a similar form, but with $-q(\phi_s - \phi_{\rm BI})$.

2. With dispersed network

When the gaps between source electrodes are wide, the coupling of fields is ignored. The precise solution of Poisson's equation is usually in an implicit and complicated form [15,16] and, to focus on the physical images, we derive an approximated and simplified solution. We use the first-order Taylor expansion for the approximation $\exp(\pm \Delta E/kT) \cong 1 \pm \Delta E/kT$ for Eq. (1), where ΔE is a small energy. ϕ_{s0} is the potential at $x=0$ and $\phi_{s\infty}$ is the potential at infinite distance (relative to ϕ_{s0}, when $V_S = 0$). As the charge-carrier density n is related to the local potential ϕ_s via the Boltzmann distribution, ϕ_s should be chosen such that $n(\phi_{s0}) = n_S$ at $x = 0$ (source interface) and $n(\phi_{s\infty}) = n_0$ at $x = \infty$ (far from the source). Then, the simplified solution to Poisson's equation is

$$\phi_s(x) = \phi_{s\infty} + (\phi_{s0} - \phi_{s\infty}) \exp\left(-\frac{x}{L_D}\right), \tag{2}$$

where L_D is the characteristic Debye length $L_D = \sqrt{\varepsilon_{\rm SC}kT/[q^2(n_0 + p_0)]}$ and, here, we take n-type semiconductors as examples, so that $L_D = \sqrt{\varepsilon_{\rm SC}kT/(q^2 n_0)}$. These equations are suitable for both the intrinsic and ionized extrinsic semiconductors. The value of $\phi_{s\infty}$ at zero V_D and V_G is $\phi_{\rm BI}$. To determine $\phi_{s\infty}$ at nonzero V_D and V_G, we consider the vertical boundary condition at the interface for Poisson's equation. Far from the source ($x=\infty$), the electric field ϵ in the y direction is estimated via linear approximation, i.e., $\epsilon = (V_D - \phi_{s\infty})/t_{\rm SC}$ at the semiconductor side and $\epsilon = (\phi_{s\infty} - V_G)/t_{\rm ox}$ at the dielectric side, and the fields satisfy Poisson's equation at the boundary. Then, in the absence of surface states, we have

$$\phi_{s\infty} = \phi_{\rm BI} + \left(1 + \frac{C_{\rm ox}}{C_{\rm SC}}\right)^{-1} V_D + \left(1 + \frac{C_{\rm SC}}{C_{\rm ox}}\right)^{-1} V_G, \tag{3}$$

where the capacitances per unit area are $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$ for the insulating oxide layer ($\varepsilon_{\rm ox}$ is permittivity) and

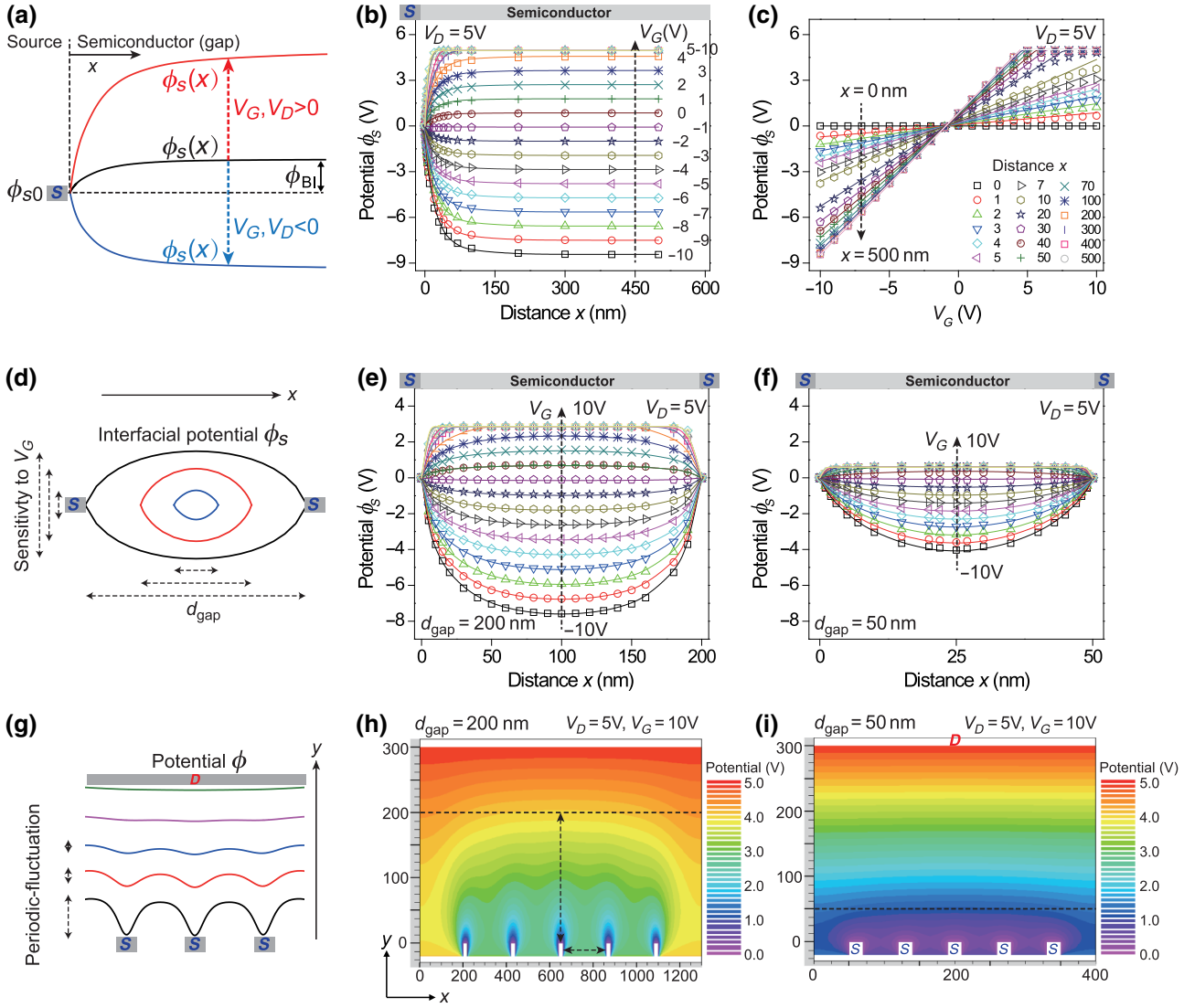

FIG. 2. Potential distribution. (a)−(c) Interfacial potential ϕ_s near single-source electrode: (a) scheme showing $\phi_s(x)$ at zero V_G and V_D (black), positive V_G or V_D (red), and negative V_G or V_D (blue); (b) $\phi_s(x)$ as a function of x for various V_G [dots are TCAD-simulated, and the curves are fitted by Eq. (4), the same below]; (c) ϕ_s as a function of V_G for various x. ϕ_{s0} is the reference point. (d)–(f) ϕ_s between neighboring electrodes: (d) scheme showing regulating ϕ_s by V_G; the capacity for regulation (or sensitivity) decreases when d_{gap} decreases. (e),(f) ϕ_s in a device with d_{gap}= 200 or 50 nm [dots are TCAD-simulated and curves are fitting by Eq. (6)]. (g)–(i) 2D distribution of potential ϕ: (g) scheme showing potential distribution in the vertical direction; (h),(i) TCAD-simulated 2D distribution of potential of the semiconductor layer in a device with d_{gap}= 200 or 50 nm (5 source electrodes). Dashed lines label the position with a distance of d_{gap} from the top of the source. Parameters of the TCAD-simulated device are $q\varphi_b = 0.4$ eV, t_{ox}= 10 nm, and t_{SC}= 320 nm.

$C_{SC} = \varepsilon_{SC}/t_{SC}$ for the semiconductor layer. Substitute Eq. (3) into Eq. (2) and we find

$$\phi_s(x) = \phi_{s0} + \left[\phi_{BI} - \phi_{s0} + \left(1 + \frac{C_{ox}}{C_{SC}}\right)^{-1} V_D + \left(1 + \frac{C_{SC}}{C_{ox}}\right)^{-1} V_G\right]\left[1 - \exp\left(-\frac{x}{L_D}\right)\right]. \quad (4)$$

The interfacial potential described by Eq. (4) is applicable when the semiconductor-dielectric interface is in depletion ($V_G < 0$) or even in some cases of accumulation when $V_G < V_D$, wherein the linear approximation of potential in the vertical direction is valid. When V_G increases beyond V_D, ϕ_s varies nonlinearly with V_G and has the upper limit $\phi_{s,max}$, which is close to V_D. Because using the first-order Taylor expansion provides a decay speed faster than that of the precise solution, we use the stretched exponential form $(x/L_D)^{\kappa}$ ($\kappa < 1$) instead of (x/L_D) in Eq. (4) to better describe the practical devices (the same below). The potential distributions obtained from the 2D TCAD numerical simulations for a Schottky-contact device ($q\varphi_b = 0.4$ eV

and $V_D = 5$ V) as a function of x and V_G are shown in Figs. 2(b) and 2(c) (dots). By using only a single set of parameters ($L_D = 23$ nm, $\kappa = 0.8$, $\phi_{s,\max} = 5$ V), we find that the potential distributions described above are a good fit for all x and V_G values below that of V_D, as shown in Figs. 2(b) and 2(c) (curves). The good agreement verifies the above derivations, despite their simple forms.

3. With dense network

Because narrow gaps are present between neighboring source electrodes, we consider the coupling between the electric fields from neighboring electrodes. The interfacial potential is approximated as the sum of the potentials generated by the neighboring electrodes:

$$\phi_s(x) = \phi_{s1} + (\phi_{s0} - \phi_{s\infty}) \times \left[\exp\left(-\frac{x}{L_D}\right) + \exp\left(-\frac{d_{\text{gap}} - x}{L_D}\right)\right], \quad (5)$$

where $x < d_{\text{gap}}$ and $\phi_{s1} = \phi_{s\infty} - (\phi_{s0} - \phi_{s\infty})\exp(-d_{\text{gap}}/L_D)$, which is determined by using the boundary conditions. Then, the potential with a small or large d_{gap} can be expressed in a single form [covering Eqs. (4) and (5)]:

$$\phi_s(x) = \phi_{s0} + \left[\phi_{\text{BI}} - \phi_{s0} + \left(1 + \frac{C_{\text{ox}}}{C_{\text{SC}}}\right)^{-1} V_D + \left(1 + \frac{C_{\text{SC}}}{C_{\text{ox}}}\right)^{-1} V_G\right] \eta(x). \quad (6a)$$

The physical meaning of $\eta(x)$ is the ratio (between 0 and 1) of the relative change in potential, i.e., $\eta(x) = [\phi_s(x) - \phi_{s0}]/(\phi_{s\infty} - \phi_{s0})$, and it is

$$\eta(x) = \begin{cases} 1 - \exp\left(-\frac{x}{L_D}\right), & \text{if} \quad d_{\text{gap}} \gg L_D \\ 1 - \exp\left(-\frac{x}{L_D}\right) - \left[\exp\left(-\frac{d_{\text{gap}} - x}{L_D}\right) - \exp\left(-\frac{d_{\text{gap}}}{L_D}\right)\right], & \text{if} \quad d_{\text{gap}} \sim L_D. \end{cases} \quad (6b)$$

The latter form of η becomes the same as the former when $d_{\text{gap}} \gg L_D$. Additionally, the upper limit of ϕ_s becomes smaller than that of V_D as the potential is pulled toward the source potential.

According to Eq. (6), the profile of ϕ_s is controlled by the gate or drain field, as illustrated in Fig. 2(d), like a plucked string. The capacity of regulating ϕ_s by V_G or V_D or, in other words, the sensitivity of ϕ_s to V_G or V_D, is reduced when d_{gap} decreases. The theoretical results are found to be highly consistent with the 2D TCAD numerical simulations [Figs. 2(e) and 2(f), dots], as Eq. (6) well fits the data [Figs. 2(e) and 2(f), curves]. Again, $(x/L_D)^{\kappa}$ ($\kappa < 1$) is used instead of (x/L_D) and the fitting parameters are $L_D = 21.5$ nm, $\kappa = 0.75$, and $\phi_{s,\max} = 2.9$ V, when $d_{\text{gap}} = 200$ nm, and $L_D = 22.3$ nm, $\kappa = 0.8$, and $\phi_{s,\max} = 0.6$ V, when $d_{\text{gap}} = 50$ nm. The dependence of $\phi_s(x)$ on V_G or V_D is derived from Eq. (6):

$$\frac{\partial \phi_s(x)}{\partial V_G} = \left(1 + \frac{C_{\text{SC}}}{C_{\text{ox}}}\right)^{-1} \eta(x), \quad (7a)$$

$$\frac{\partial \phi_s(x)}{\partial V_D} = \left(1 + \frac{C_{\text{ox}}}{C_{\text{SC}}}\right)^{-1} \eta(x). \quad (7b)$$

The clues for device operation are given by Eq. (7) and are as follows: (1) the interfacial potential ϕ_s can be tuned by both V_G and V_D; (2) ϕ_s is much more sensitive to V_G if $C_{\text{ox}} \gg C_{\text{SC}}$ and more sensitive to V_D if $C_{\text{ox}} \ll C_{\text{SC}}$; (3) reducing t_{ox} or increasing t_{SC} noticeably increases the gate tunability of ϕ_s, as it is controlled by V_G with a ratio of $[1 + (t_{\text{ox}}/t_{\text{SC}})(\varepsilon_{\text{SC}}/\varepsilon_{\text{ox}})]^{-1}$; and (4) reducing d_{gap} changes the potential ϕ_s in roughly an exponentially decaying manner toward the source potential and, thus, remarkably weakens the gate tunability for switching.

4. Potential in the vertical direction

For electrodes composed of a conductive network, an important issue is the screening effect and the question is as follows: In the vertical direction, how far does the fluctuation of the field due to periodic source electrodes extend into the semiconductor layer? This is also related to the gate-tuning capacity inside the semiconductor. Because electrodes are periodic, the potentials in the bulk of a semiconductor should also be periodic and, by referring to the Feynman method on conductive grids [17], they can be expressed as a Fourier series

$$\phi(x, y) = \sum_{m=1}^{\infty} f_m(y) \cos\frac{2\pi m x}{d_{\text{gap}}}, \quad (8)$$

where m serves as a summation index. Using the case of a static electric field as an example, the above potential satisfies Poisson's equation without charges, and $f_m(y) = A_m \exp(-2\pi m y/d_{\text{gap}})$, where A_m is the coefficient for each harmonic term. For the first order of the harmonic term, the value decays exponentially with a characteristic length of d_{gap} (higher orders of harmonic terms decay faster). Therefore, outside the distance of d_{gap} in the y direction, the periodic fluctuation of the potential from the conductive network becomes negligible, and the potential is almost uniform in the x direction. This is illustrated in Fig. 2(g). Although derived from a highly simplified scenario, the results agree well with the numerical calculations of a vertical transistor, as shown in Figs. 2(h) and 2(i), wherein the potential beyond the distance of d_{gap} above the semiconductor-dielectric interface is almost uniform in the x direction.

The above theories give a simplified and explicit form of ϕ, in particular, of ϕ_s, which helps to clarify the key

physical image of the device operation and understand the current-voltage relations, as discussed below.

III. DEVICE OPERATION

In this section, we study the band diagrams, distribution of carrier densities, and currents before discussing the current-voltage (I-V) characteristics. We use devices with Schottky contacts as the primary examples because they are commonly fabricated in experiments, and we also mention Ohmic-contact devices in the following. For the 2D TCAD numerical simulations, Poisson's equation and drift-diffusion equations are solved, and the Schottky barrier lowering effect is also involved. The electrodes have a width of $d_S = 20$ nm and the same thickness. For the semiconductor, the carrier mobility of the electrons is $10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, the band gap is 3.3 eV, and the effective density of states for the conduction band is $5 \times 10^{20}\ \mathrm{cm^{-3}}$. The relative dielectric constant (k) of the insulator and semiconductor is set at 3.9 and 9, respectively. The film thickness is 10 nm for the insulator and 320 nm for the semiconductor to enable strong gate control. The dielectric constant is a commonly used value for oxide semiconductors and, for organic semiconductors with lower k values (3–4), thinner semiconducting films can be used to obtain the same V_G tunability. See the Supplemental Material [18] for more details of simulations. For simplicity, the semiconductor-dielectric interface is assumed to be defect-free, unless stated otherwise.

A. Tuning by gate and drain fields

1. Bending of energy bands

The TCAD-simulated band diagrams along the two arrows in Fig. 2(h) are shown in Figs. 3(a)–3(d). The main

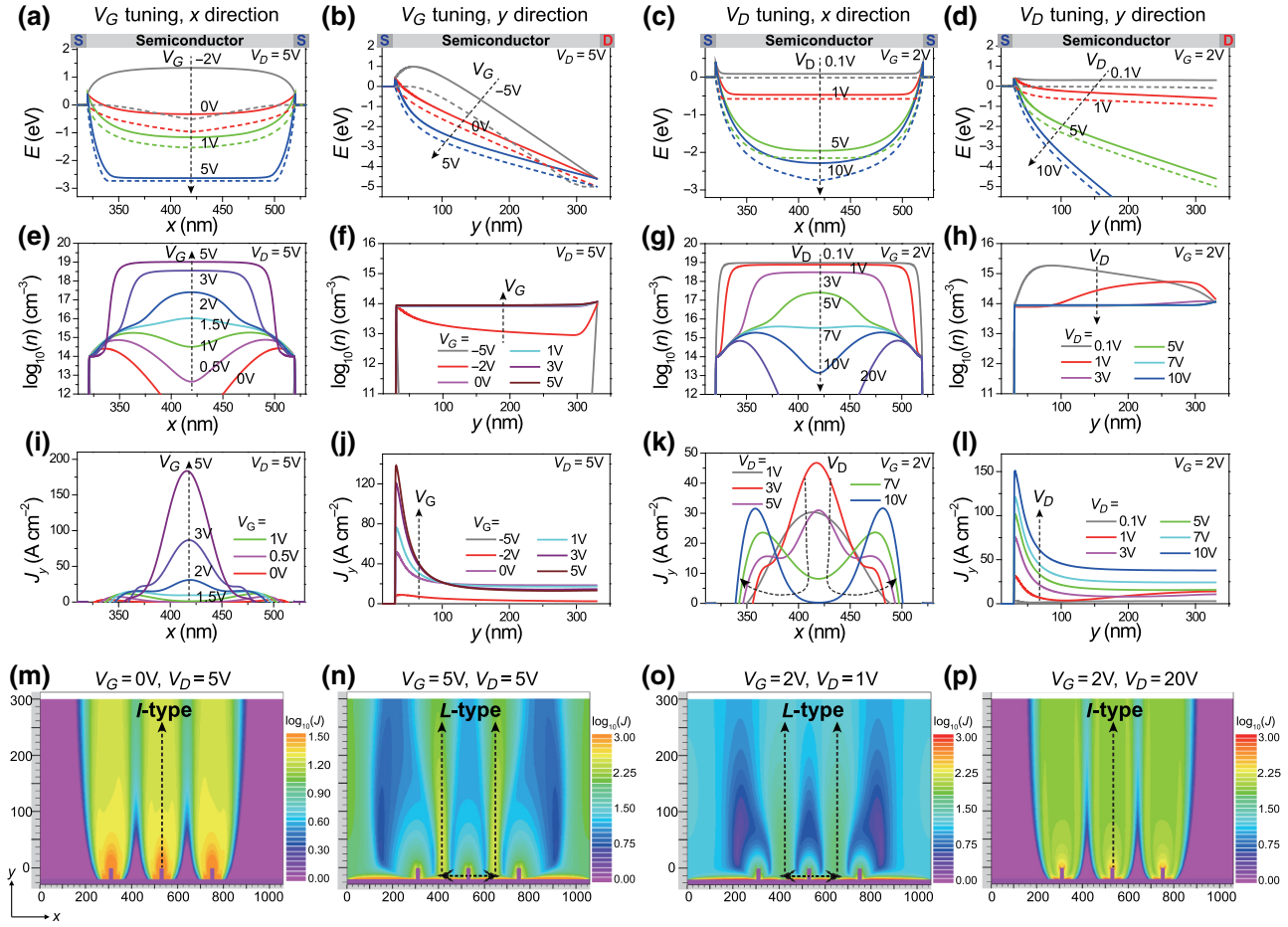

FIG. 3. Band bending, carrier density, and channel formation. TCAD-simulated results along the two arrows in Fig. 2(g), i.e., at the semiconductor-dielectric interface between two source electrodes (x direction) and from one source to the drain electrode (y direction). For V_G tuning, the energy levels of E_c and E_{Fn} are shown in (a) and (b) with solid and dashed curves, respectively. Carrier density n is shown in (e),(f), and the vertical component of current density J_y is shown in (i), (j). For V_D tuning, the energy levels, n, and J_y are shown in (c), (d), (g), (h), (k), and (l). (m)–(p) 2D $\log_{10}$-scaled current distribution in devices (3 sources) during transfer scanning (m),(n) or output scanning (o),(p). Parameters of the TCAD-simulated device are $q\varphi_b = 0.4$ eV, $t_{\mathrm{ox}} = 10$ nm, $t_{\mathrm{SC}} = 320$ nm, and $d_{\mathrm{gap}} = 200$ nm.

features of V_G tuning, i.e., increasing V_G with a fixed V_D, are as follows: (1) between two source electrodes and at the dielectric surface [x direction, Fig. 3(a)] the energy bands are strongly lowered with a reduction in the difference between E_c (solid curves) and the quasi-Fermi energy for the electrons (E_{Fn}, dashed curves), causing an accumulation region in the gap. Additionally, a flat band appears in the gap center when V_G approaches and exceeds V_D because ϕ_s starts to gradually approach its upper limit (i.e., lower limit of electron energy), as stated above; and (2) from the source to the drain [y direction, Fig. 3(b)], the energy bands between electrodes are modified to a much smaller extent, increasing the local electric field near the source.

The main features of V_D tuning, i.e., increasing V_D with a fixed V_G, are as follows: (1) between two source electrodes and at the dielectric surface [x direction, Fig. 3(c)] the energy bands are lowered with an enlarged difference between E_c and E_{Fn}, causing a depletion region in the gap because ϕ_s is raised by V_D and gradually approaches the value of V_G; and (2) from the source to the drain [y direction, Fig. 3(d)], the energy bands between electrodes are strongly lowered toward lower electron energies, enhancing the electric field. The increased downward bending is a natural consequence of the fact that the applied source-drain voltage has to fully drop along the y direction.

2. Evolution of carrier and current distributions

The corresponding modulations of the electron density, n, and vertical component of current density, J_y, between neighboring source electrodes (x direction) and from the source to the drain (y direction) are shown in Figs. 3(e)–3(h) and 3(i)–3(l), respectively. For transfer scanning (increasing V_G with a fixed V_D), the features are as follows: (1) at the dielectric surface [x direction, Fig. 3(e)], n increases from below 10^{12} cm^{-3} (depletion) at $V_G = 0$ V to 10^{14} cm^{-3} at $V_G = 1$ V and above 10^{17} cm^{-3} at $V_G = 5$ V (accumulation); (2) on top of the source electrode [y direction, Fig. 3(f)], n increases from below 10^{12} cm^{-3} at $V_G = -5$ V (depletion) to about 10^{14} cm^{-3}, when V_G is above 0 V; and (3) as a result, the accumulated interface is accompanied by the increased current density J_y [Fig. 3(i)] in the center of the gap between two electrodes, and the L-type channel dominates when V_G increases from zero to a positive value [Figs. 3(m) and 3(n)].

For output scanning (increasing V_D with a fixed V_G), the features are as follows: (1) at the dielectric surface [x direction, Fig. 3(g)], n decreases from 10^{19} cm^{-3} (accumulation) at $V_D = 0.1$ V to 10^{15} cm^{-3} at $V_D = 7$ V and below 10^{12} cm^{-3} at $V_D = 20$ V (depletion); (2) on top of the source electrode [y direction, Fig. 3(h)], n remains almost constant ($\sim 10^{14}$ cm^{-3}); and (3) as a result, the current distribution shifts from being in the center of the gap to being near the source electrodes when $V_D \gg V_G$ [Fig. 3(k)], that is, the transition from the L-type to I-type channel [Figs. 3(o) and 3(p)]. More details of the transition in output scanning are shown in Fig. S1 within the Supplemental Material [18]. Generally speaking, the primary channels shift from being next to or above the source electrodes to the center of the gap when V_G increases, whereas the opposite occurs when V_D increases toward and beyond V_G. With the above information, we study the transfer and output characteristics, derive equations to describe the I-V relations in their simplest forms, and clarify the impacts of device factors on performance in the following sections.

B. Subthreshold transfer characteristics

The main issue with vertical transistors is the difficulty of obtaining a sharp turn-on property and a high on:off ratio (I_{on}/I_{off}), especially with a steep subthreshold swing and a low off current. In addition to using semiconductors with a low intrinsic carrier density, the parameters for device structure should carefully considered. The features of threshold voltage, V_{th}, are discussed by referencing $\phi_s(x)$. According to Eq. (6), above or below a certain V_G, $\phi_s(x)$ could be higher or lower than the source potential, ϕ_{s0}, and then the carrier density, n, would be above or below that near the source (n_S), leading to strong accumulation or deep depletion. Thus, the value of V_G resulting in $\phi_s(x) = \phi_{s0}$ in Eq. (6) can be referenced to discuss V_{th} in I-V characteristics and, then, the relationship between V_{th} and V_D is

$$V_{th} \propto -\frac{C_{SC}}{C_{ox}} V_D. \tag{9}$$

Accordingly, when the capacitance ratio C_{SC}/C_{ox} is small, V_{th} is weakly affected by the V_D, but, when C_{SC}/C_{ox} is large, a more positive (negative) V_D leads to more negative (positive) V_{th} for n-type (p-type) devices. This result well explains the experimental results in previous reports [19] and agrees well with the TCAD-simulated device shown below.

1. Subthreshold swing

In the subthreshold regime ($V_G < V_{th}$), the I-type channel dominates and entire electrodes are injecting the current. The subthreshold current is governed by diffusion current, $I_S \cong I_0 \exp(qV_m/kT)$, where I_0 is proportional to the area of the source electrode S and the diffusion coefficient D_n, and $V_m < 0$ is the applied voltage across the depletion region, which regulates the carrier density around the source electrode. Because of the continuity of the electric field and the rotational symmetry of the potential around the source [see Figs. 2(h) and 2(i)], the potential V_m around the source follows the interfacial potential ϕ_s on the same contour line (denoting the corresponding position as $x = x_m$). As ϕ_s is tuned by both V_G and V_D, as described

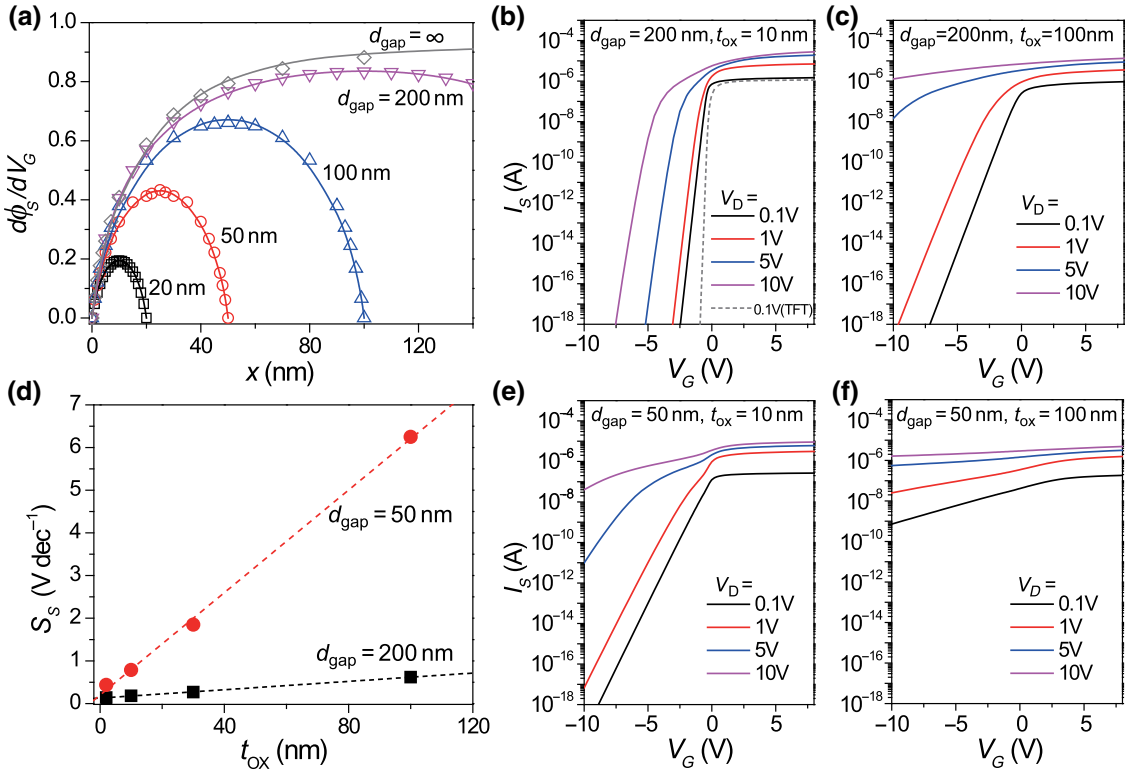

FIG. 4. Subthreshold transfer characteristics. (a) Differential change of $\phi_s(x)$ to V_G. Devices have varied d_{gap} values ($d_{gap} = 10$–200 and ∞, $t_{ox} = 10$ nm). Dots are TCAD-simulated data and curves are calculated from Eq. (7). (b),(c) Transfer curves for devices with $d_{gap} = 200$ nm and an oxide thickness, t_{ox}, of 10 (b) or 100 nm (c). Only the source current, I_S, from the middle of five neighboring electrodes is shown, the same below. In (b), data of conventional TFT with the same materials ($W/L = 0.5$ and the semiconductor is 20 nm thick) are shown as a reference (gray dashed curve). (d) Extracted S_S values ($V_D = 0.1$ V) as a function of t_{ox} for devices with $d_{gap} = 50$ nm (red) or $d_{gap} = 200$ nm (black). (e),(f) Transfer curves of devices with $d_{gap} = 50$ nm and $t_{ox} = 10$ (e) or 100 nm (f). Parameters of the TCAD-simulated device are $q\varphi_b = 0.4$ eV, $t_{ox} = 10$ or 100 nm, $t_{SC} = 320$ nm, and $d_{gap} = 20$–200 nm.

by Eq. (6), the drain current I_D in the subthreshold regime can be expressed as

$$I_D \cong I_0 \exp\left(\frac{qV_D}{bkT}\right) \exp\left[\frac{q(V_G - V_{th})}{akT}\right] \propto \exp\left[\frac{q\eta_0 V_D}{kT\left(1 + \frac{C_{ox}}{C_{SC}}\right)}\right] \exp\left[\frac{q\eta_0 V_G}{kT\left(1 + \frac{C_{SC}}{C_{ox}}\right)}\right], \quad (10)$$

and η_0 is the value of η defined by Eq. (6b) at $x = x_m$ from the source. Factors a and b are the values of $[\partial\phi_s(x)/\partial V_G]^{-1}$ and $[\partial\phi_s(x)/\partial V_D]^{-1}$, respectively, at $x = x_m$ described by Eq. (7). They characterize how the I_D changes according to the V_G and V_D in the subthreshold regime, respectively. The reversed subthreshold slope (S_S) is

$$S_S = \left(\frac{\partial \log_{10} I_D}{\partial V_G}\right)^{-1} \cong \frac{kT\ln 10}{q} a = \frac{kT\ln 10}{\eta_0 q}\left(1 + \frac{C_{SC}}{C_{ox}}\right). \quad (11)$$

When there are substantial interfacial traps, we can modify Eq. (11) by replacing C_{SC} with $C' = C_{SC} + C_{IT}$, where C_{IT} is the capacitance per unit area induced by interfacial traps, and the value of S_S obviously increases.

When the electrodes are dispersed ($d_{gap} \sim \infty$), coupling in the field between neighboring electrodes is weak, and $\eta(x) = 1 - \exp(-x/L_D)$. To estimate S_S, we use L_D as x_m and obtain $\eta_0 = 1 - 1/e$ and so $S_S \cong (1.46kT/q)[1 + (C_{SC}/C_{ox})]$. The lower limit of S_S is obtained by using infinite C_{ox} and, for a device at 300 K, the value is 96 mV dec^{-1}. When the electrodes are composed of a dense conductive network ($d_{gap} \sim L_D$), the coupling between neighboring electrodes is significant; thus, the second case of Eq. (6b) is involved. The values of $\partial\phi_s(x)/\partial V_G$ for various d_{gap} (from 20 nm to ∞) are calculated and plotted in Fig. 4(a) (curves) and agree well with those extracted from the 2D TCAD-simulated device (hollow dots). Obviously, strong control of $\phi_s(x)$ can be obtained with large d_{gap}.

To examine the S_S values, the 2D numerically simulated transfer curves of devices are shown in Figs. 4(b) and 4(c), which exhibit shapes similar to those

of the experimental results [13,20]. Data of a conventional TFT are also shown for reference [Fig. 4(b), dashed curve]. Importantly, the S_S values clearly follow a linear relationship with t_{ox} [Fig. 4(d)], which is highly consistent with Eq. (11). For example, for the device with $d_{gap}=200$ nm and $V_D=0.1$ V, S_S is 140 or 181 mV dec^{-1} when $t_{ox}=2$ or 10 nm, respectively. This result also agrees well with the experimental results of vertical transistors based on a polymer semiconductor, Poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,59-(2,29-bithiophene)} (P(NDI2DO-T2), and porous gold electrodes [13]. In these devices, using a thin high-k AlO_x dielectric layer efficiently reduces S_S, as compared with using a thick low-k SiO_2 dielectric layer.

By contrast, the subthreshold swing of the TCAD-simulated device becomes less steep with sharply increased S_S, when the value of t_{SC} decreases (see Fig. S2 within the Supplemental Material [18] for more details), which also agrees with Eq. (11). In addition, when d_{gap} decreases, the potential ϕ_s becomes much less sensitive to V_G, the value of η decreases, and the value of $S_S \propto 1/\eta_0$ increases correspondingly. For example, the transfer curves from a device with $d_{gap}=50$ nm are shown in Figs. 4(e) and 4(f), wherein the extracted S_S is much larger than that with $d_{gap}=200$ nm [Fig. 4(d)]; this also validates the above discussion.

2. The impact of V_D

According to Eq. (10), the current increases when V_D increases, even in the subthreshold regime. This is consistent with Figs. 4(b)–4(c) and 4(e)–(f). We can characterize such a property by defining a parameter, $SS_D = (\partial \log_{10} I_D/\partial V_D) = (kT\ln 10/\eta_0 q)[1+(C_{ox}/C_{SC})]$, for a certain V_G value, learning from the definition of S_S. For example, when a typical device is in the deep subthreshold regime ($V_G=-7$ V), the value of SS_D is 448 mV dec^{-1} when t_{ox} is 10 nm and 152 mV dec^{-1} when t_{ox} is 200 nm (see Fig. S3 within the Supplemental Material [18] for more details). These results indicate the weaker dependence of the current on V_D with thinner dielectric films. A small value of C_{SC}/C_{ox} simultaneously leads to strong gate tuning (high I_{on}/I_{off} with small S_S) and weak drain tuning, which is required for stable circuit applications. However, when increasing the ratio of C_{SC}/C_{ox}, e.g., by using a thin semiconductor layer or thick dielectric layer, the subthreshold current becomes insensitive to V_G, but highly sensitive to V_D, according to Eq. (10), and, possibly, due to the drain-induced barrier-lowering effect. This leads to large S_S values and small I_{on}/I_{off} values. This result agree with the experimental observations of V_D-sensitive subthreshold characteristics in vertical transistors based on organic semiconductors, such as dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) [21] or oxide semiconductors, such as $InGaZnO_4$ [9].

3. Toward the lower limit of S_S

To decrease S_S toward the Boltzmann limit for FETs or TFTs (i.e., $kT\ln 10/q$), Eq. (11) shows that the most effective methods include increasing d_{gap}; reducing the oxide thickness t_{ox} to be as thin as possible, using high-k dielectrics; and increasing semiconductor thickness t_{SC} for a certain semiconductor. In addition, using nanowires with a smaller d_S leads to an even smaller S_S (see Fig. S4 within the Supplemental Material [18] for more details), because the capacity of tuning the potential above the source electrodes is enhanced. For example, using a very narrow nanowire ($d_S=1$ nm) and very thin oxide layer ($t_{ox}=1$ nm), the device with a single electrode exhibits a S_S value of 102 mV dec^{-1} (see Fig. S4 within the Supplemental Material [18] for more details), which is very close to the above-estimated limit (96 mV dec^{-1}). The above discussions are applicable for devices with either Ohmic or Schottky contacts and are similar for vertical transistors in some other structures, such as those with an insulating oxide layer on top of the source electrodes [8,22]. For metal meshes with widths of electrode lines on the micron scale, the off current and S_S will be increased because of the screening effect of the semiconductor above the sources. In particular, the strong dependence of S_S on t_{ox} and t_{SC} in such transistors is in contrast with that of micron-scale planar FETs or TFTs and, therefore, should be carefully considered during design and fabrication.

C. Above-threshold transfer characteristics

1. The I_D-V_G relation

As discussed above, when scanning V_G with a fixed V_D, the L-type channel becomes dominated and the corresponding resistance is denoted as R_{side}. Actually, d_{gap} in the devices investigated here is much smaller than that of the usual effective injection length ($\sim\mu$m) used in staggered FETs or TFTs with the current crowding effect, characterizing how far the current extends from the source electrode at the dielectric surface [14,23]. The TCAD-simulated transfer curves are shown in Fig. 5(a) (dots). Similar to FETs or TFTs, R_{side} can be divided into gate-dependent resistance, $R_{side,ch}$, and gate-independent resistance, $R_{side,C}$. The former is mainly the sheet resistance near the dielectric surface and the latter includes contact resistance near the source and some access resistances from the dielectric surface to the drain [24]. This is verified by observing the gradually decaying transconductance, $g_m = \partial I_S/\partial V_G$ [25], as shown in Fig. 5(b). The analytical form of R_{side} is rather complicated; therefore, to focus on the physical image, we consider that, when V_G increases, the carrier concentration near the dielectric surface increases and $R_{side,ch}$ decreases. Then, the I-V relationship is derived in the simplest form,

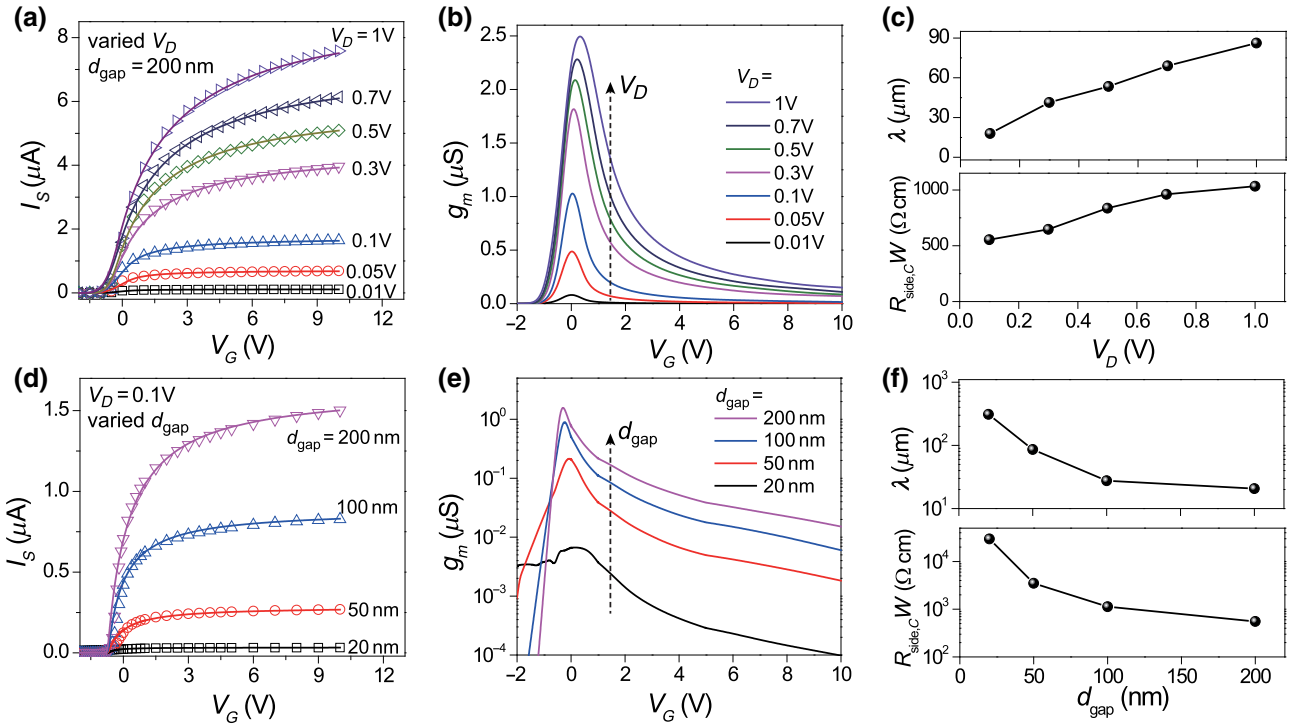

FIG. 5. Above-threshold transfer characteristics. (a)−(c) Device operated with varied V_D: (a) source current I_S from a 2D TCAD-simulated device (dots) and from fitting with Eq. (12) (curves) for various V_D values. (b) Corresponding transconductance g_m. (c) Fitting parameter equivalent channel length λ (top) and extracted parameter contact resistance $R_{side,C}$ (normalized with the channel width W, bottom). (d)−(f) Devices with varied d_{gap} operated at $V_D = 0.1$ V: (d) source current I_S with varied d_{gap} values, from a 2D TCAD-simulated device (dots) and from fitting with Eq. (12) (curves). (e) Corresponding transconductance g_m. (f) Corresponding λ and $R_{side,C}$. Parameters of the 2D TCAD-simulated device are $q\varphi_b = 0.4$ eV, $t_{ox} = 10$ nm, $t_{SC} = 320$ nm, and $d_{gap} = 20$–200 nm.

which allows for direct comparison with FETs or TFTs:

$$R_{side} = R_{side,ch} + R_{side,C} \cong \frac{\lambda}{WC_{ox}\mu(V_G - V_{th})} + R_{side,C}, \tag{12}$$

where λ is an equivalent channel length in transfer scanning, including the impact of V_D on the accumulation and drift field, W is the channel width defined by the source and drain electrodes, and μ is the carrier mobility. Equation (12) can be used to calculate $I_S = V_D/R_{side}$ and fit transfer curves with $V_D \ll V_G$ using λ and V_{th} as fitting parameters. The value of $R_{side,C}$ is extrapolated by the Y function used in FETs or TFTs [26,27]. In the case with large V_D or rich defects, $(V_G–V_{th})^\beta$ should be used instead of $V_G–V_{th}$ and β is a fitting parameter above one, to consider different accumulation or hopping transport [28,29]. As observed in Fig. 5(a), Eq. (12) provides generally good fitting (curves) to the numerically simulated device (dots) using various V_D values, and thus, verifies the above derivations.

2. Characteristic parameters

The equivalent channel length λ in Eq. (12) varies with varying V_D, d_{gap}, and the injection barrier. As shown in Fig. 5(c), λ increases when V_D increases, because the interfacial potential, ϕ_s, increases and the carrier density decreases, according to Eq. (6) and as shown in Fig. 3(g). This effect is considered in output scanning in the next section. In comparison, $R_{side,C}$ weakly depends on V_D. In general, λ and $R_{side,C}$ decrease sharply when the injection barrier $q\varphi_b$ decreases and d_{gap} increases. The large λ shown in Fig. 5(c) is mainly due to a large $q\varphi_b = 0.4$ eV, which probably limits current injection and the gate-tuning capacity of carrier concentration near the source. The impact of varied d_{gap} is shown in the transfer curves given in Fig. 5(d) (dots), which are well fitted by Eq. (12) (curves). As discussed above, when d_{gap} decreases, the gate tunability of the interfacial potential, ϕ_s, decreases through an almost exponential decay [Eq. (6)]. This is also manifested in Figs. 5(e) and 5(f), where transconductance g_m significantly decreases and λ and $R_{side,C}$ significantly increase when d_{gap} decreases. Moreover, the gradually saturated current in the transfer curves, as described in Eq. (12) and shown in Figs. 5(a) and 5(d), agrees well with the experimental results of organic vertical transistors, e.g., using C_{60} as the semiconductor and porous gold films as the source electrodes [30].

D. Output characteristics

1. The I_D-V_D relation

As discussed above, when V_D increases, ϕ_s increases and the gap-center area gradually changes from accumulated to depleted, with the gradual transition from L-type to I-type channels. Then, the total resistance, $R_{\rm tot}$, can be simplified as the parallel resistances composed of $R_{\rm side}$ (discussed above) and $R_{\rm top}$ (along the vertical channel between the source and the drain):

$$R_{\rm tot} = \frac{V_D}{I_S} = (R_{\rm side}^{-1} + R_{\rm top}^{-1})^{-1}. \tag{13}$$

When V_D increases from zero, $R_{\rm tot}$ is mainly dominated by $R_{\rm side}$ first and then becomes mainly dominated by $R_{\rm top}$.

To describe $R_{\rm side}$, we refer to Eq. (12) and consider that accumulated carriers in the center of the gap will be reduced as ϕ_s gradually increases during output scanning. For reference, we consider the channel resistance, $R_{\rm ch}$, in FETs and TFTs: when $V_D < V_G$, the carrier concentration is proportional to $C_{\rm ox}(V_G - V_{\rm th} - BV_D)/q$, where B is a constant and is 1/2 in TFTs, and therefore, $R_{\rm ch} \propto (V_G - V_{\rm th} - BV_D)^{-1}$. We use Taylor expansions for $R_{\rm ch}$, so that $R_{\rm ch}$ is approximately proportional to $(V_D)^{\alpha}$, where α is a constant and should be close to one in vertical transistors by referencing Eq. (6). In addition, the capacitance ratio, $C_{\rm SC}/C_{\rm ox}$, is usually small and $V_{\rm th}$ remains almost constant during output scanning by referencing Eq. (9). Therefore, Eq. (12) can be used in output scanning by considering the impact of V_D in the equivalent channel length λ:

$$\lambda = \lambda_0 \left(\frac{V_D}{1}\right)^{\alpha}, \tag{14}$$

where 1 denotes 1 V and λ_0 is a constant that decreases when $q\varphi_b$ decreases or $d_{\rm gap}$ increases. Equation (14) also agrees well with data shown in Fig. 5(c), verifying the simplification.

To determine $R_{\rm top,}$ we consider current density J injected from the source, which is diffusion limited [31], $J = q\mu N_c \exp(-q\varphi_b/kT)[1 - \exp(-qV_a/kT)]\epsilon$, where N_c is the effective density of states for the conduction band, and V_a is the applied voltage on the semiconductor (much larger than kT). The electric field is approximated as $\epsilon \cong V_D/t_{\rm SC}$, as $t_{\rm SC}$ is usually much larger than the thickness of electrodes. Then, $R_{\rm top}$ is simplified as

$$R_{\rm top} = \frac{V_D}{JS} \cong \frac{t_{\rm SC}}{Wd_S\theta} \frac{\exp(q\varphi_b/kT)}{qN_c\mu}, \tag{15}$$

where S is the injection area of the source electrode, d_S is the width or diameter of the nanowire or nanotube electrodes, and θ is the geometrical factor related to the shape of and distance between the source electrodes. Accordingly, the differential output resistance, $R_{\rm dif} \equiv \partial V_D/\partial I_S$, generally approaches a constant, as $R_{\rm top}$ described by Eq. (15), when V_D exceeds V_G. This is highly consistent with the 2D TCAD numerical simulations. The simulated output curves above the threshold are shown in Fig. 6(a) (dots) and extracted $R_{\rm dif}$ is shown in Fig. 6(b). Additionally, it is consistent with the experimental results of vertical organic transistors with carbon-nanotube-network electrodes and DNTT semiconductors [21], wherein the differential output resistances gradually become independent of V_D.

$R_{\rm tot}$ described by Eq. (13) well fits the output characteristics of the 2D TCAD-simulated devices, as shown in Fig. 6(a) (curves). The five curves with various V_G are fitted by only using a single set of fitting parameters, λ_0 (2 μm), $V_{\rm th}$ (−0.05 V), and $R_{{\rm side},C}$ (1.22×10^5 Ω), whereas $R_{\rm top}$ is extracted by reading the plateau in the $R_{\rm dif}$-V_D curves [Fig. 6(b)] and α is set as 1.1 empirically. The critical parameters in determining $R_{\rm top}$ as the final output resistance, according to Eq. (15), are the injection barrier, $q\varphi_b$, and semiconductor thickness, $t_{\rm SC}$. First, the extracted $R_{\rm top}$ values from devices with different injection barriers are shown in Fig. 6(c), which follow the exponential law with $q\varphi_b$ and agree with the above derivations. Second, the output curves of devices with various $t_{\rm SC}$ values are shown in Fig. 6(d). Extracted $R_{\rm dif}$ and $R_{\rm top}$ increase as $t_{\rm SC}$ increases, as shown in Figs. 6(e) and 6(f). In Fig. 6(f), the lines depict $R_{\rm top}$ calculated directly from Eq. (15), using θ as 4.3 or 3.2 for $d_{\rm gap} = 200$ or 50 nm, respectively. The calculated values agree well with the 2D TCAD-simulated devices, verifying Eq. (15) in predicting the output resistance of Schottky-contact devices.

2. Saturation or not

The output conductance finally approaches a constant, $g_{d0} = 1/R_{\rm top}$, that is independent of V_D. When the contact-induced depletion is significant, g_{d0} is very small and may benefit stable circuit applications. However, this behavior may only be referred to as "pseudosaturation" because "real saturation" for an ideal MOSFET or TFT is defined as zero g_d. As discussed above, the tops of the source electrodes are the main injection areas and the device works as a diode or resistor, when the I-type channel dominates; the sides of the source electrodes are the main injection areas and the device works similarly with TFTs, when the L-type channel dominates. Therefore, to achieve better saturation, one strategy is to eliminate the I-type channel and keep only the L-type channel, where carriers at the semiconductor-dielectric interface become weakly accumulated or even depleted when $V_D > V_G$ in a Schottky-contact device. This understanding well explains that, in some experiments [32], capping the top of source electrodes with an insulating oxide film leads to better saturated behavior in vertical transistors. Without such capping, a high output resistance calls for severe Schottky contacts and is also expected to be

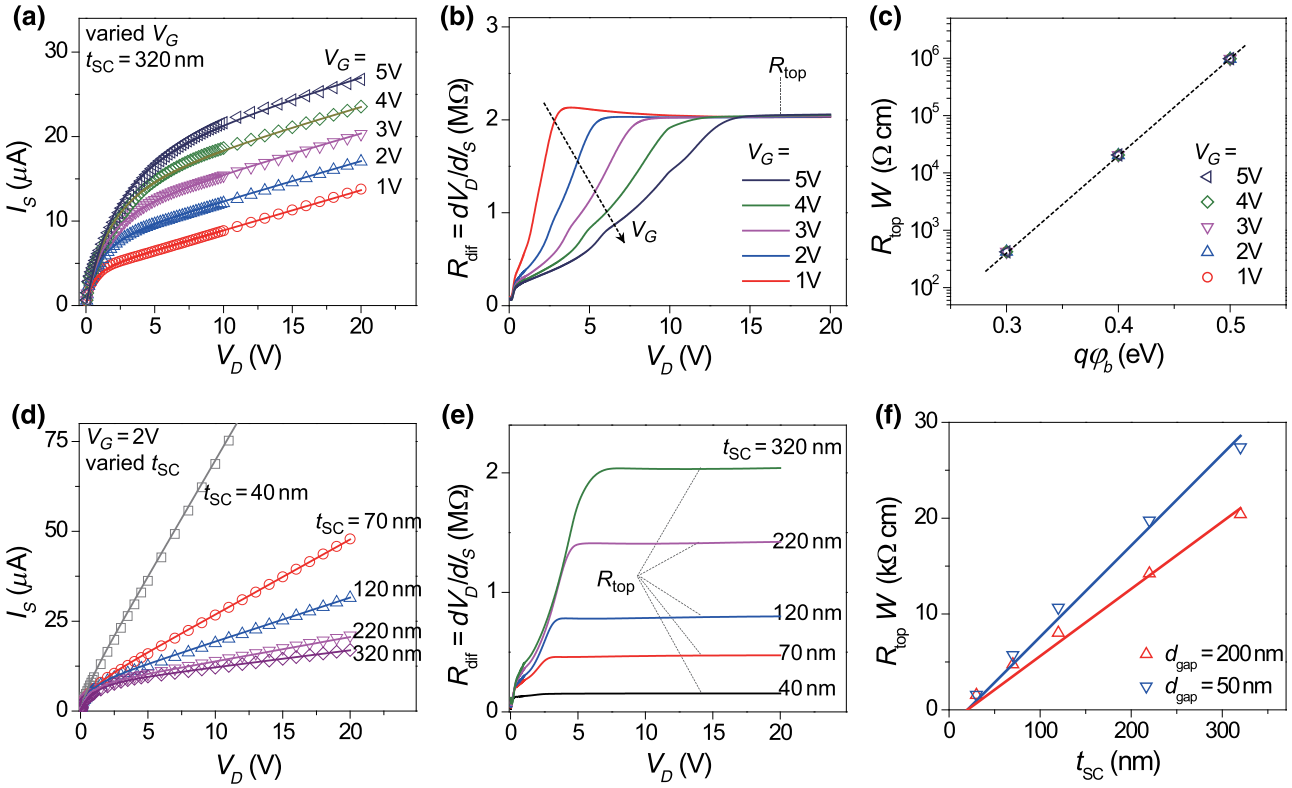

FIG. 6. Output characteristics. (a) Output characteristics for various V_G values from the TCAD-simulated devices (dots) and fitting (curves). (b) Extracted differential output resistance R_{dif}, all of which gradually approach constant R_{top}. (c) Extracted R_{top} (normalized by W) from the output characteristics as a function of the injection barrier $q\varphi_b$, with the dashed line showing $R_{top} \propto \exp(q\varphi_b/kT)$. Dots from various V_G values overlap. (d) Output characteristics for devices with various film thicknesses of semiconductor t_{SC} from 40 to 320 nm ($V_G = 2$ V). (e) Extracted R_{dif}. (f) Extracted R_{top} (normalized by W) from devices with various t_{SC} values (red dots). Red line represents values calculated from Eq. (15). Parameters of the TCAD-simulated device are $q\varphi_b = 0.4$ eV, $t_{ox} = 10$ nm, and $d_{gap} = 200$ nm. In (f), data of R_{top} for devices with $d_{gap} = 50$ nm are also shown (blue dots and line).

obtained by using multilayer semiconductors with a large energy offset between their conduction levels. In contrast, it cannot be obtained in an Ohmic-contact device if the I-type channel dominates, wherein the space-charge-limited current governs the output characteristics [33], for example, $I_D \propto V_D^2$, when there are no defects. This is observed in some vertical transistors showing a large and increasing g_d, for example, devices using porous aluminum electrodes and a poly(3-hexylthiophene) semiconductor [33] or using carbon-nanotube-network electrodes and organic pentacene semiconductor [34].

E. Design rules for devices

1. Impacts of device factors

A primary motivation for developing such vertical transistors is to obtain a high on-current density (J_{on}) without submicron patterning techniques. We use the above knowledge and 2D TCAD-simulated devices to summarize the impacts of various device factors, including $q\varphi_b$, t_{ox}, t_{SC}, d_{gap}, and d_S, on the device performance. As a negative V_G is needed to obtain a large on:off ratio in the presented transistors, the ratio between currents when $V_G = 5$ V and $V_G = -5$ V are calculated, and the lower limit of detected current is set as 10^{-20} A. Because the surface area of a vertical transistor is $W(d_S + d_{gap})$ per electrode, the current per unit area J_{on} is defined as $J_{on} = I_{on}/[W(d_S + d_{gap})]$. Data for simulated devices with $V_D = 0.1$ V are shown in Fig. 7 and the impacts are as follows:

(1) Impact of injection barrier $q\varphi_b$ [Fig. 7(a)]. Although a small value of $q\varphi_b$ leads to large values of J_{on} and on:off ratio, it also leads to a very large value of g_d in output scanning and almost-zero g_m in transfer scanning in the on state, causing large current fluctuations, weak gate tuning in the on state, and very small gain if used in logic units. Thus, devices with moderate Schottky contacts are needed, if large output resistance and strong gate tuning in the on state are required.

(2) Impact of oxide thickness t_{ox} [Fig. 7(b)]. This is straightforward, as the thin dielectric thickness benefits a large value of J_{on}, high I_{on}/I_{off} ratio, small S_S, and low operational voltage.

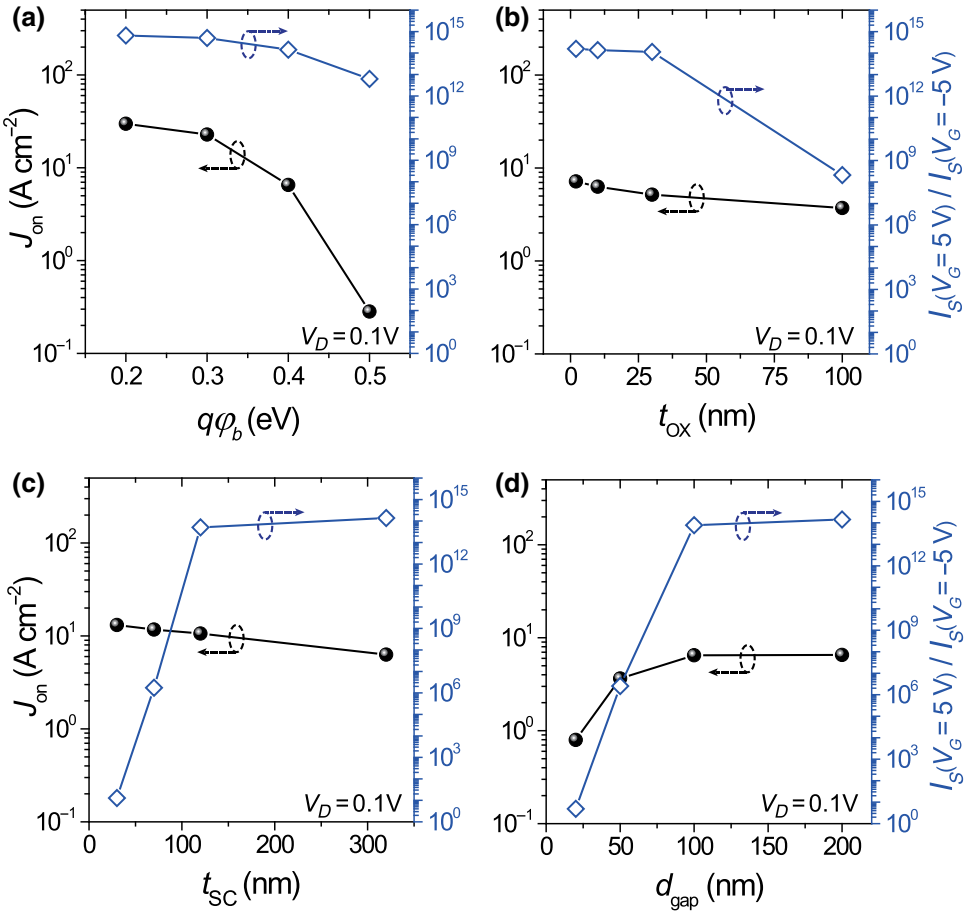

FIG. 7. Current density and on:off ratio. Extracted values of J_{on} and current ratio between $V_G = 5$ V and -5 V for devices ($V_D = 0.1$ V) with various (a) $q\varphi_b$, (b) t_{ox}, (c) t_{SC}, or (d) d_{gap} values. Parameters of the TCAD-simulated device are based on $q\varphi_b = 0.4$ eV, $t_{ox} = 10$ nm, $t_{SC} = 320$ nm, and $d_{gap} = 200$ nm, and one parameter at a time is changed to investigate the impact.

(3) Impact of semiconductor thickness t_{SC} [Fig. 7(c)]. Although a small t_{SC} leads to a large value of J_{on}, it also leads to a high value of I_{off}, low I_{on}/I_{off} ratio, and large S_S, as the interfacial potentials become sensitive to V_D. Therefore, similar to $q\varphi_b$, the impact of decreased t_{SC} has both advantages and disadvantages and is dependent on certain application purposes.

(4) Impact of gap width d_{gap} [Fig. 7(d)]. In Schottky-contact devices, very dense electrodes with a small value of d_{gap} do not lead to a higher value of J_{on} due to the weakened gate-tuning capacity and a low carrier concentration. A large on:off ratio and small S_S can be obtained only when d_{gap} is much larger than L_D (above 100 nm in the presented devices), but, if it is too large, it will lead to a reduced current density because the proportion of the electrode area decreases.

(5) Impact of the width of the source electrode d_S. When the value of d_S increases, S_S increases, the off-current increases, and the on:off ratio decreases. This is because the gate-tuning capacity decreases for areas above the source electrodes. Above the threshold, the impact of increasing d_S depends on the channel type: when the I-type channel dominates (e.g., Ohmic contact or $V_D \gg V_G$), the on-state current I_{on} increases linearly with increasing d_S [according to Eq. (15)] and then J_{on} increases, because the injection area increases; when the L-type channel dominates (e.g., Schottky contact with $V_D < V_G$), the value of I_{on} is not significantly affected, but J_{on} decreases because the proportion of the injection area (mainly the sides of the sources) decreases. These results are also verified by TCAD device simulations (see Fig. S4 within the Supplemental Material [18] for more details). Therefore, narrow nanowires or fine metal meshes generally lead to a steep subthreshold swing, but the impact on the current density depends on the contact properties and operational modes.

2. Comparison with TFTs

For applications, we compare the studied vertical transistors with TFTs in terms of current density. For a TFT with Ohmic contacts operating in the saturated regime, the source-drain current is $I_{D,TFT} = (W/2L)C_{ox}\mu(V_G - V_{th})^2$ with channel length L [35]. When the lengths of the source and drain electrodes are the same (L_S), the surface area of a TFT is $W(L + 2L_S)$ and the saturated current per unit area J_{on} is $J_{on,TFT} = I_{D,TFT}/[W(L + 2L_s)] = C_{ox}\mu(V_G - V_{th})^2/[2L(L + 2L_s)]$. For example, for typical vertical transistors with Schottky contacts ($q\varphi_b = 0.4$ eV), the current level at $V_D = 10$ V and $V_G = 2$ V is

I_{on}= 11.6 μA for one of the electrodes of the device shown in Fig. 6(b). Then, the value of $J_{on} = I_{on}/[W(d_s + d_{gap})]$ is 52.6 A cm^{-2}. To afford the same values of J_{on}, an Ohmic-contact TFT with the same semiconductor, dielectric, and operational voltages ($V_G = 2$ V and $V_{th} = 0$ V) should have a channel length of $L = 1.2$ μm when $L_S = 5$ μm or $L = 2.14$ μm when $L_S = 2$ μm. Therefore, even for a vertical transistor with Schottky contacts, its current density per unit surface area is comparable to that of Ohmic-contact TFTs with dimensions at the limit of conventional photolithography ($L = L_S = 2$ μm). With a smaller value of $q\varphi_b$, the vertical transistors will have a larger value of J_{on} and are comparable to TFTs with a sub-500-nm channel length.

IV. CONCLUSION

Device theories and physical images are developed and revealed for vertical transistors with conductive-network electrodes. An approximated and simplified form of the potential at the semiconductor-dielectric interface (ϕ_s) is derived, which indicates that the potential distribution can be tuned by both the gate field and drain field, like a plucked string. The capability of tuning ϕ_s by V_G decreases if the spacing between the electrodes decreases or the capacitance ratio between the semiconductor and dielectric layers (C_{SC}/C_{ox}) increases.

The subthreshold current increases exponentially with ϕ_s raised by V_G; thus, moderately large spacing between the electrodes and a small capacitance ratio (C_{SC}/C_{ox}) will benefit fast turn-on properties of the devices toward the Boltzmann limit. During transfer scanning with increasing V_G, the dielectric surface in the gap between electrodes changes from depletion to accumulation, forming L-type conduction channels. During output scanning with increasing V_D, the dielectric surface between the source electrodes changes from accumulation to depletion, allowing for a transition from L-type to I-type conduction channels. Simple equations to describe the I-V relationships are derived for both transfer and output characteristics, allowing direct comparisons with planar FETs or TFTs. The derived theories and equations are verified via numerically simulated devices and are in agreement with the experimental results from devices composed of organic or oxide-based semiconductors. The device theories and physical images reveal the device operation mechanisms and provide explicit guidance for the design, fabrication, and characterization of such vertical transistors.

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