# Gate-Defined Accumulation-Mode Quantum Dots in Monolayer and Bilayer $WSe_2$

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(Received 26 February 2020; revised manuscript received 26 March 2020; accepted 14 April 2020; published 22 May 2020)

*This paper is a contribution to the joint Physical Review Applied and Physical Review Materials collection titled* Two-Dimensional Materials and Devices.

We report the fabrication and characterization of gate-defined hole quantum dots in monolayer and bilayer $WSe_2$. The devices are operated with gates above and below the $WSe_2$ layer to accumulate a hole gas, which for some devices is then selectively depleted to define the dot. Temperature dependence of conductance in the Coulomb-blockade regime is consistent with transport through a single level, and excited-state transport through the dots is observed at temperatures up to 10 K. For adjacent charge states of a bilayer-$WSe_2$ dot, the magnetic field dependence of excited-state energies is used to estimate $g$ factors between 0.8 and 2.4 for different states. These devices provide a platform to evaluate valley-spin states in monolayer and bilayer $WSe_2$ for application as qubits.

DOI: 10.1103/PhysRevApplied.13.054058

## I. INTRODUCTION

Certain crystals possess two or more inequivalent band extrema, or valleys, that can serve as a pseudospin defining a qubit. Application of the valley and spin degrees of freedom for qubits was demonstrated in carbon-nanotube quantum dots [1] and has also been investigated in Si quantum dots [2,3]. As an alternative, coherent valleytronics using few-layer transition-metal dichalcogenides (TMDs) and their heterostructures offers long-lived and coherent valley-spin states [4–14], several proposals for qubit designs [15–22], and an inherent light-matter interface for control, readout, and coupling to other quantum systems [23].

Confinement sufficient to address valley-spin states of a small number of particles is required to define a qubit in this context, and significant recent activity in this area has focused on quantum emitters localized by defects [24–27], strain [28–30], and moiré patterns [31–34]. For the valley pseudospin, localization to length scales not much greater than the lattice spacing generates valley coupling that would be detrimental to the design and coherence of an eventual TMD valley-spin qubit [35]. Gate-defined quantum dots, in addition to allowing electronic probes and electrical control of devices, provide a means to tune the confinement length $L$ in valley-based qubits to balance the competing demands of valley coupling in small dots against impractically small level spacing $\Delta \propto 1/L^2$ in large dots.

TMD single quantum dots defined by gates have been reported for multilayer $WSe_2$ and $WS_2$ [36,37] and few-layer $MoS_2$ [38–40], and a double quantum dot has been reported in multilayer $MoS_2$ [41]. Additionally, excited states have been observed in a dot defined in a $MoS_2$ nanotube [42], and size-controlled dots have also been formed in etched $MoS_2$ [43]. All gate-defined two-dimensional TMD quantum-dot devices reported so far have operated in a so-called classical limit, $\Delta < k_B T$, in which the individual quantum states required to define an eventual qubit were not resolved [44].

We report the fabrication and characterization of gate-defined hole quantum dots using monolayer and bilayer $WSe_2$, which has so far been the most actively investigated and promising material for non-gate-defined quantum emitters. Our devices have $L \sim 25$ nm, small enough for the observation of discrete levels at temperatures up to 10 K. Because of the low level of unintentional doping in monolayer and bilayer $WSe_2$, an additional accumulation gate is required to generate a hole gas within which the dot could be defined, similar to an approach that has been used successfully for quantum dots in Si [45,46]. Temperature dependence of a Coulomb-blockade conductance-peak maximum confirms single-level transport, and comparison of excited-state energies at different magnetic fields provides a lower bound on the $g$ factors of excited states of adjacent charge states in

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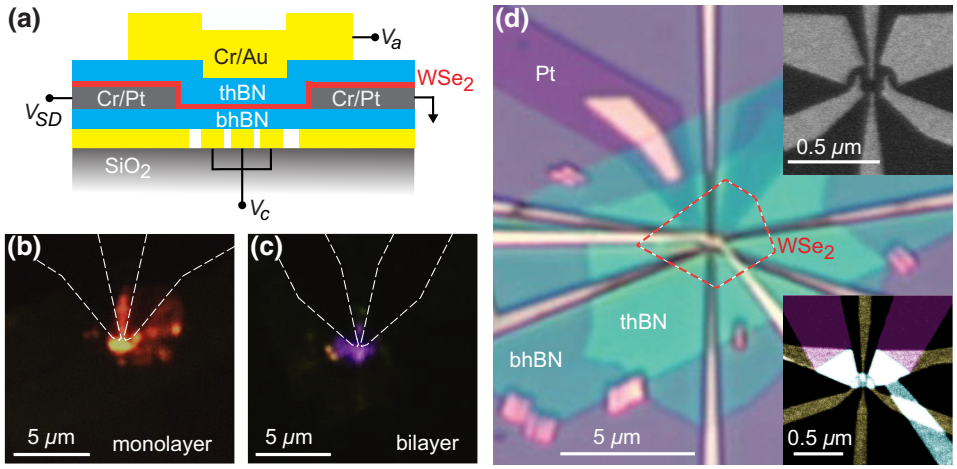


FIG. 1. (a) Monolayer- or bilayer-$WSe_2$ quantum-dot devices, contacted on the bottom by Pt, encapsulated by top (thBN) and bottom (bhBN) *h*-BN layers, and with bottom confining gates and a top accumulation gate. (b) Photoluminescence images of a monolayer-$WSe_2$ device and (c) a bilayer-$WSe_2$ device with contacts outlined in white. (d) Optical image of a complete device (the location of $WSe_2$ is outlined with a dashed red line). The upper inset shows a scanning electron micrograph of the confining gates. The lower inset shows a false-color scanning electron micrograph of a complete device showing alignment of the confining gates (yellow), *h*-BN-support gates (green), contacts (purple), and the accumulation gate (blue).

a bilayer-$WSe_2$ quantum dot ranging from $g = 0.8$ to $g = 2.4$.

## II. EXPERIMENTAL METHODS

Because of the relatively large band gap and large effective mass in $WSe_2$ compared with most other materials used for gate-defined quantum dots, two principles guide the design of our devices: first, gate dimensions are made as small as possible to maximize $\Delta$, and second, metal contacts are brought as close as possible to the entrance and exit of the dot to avoid the creation of multiple accidental dots in the contact region.

A schematic of the $WSe_2$ quantum-dot devices we fabricate is shown in Fig. 1(a), in which monolayer or bilayer $WSe_2$ is encapsulated by two hexagonal-BN (*h*-BN) layers and contacted from below with Pt. The devices are gated on the top with a single accumulation gate and on the bottom with four confining gates. In detail, fabrication begins with lithography and evaporation [Cr(5 nm)/Au(15 nm)] of bottom confining gates defining a quantum dot with a lithographic diameter of approximately 80–100 nm [upper inset in Fig. 1(d)]. The larger gates under the contact region of the device [colored green in the lower inset in Fig. 1(d)] are not used electrically but are present to promote flatness of the final *h*-BN/$WSe_2$/*h*-BN stack (without these features, the bottom *h*-BN layer invariably wrinkles in the dot region). Next, the confining gates are insulated by polycarbonate-based dry transfer of the bottom *h*-BN layer (approximately 10 nm thick), which is tacked in place around the perimeter [Fig. 1(d)] to prevent lateral movement during the second transfer. Bottom contacts for the $WSe_2$ are then patterned on the bottom *h*-BN layer with use of Cr(2 nm)/Pt(8 nm) deposited by electron-beam evaporation [47]. To remove processing residue from the bottom *h*-BN layer, the devices are then annealed for 3 h at 200 °C in forming gas (3% $H_2$ in Ar).

Bulk $WSe_2$ grown by chemical vapor transport is mechanically exfoliated to obtain monolayer and bilayer flakes, which are identified and confirmed by photoluminescence imaging and spectroscopy [48]. *h*-BN flakes are also obtained by exfoliation of bulk crystals, and the top *h*-BN layer (approximately 10 nm thick) and monolayer or bilayer $WSe_2$ are then picked up and transferred onto the contacts and the bottom *h*-BN layer. Photoluminescence images for monolayer and bilayer $WSe_2$ at this stage of the fabrication process are shown in Figs. 1(b) and 1(c), respectively. The top accumulation gate and bond pads (5-nm Cr and 40–65-nm Au) are then defined in a final lithography step. The accumulation gate is shaped such that holes accumulate only in the dot and contact regions of the $WSe_2$ flake. The overlay of all three metal layers is shown in the lower inset in Fig. 1(d) [49]. Finally, a second forming-gas-anneal identical to the first one is necessary to achieve adequate contact transparency for low-temperature, low-frequency transport measurements. An optical image of a completed device is shown in Fig. 1(d), with the location of the monolayer $WSe_2$ outlined in red. Devices are measured by standard dc transport and lock-in techniques in a pumped $^4$He cryostat (2 K) or a dilution refrigerator (50 mK).

## III. RESULTS AND DISCUSSION

Six devices (two monolayer devices and four bilayer devices) are measured, and we focus on electronic transport data for three of them, one monolayer device (denoted

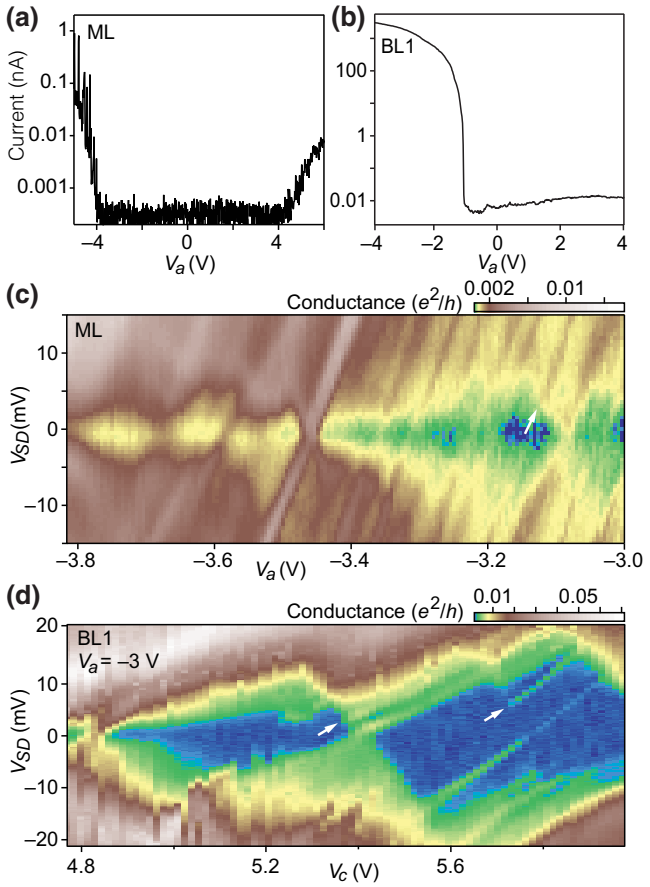


FIG. 2. (a) Current as a function of $V_a$ for monolayer device ML at a temperature of 50 mK. (b) Current as a function of $V_a$ for bilayer device BL1 at a temperature of 2.1 K. (c) Conductance as a function of $V_{SD}$ and $V_a$ for device ML. (d) Conductance as a function of $V_{SD}$ and $V_c$ with $V_a = -3$ V.

ML) and two bilayer devices (BL1 and BL2). First, direct current at fixed source-drain bias $V_{SD}$ is measured as a function of the voltage applied to the accumulation gate, $V_a$. Both monolayer devices display ambipolar transport characteristics as shown in Fig. 2(a) for device ML at a temperature of 55 mK and $V_{SD} = 12$ mV. Current strongly favors hole conduction, as expected for the high-work-function Pt contacts [47]. Bilayer devices are similar but with generally lower resistance, and in contrast to the monolayer devices, no measurable $n$-type current reliably distinct from leakage current is observed, even at a relatively high $V_{SD}$ of 0.3 V and higher temperature (2.3 K), as shown in Fig. 2(b).

In measurements of differential conductance as a function of $V_{SD}$ and gate voltage ($V_a$, confining gate voltage $V_c$, or both), all six devices show diamond-shaped conductance features indicative of Coulomb blockade. Devices with higher resistance form quantum dots when only $V_a$ is swept (accumulation mode), presumably because of sufficiently high contact resistance to form tunnel barriers at the contacts. One example of accumulation-mode operation is shown in Fig. 2(c) for device ML, in which we note a transition from well-defined though somewhat irregular Coulomb diamonds for $V_a > -3.5$ V to a more-open regime for lower $V_a$. Upward- and downward-moving features in Fig. 2(c) have slopes with similar magnitudes (+0.21 and −0.19 V/V). Defining contributions to the dot capacitance from the source, drain, accumulation gate and all confining gates as $C_s$, $C_d$, $C_a$, and $C_c$, respectively, we expect features with slope magnitudes of $C_a/C_s$ and $C_a/(C_d + C_c)$ [50]. Because $C_d \gg C_c$, near equality of slope magnitudes implies $C_s \simeq C_d$ and locates the dot approximately equidistant from each lead.

In lower-resistance devices such as BL1 [Fig. 2(b)], activation of the confining gates is required to form a dot by depletion of charge accumulated by $V_a$. Coulomb diamonds for this device as a function of $V_{SD}$ and $V_c$ at $V_a = -3$ V are shown in Fig. 2(d). Here $V_c$ is the voltage applied to all confining gates simultaneously. In this case the Coulomb diamonds are tilted with unequal slopes for positively and negatively sloped features. In a Coulomb diamond measured as a function of $V_c$, the slopes are $C_c/C_s$ and $C_c/(C_d + C_a)$ [50]. Because $C_a \gg C_c$, $C_a$ cannot be ignored in the denominator of the latter slope; therefore, diamonds as a function of $V_c$ are expected to be tilted even for $C_s = C_d$.

We also note the appearance of clear finite-bias resonances in the Coulomb diamonds of devices ML and BL1, marked with white arrows in Figs. 2(c) and 2(d). For example, these resonances appear most prominently in Fig. 2(d) at positive bias for the charge transitions near $V_c = 5.4$ and 5.7 V. Such features may arise from excited valley, spin, and/or orbital states in the limit $\Delta > k_B T$, but various extrinsic mechanisms such as quasi-one-dimensional density-of-states fluctuations in the leads could also give rise to finite-bias conductance resonances even for $\Delta < k_B T$, particularly for devices such as ours with narrow leads [51–53].

We now examine two scenarios for the observed finite-bias conductance resonances, one involving single-level transport only and one involving multilevel transport combined with some extrinsic mechanism giving rise to the finite-bias resonances. The temperature dependence of the Coulomb-blockade peak height is a standard method to distinguish between single-level and multilevel transport through a quantum dot: the peak resistance is linear in $T$ in the single-level case and independent of $T$ in the multilevel case [44,54]. For example, Song *et al.* [37] demonstrated the multilevel, temperature-independent regime for a $WS_2$ quantum dot. In Fig. 3(a) we show the evolution of a Coulomb-blockade peak at zero bias for temperatures from 2.1 to 10 K for a second bilayer-$WSe_2$ device, BL2. The resistance at the peak increases approximately linearly [Fig. 3(b)], consistent with single-level transport. We therefore conclude that device BL2 and all our other

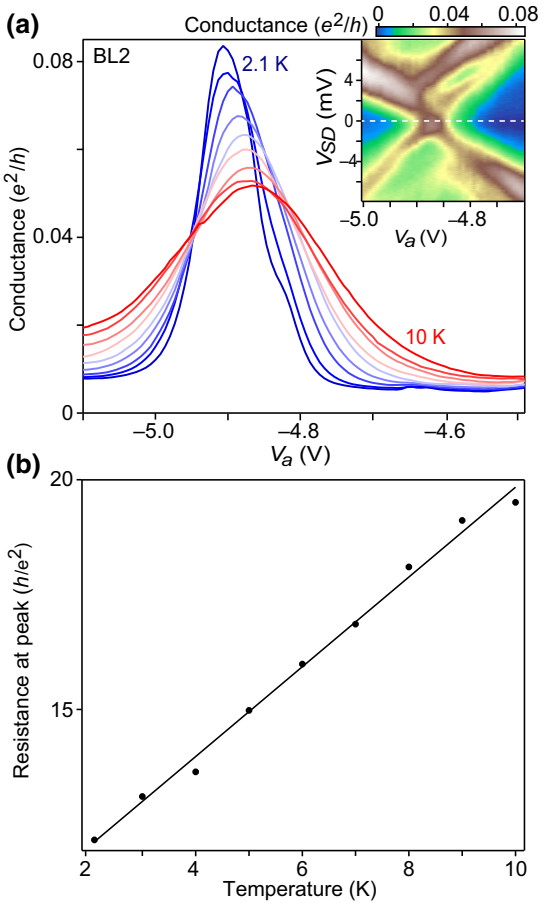


FIG. 3. (a) Conductance at zero bias and zero magnetic field as a function of $V_a$ at temperatures from 2.1 K (blue) to 10 K (red) for device BL2. The inset shows the Coulomb diamond associated with the data shown in (a), taken in a magnetic field of 8 T and at a temperature of 2.3 K. (b) Peak resistance of the curves in (a) as a function of temperature. The solid black line is a linear fit.

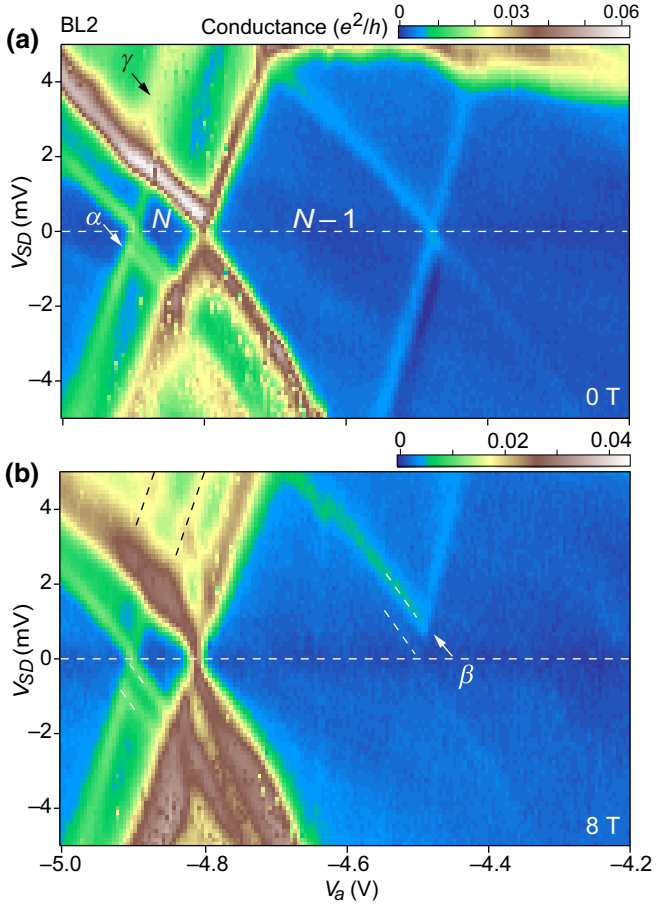


FIG. 4. (a) Conductance as a function of $V_{SD}$ and $V_a$ at zero magnetic field and a temperature of 50 mK for device BL2. (b) Same as (a) in a perpendicular magnetic field of 8 T. Pairs of dashed lines highlight the levels used to calculate $E_Z$ and $g$ factors. For the ground state below $\beta$, the position is inferred by extension from negative bias.

devices, which are lithographically identical to BL2, are small enough that $\Delta > k_B T$, and we associate the finite-bias conductance resonances with excited states of the quantum dots. Additionally, given our accumulation-gate geometry in which $V_a$ modulates the carrier density in the dot as well as the $WSe_2$ covering the contacts, we would not expect density-of-states resonances in the leads to be parallel to the Coulomb-diamond edges.

Next we investigate the magnetic field dependence of excited-state energies for two adjacent charge states in device BL2 (Fig. 4). We apply a field perpendicular to $WSe_2$ because the large out-of-plane Zeeman-like spin splitting due to spin-orbit coupling[55] suppresses in-plane moments of valley-spin states in monolayer TMDs [56]. This situation also applies to bilayer TMDs because of weak interlayer coupling [15] and "hidden spin polarization" [57,58].

At zero field an excited state, denoted $\alpha$, is visible at 0.4 meV above the ground state of the charge state labeled $N$ in Fig. 4(a). In a perpendicular magnetic field of 8 T, this state moves up to an energy of 0.8 meV without splitting, and for the $N-1$ charge state, an excited state, $\beta$, appears at 0.9 meV, while the ground-state conductance is suppressed [Fig. 4(b)]. Additionally, the state labeled $\gamma$ in Fig. 4(a) splits by 1.1 meV, as indicated by the dashed black lines in Fig. 4(b). On the basis of these energy shifts of $E_Z = g\mu_B B$, we calculate $g$ factors of 0.8, 1.9, and 2.4 for $\alpha$, $\beta$, and $\gamma$, respectively. These estimates represent lower bounds on the $g$ factors because this method of measurement is insensitive to intermediate-level crossings that may occur between 0 and 8 T.

We emphasize that these $g$ factors, which are significantly smaller than those observed for confined $WSe_2$ excitons [24–27], are not expected to be generic to all $WSe_2$ quantum dots, different even or odd charge-state pairs within the same dot, or even different levels of the same charge state. First, in addition to dot orbital effects in a perpendicular field, the Zeeman energy in $WSe_2$ hole quantum

dots has contributions from spin, valley, and atomic orbital magnetic moments [59], which in a simple model could individually combine to add to or subtract from the total moment of a given state [60], or that may each be coupled in complicated ways through device-specific parameters. Second, while the dominant contribution to spin-orbit coupling in TMDs is Zeeman-like, Rashba spin-orbit coupling is expected to be non-negligible in aggressively gated devices [61], and $g$ factors may therefore be dependent on device geometry and electric fields as well [62,63].

Given the expected importance of dot size to valley coupling strength and the performance of eventual coherent valleytronic devices, we roughly estimate the diameter of our dots using the gate capacitance. The change in gate voltage required to add one hole to the dot is

$$\Delta V_a = \frac{e}{C_a}\left(1 + \frac{\Delta}{E_C}\right),$$

where $C_a$ is the accumulation-gate capacitance and $E_C$ is the charging energy [64]. For the charge state labeled $N-1$ in Fig. 4(b), the addition energy is $E_{\text{add}} \equiv E_C + \Delta = 4.8$ meV. To obtain $\Delta$, we note that the $(N-1)$-hole excited state $\gamma$ at $V_a = -4.9$ V in Fig. 4(a) moves with $V_a$ at the same slope as the boundaries of the diamond and that $\gamma$ splits in a magnetic field. These observations strongly suggest that $\gamma$ is an orbital excited state of the dot with $\Delta = 2$ meV [53].

Using these parameters and with $\Delta V_a = 0.32$ V, we obtain $C_a \sim 0.9$ aF. The planar geometry of the device in which the accumulation gate covers the entire area of the dot permits us to model the accumulation gate and dot as a parallel-plate capacitor with the relative permittivity of $h$-BN $\epsilon_{h\text{-BN}}$ assumed to range from 2.5 to 3.5 [65,66]. The thickness of the top $h$-BN layer for device BL2 is 7 nm, which yields a dot diameter $L \sim 1520$ nm depending on the value of $\epsilon_{h\text{-BN}}$. A similar analysis for device BL1 yields a slightly larger dot size in the range from 20 to 25 nm [67]. These sizes are a factor of 3–5 larger than defect- or strain-bound quantum dots in TMDs [68] and are comparable to the size of the moiré supercell in moiré-defined dots [31–34]. We also note that a particle-in-a-box estimate for $\Delta \sim \hbar^2/mL^2$ is on the order of 1 meV assuming a hole mass of $0.45m_0$ [69], which roughly agrees with the zero-field energy of state $\gamma$.

Finally, we estimate the number of holes in our dots. Hole conduction turns on at room temperature in our devices at electric fields from the accumulation gate of approximately 0.2 V/nm, and a typical operating point for the dots at low temperature is 0.4 V/nm. In a parallel-plate approximation, the difference in threshold and operating electric fields, $\Delta E$, yields a hole density $n = \epsilon_0\epsilon_{h\text{-BN}}\Delta E/e \sim 3 \times 10^{12}$ cm$^{-2}$, and multiplication by the dot area estimated above yields a hole number that could be expected to lie between 10 and 20. Here the uncertainty is dominated by the use of room-temperature threshold voltage to estimate the location in gate voltage of zero density.

## IV. CONCLUSION

We fabricate small monolayer- and bilayer-$WSe_2$ quantum dots using a combination of accumulation and confining gates. Six devices show Coulomb blockade at temperatures below 10 K, and three devices (one monolayer device and two bilayer devices) show conductance resonances consistent with single-level transport, as confirmed by temperature dependence of the peak height for one of the devices. Magnetic field dependence of peak positions implied $g$ factors ranging from 0.8 to 2.4 in one bilayer device. In addition to satisfying essential prerequisites for the development of future electronic and/or optoelectronic qubits based on valley-spin states in few-layer TMDs, these devices also provide a platform for high-resolution, fundamental investigations of those states using Coulomb-blockade spectroscopy and other techniques.

## V. OUTLOOK

Gate-defined quantum dots based on TMDs remain at an early stage of development for valley-spin qubit applications compared to the current status of GaAs- and Si-based quantum dots for spin-only qubits. Our device design, similar to previously reported gate-defined TMD quantum dots [36–41], has followed the design of earlier lateral quantum dots quite closely. Going forward, we believe a more promising approach will be to create devices that leverage the unique advantages of TMDs, which combine a coherent valley-spin degree of freedom with an inherent light-matter interface. For example, because $WSe_2$ is an ambipolar conductor [cf. Fig. 1(a)], it is possible to create a lateral, gate-defined, and ambipolar double quantum dot in $WSe_2$. Such devices could unite the superior tunability and coherence observed for electrically controlled spin qubits with ultrafast gating that is possible with optically controlled spin qubits, resulting in valley-spin qubits with very high gate fidelity.

## ACKNOWLEDGMENTS

We acknowledge support from the U.S. Air Force Office of Scientific Research (Grant No. FA9550-16-1-0203). $WSe_2$ single-crystal growth was supported by the U.S. Department of Energy, Office of Science, Basic Energy Sciences program under Grant No. DE-SC0019467. Growth of $h$-BN crystals was supported by the MEXT Element Strategy Initiative To Form Core Research Centers (Grant No. JPMXP0112101001) and the Core Research for Evolutional Science and Technology

program (Grant No. JPMJCR15F3), Japan Science and Technology Agency.


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