Stochastic Computing Implemented by Skyrmionic Logic Devices

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Magnetic skyrmions, which are a topologically nontrivial spin texture, have been considered as promising information carriers in future electronic devices because of their nanoscale size, low depinning current density, and high motion velocity. Despite the broad interest in skyrmion racetrack memory, researchers have recently been exploiting logic functions enabled by using the particlelike behavior of skyrmions. These functions can be applied to unconventional computing, such as stochastic computing (SC), which treats data as probabilities and is superior to binary computing due to its simplicity of logic operation. In this paper, we demonstrate SC implemented by the use of skyrmionic logic devices. We propose a skyrmionic AND-OR logic device as a multiplier in the stochastic domain and two skyrmionic multiplexer (MUX) logic devices as stochastic adders. With the assistance of voltage-controlled magnetic anisotropy (VCMA), precise control of skyrmion collisions is not required in the skyrmionic AND-OR logic device, thus improving the operational robustness. In the two MUX logic devices, skyrmions can be driven by the Zhang-Li torque or the spin-orbit torque (SOT). In particular, we can regulate the skyrmion motion flexibly by using VCMA or voltage-controlled Dzyaloshinskii-Moriya interaction in the SOT case. Furthermore, a 3-bit stochastic multiplier and adder are demonstrated by micromagnetic simulations. Simulations in synthetic antiferromagnets show that the performance of our skyrmionic logic gates can be optimized through the use of advanced materials. Our work opens up possibilities for implementing SC using skyrmionic logic devices.

I. INTRODUCTION

Magnetic skyrmions are topologically stable chiral structures, which are generated in B20-type bulk materials and ultrathin ferromagnetic (FM) layers and are favored by the Dzyaloshinskii-Moriya interaction (DMI) [1–4]. Because of their small size, high motion velocity, and low depinning current density, skyrmions are considered as promising carriers for transferring information in future electronic devices [5–9]. Over the years, much effort has been devoted to developing skyrmion racetrack memories [10–12], which require no mechanical parts and show great potential for advanced high-density storage. Moreover, logic devices with high operation speed and low power consumption have also been proposed, exploiting the particlelike behavior of skyrmions [6,7].

One of the most essential applications of skyrmionic logic devices is to support stochastic computing (SC), which can be realized with AND and multiplexer (MUX) logic operations. SC is an unconventional computing method that treats data as probabilities [13–17]. An N-bit bit stream with X "1"s, forming a stochastic number (SN), denotes a probability $P = X/2^N$, indicating the probability of observing a bit "1" in the bit stream. SC has been applied in a massively parallel computing system because of its tolerance to soft errors as well as its high operation speed [18]. Besides, the SN and X are flexible, which makes the application of SC very convenient. To date, SC has been implemented only in CMOS-based stochastic circuits, which suffer from challenges of power and area cost [19,20].

Skyrmionic logic devices are emerging as a solution to these issues. The existing proposals for skyrmionic AND logic devices require precise control of skyrmion collisions to execute logic operations [6,7], which rely on various effects such as skyrmion-edge interactions [21,22] and the skyrmion Hall effect [23–27]. However, recent studies have shown that the skyrmion Hall angle varies with the skyrmion velocity in the presence of defects and thermal fluctuations, therefore increasing the difficulty of accurately controlling the skyrmion trajectory [28,29]. In addition, other recent studies have shown that skyrmions with a size below 10 nm cannot be stabilized in ferromagnetic multilayers without external magnetic fields, because of the demagnetization field, while small skyrmions in ferromagnetic thin films suffer from thermal-stability issues

[30,31]. As a consequence, it is necessary to demonstrate skyrmionic gates in ferrimagnets [32] or synthetic antiferromagnets (SAFs) [33–35], which are promising for hosting sub-10-nm skyrmions at room temperature. Since the skyrmion Hall effect is (largely) suppressed in such systems [34], new schemes to realize skyrmion logic gates are in demand. Furthermore, no skyrmionic MUX logic device has been proposed yet.

In this paper, we propose a skyrmionic AND-OR logic device and two types of skyrmionic MUX logic device, which differ in the manner in which skyrmion motion is achieved, to implement SC. In the skyrmionic AND-OR logic device, which acts as a stochastic multiplier [36], skyrmions are driven by the spin-orbit torque (SOT) [37,38] and guided by the voltage-controlled-magnetic-anisotropy (VCMA) effect [39,40]. As a consequence, it is not necessary to accurately control skyrmion collisions to implement logic operations, and this device can tolerate thermal diffusion at $T = 250$ K. In the skyrmionic MUX logic devices, operating as stochastic adders [36], skyrmions can be moved by the Zhang-Li torque [41] or the SOT. VCMA or voltage-controlled DMI (VCDMI) [42] is used to dynamically modify the energy landscape to regulate skyrmion motion in these devices. Based on the proposed logic devices, the functionality of a 3-bit SN

stochastic multiplier and stochastic adder is confirmed by micromagnetic simulations. We also demonstrate that our proposed skyrmionic logic devices can work in a SAF, where no skyrmion Hall effect exists, and small magnetic skyrmions can be stabilized at room temperature. The performance of the proposed skyrmionic logic devices in FM materials and SAFs is analyzed, and shows good prospects for the use of these devices in implementing SC.

II. SKYRMIONIC AND-OR LOGIC DEVICE

In the proposed structure shown in Fig. 1(a), the skyrmionic AND-OR device is composed mainly of three parts, including a heavy-metal (HM) layer, a FM layer, and two voltage-electrode gates. The HM layer, which is beneath the FM layer and is not shown in the figure, is used for the flow of a driving current to drive skyrmions from the left to the right side by means of the spin Hall effect (SHE) [43]. We apply positive voltages to electrode gates 1 (V_{g1}) and 2 (V_{g2}) [see Fig. 1(b)], increasing the potential energy of the FM layer beneath gates 1 and 2 to guide the skyrmion motion. The effect of the voltage on the perpendicular magnetic anisotropy (PMA) can be calculated from the equation $K_g = K_u + \xi V_g/(dh)$, where the VCMA coefficient ξ is set to 48 fJ V^{-1} m^{-1} according to previous
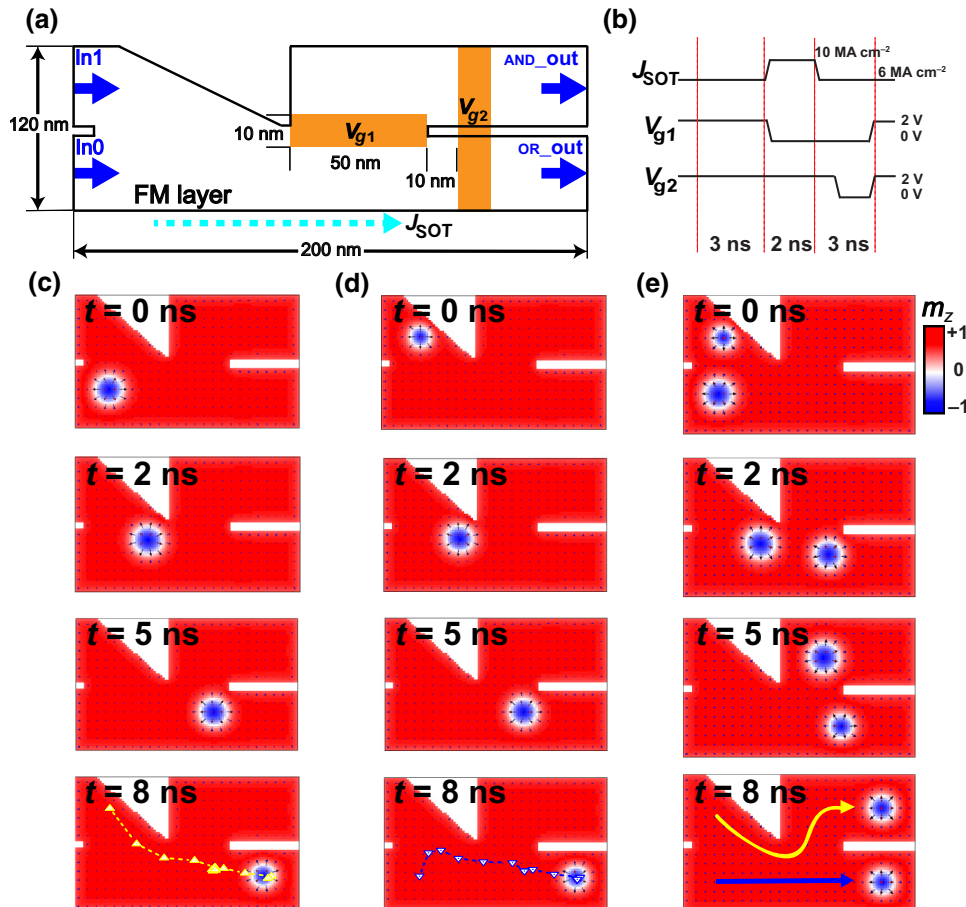

FIG. 1. Skyrmionic AND-OR logic device at $T = 0$ K. (a) Device structure with two input lanes and two output lanes. The two electrode gates (with voltages V_{g1} and V_{g2}) are designed to modulate skyrmion motion through the VCMA effect. (b) Profile of driving current density (J_{SOT}) and positive voltages applied to achieve device function. (c)–(e) Three cases of inputs and their corresponding simulated processes and outputs. In the snapshots of the micromagnetic simulations, the color red represents spin up ($m_z = +1$), blue represents spin down ($m_z = -1$), and white represents spins that are horizontal in the plane ($m_z = 0$). Skyrmion trajectories are indicated in the magnetization snapshots at $t = 8$ ns.
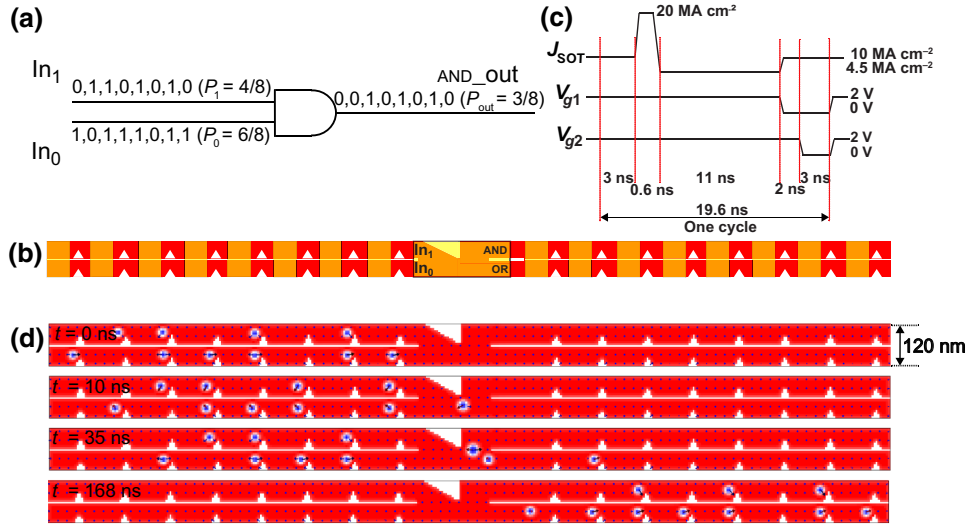
FIG. 2. 3-bit skyrmionic AND-OR logic device used as a stochastic multiplier. (a) Schematic illustration of exact computation of the multiplication $4/8 \times 6/8 = 3/8$. A logic AND gate is required during the operation. (b) Schematic illustration of the proposed 3-bit skyrmionic stochastic multiplier. Notches are used to divide each lane into eight regions and synchronize the motion of skyrmions. (c) Profile of driving current density (J_{SOT}) and electrode voltages in an operation cycle. (d) Snapshots of magnetization configuration of the 3-bit stochastic multiplier at selected times. At $t = 0$ ns, the skyrmions distributed in the two input lanes represent probabilities $P_1 = 4/8$ and $P_0 = 6/8$. After 168 ns, the AND lane outputs the binary sequence "0, 0, 1, 0, 1, 0, 1, 0," i.e., a probability $P_{\mathrm{out}} = 3/8$, which denotes the result of multiplication of the two inputs.

reports [40]. d denotes the thickness of the insulator layer between the electrode gates and the FM layer, and h is the thickness of the FM layer; these are both set to 1 nm in our simulations. Precisely, if a voltage of $+2$ V is applied to one electrode gate, the PMA of the FM layer beneath it increases from 0.8 to 0.896 MJ m^{-3}, creating an energy barrier that blocks skyrmions from crossing this region (see Appendix A for other details of the simulations).

Figure 1(b) shows the profile of the SOT current density (J_{SOT}) and the electrode voltages required to achieve device function. Voltages V_{g1} and V_{g2} of $+2$ V are dynamically applied to guide the skyrmion motion. Figures 1(c)–1(e) show top-view simulation snapshots for three different inputs. Data values "1" and "0" are encoded by the presence or absence (FM background) of a skyrmion. In the circumstance of only one skyrmion input, this skyrmion enters the OR lane and is blocked at a position near gate 2 under the joint effect of VCMA, the application of $J_{\mathrm{SOT}} = 6$ MA cm^{-2} for 3 ns, and repulsion from the edge [21,22]. After the positive voltage V_{g2} is removed, the skyrmion is finally output from the OR lane. Therefore, the OR and AND lane generate outputs of "1" and "0," respectively. In the case of two skyrmion inputs, the first skyrmion (from In$_0$) stops near gate 2, similarly to the aforementioned behavior. The subsequent skyrmion (from In$_1$) is then blocked because of repulsion from the first skyrmion and the energy potential caused by V_{g1}. At $t = 3$ ns, the voltage V_{g1} is set to 0, and J_{SOT} increases to 10 MA cm^{-2}. Thus the subsequent skyrmion is driven to the AND lane by the combined effect of the skyrmion

Hall effect [23–27], skyrmion-skyrmion repulsion, and skyrmion-edge repulsion, while the first skyrmion moves out from the OR lane after the voltage V_{g2} returns to 0. In this case, both the OR and the AND lane give rise to the output of the data value "1." Obviously, an AND-OR logic function is realized in our proposed device. Note that during these operations, it is not necessary to control skyrmion-skyrmion collisions precisely. However, in previous proposals [6,7], this is required to realize logic functions, which suffer from instability in the presence of thermal effects and pinning. We verify the function of the proposed AND-OR logic device at $T = 250$ K (see Appendix B for details), indicating the operational robustness of our device.

Moreover, we design a 3-bit stochastic multiplier (where the length of the stochastic bit stream is 8), using the proposed skyrmionic logic AND-OR device as a stochastic-multiplier cell. Figure 2(a) shows a schematic illustration of the computation of the multiplication $4/8 \times 6/8$ implemented by an AND logic gate, which can be physically achieved in our proposed skyrmionic device as exhibited in Fig. 2(b). The AND function is implemented using the above skyrmionic logic AND-OR device, while the inputs and outputs can be stored in the corresponding elongated lanes. Notches in the lanes are used to synchronize the input and output skyrmions, and divide each lane into eight regions [yellow regions in Fig. 2(b)]. Through periodically increasing the current to $J_{\mathrm{SOT}} = 20$ MA cm^{-2} for 0.6 ns, skyrmions can be moved to the region of the next data bit [7]. Otherwise, the skyrmions are blocked in their

original area. An operation-timing diagram of the AND-OR logic operation in one cycle is shown in Fig. 2(c). Compared with the timing diagram in Fig. 1(b), an additional 0.6-ns-wide high-current pulse is provided every 19.6 ns to synchronize the skyrmions, which means that the whole operation time for computing a 3-bit multiplication is about 156.8 ns. In our simulations, the input skyrmions are initialized in the left racetracks. There are four and six skyrmions distributed in the two input lanes, denoting two probabilities $P_1 = 4/8$ and $P_0 = 6/8$, respectively. Note that the skyrmion nucleation time is not considered in our simulations, as recent studies have shown that skyrmions can be generated in approximately 0.6 ns by SOT pulses [9]. More interestingly, the input skyrmion stream can also be provided through a reshuffler device with a skyrmionic reservoir [44], in which the skyrmions are generated asynchronously. Therefore, the skyrmion nucleation time does not bound the clock speed of the whole system. After eight cycles, three skyrmions are output from the AND lane, as shown in Fig. 2(d), which illustrates an output probability $P_{out} = 3/8$ and the capability of our device to perform stochastic multiplication.

III. SKYRMIONIC MUX LOGIC DEVICE

The addition operation in SC can be performed by a MUX [36], where two input bit streams (In$_1$, In$_0$) are selected by a select signal S with a probability of 0.5, and thus the output bit stream has a probability of half the sum of the two inputs. Making use of the particlelike behavior of skyrmions, we propose two types of skyrmionic MUX logic device, which differ in the manner in which skyrmion motion is achieved.

Figure 3(a) shows one scheme for implementing MUX logic, which is based on the deflection of skyrmions at an interface between regions with different DMIs. The DMI constant D_1 on the left side is set to 3.5 mJ m^{-2}, while D_2 for the right plane varies from 3.35 to 3.65 mJ m^{-2}. The skyrmion deflection direction depends on the relative magnitudes of D_1 and D_2. Specifically, in our setting, if $D_2 > D_1$, skyrmions are deflected along the $+y$ direction. Therefore, skyrmions from In$_0$ enter the OUT lane, while skyrmions from In$_1$ are output from the terminal above the OUT lane, which means that data from In$_0$ are selected. In contrast, if $D_2 < D_1$, skyrmions from In$_1$ enter the OUT lane, while skyrmions from In$_0$ are crushed at the lower edge. By regulating D_2 using the VCDMI effect according to an electronic select signal S to select two skyrmionic input signals, MUX logic can be implemented in our device. Note that the skyrmions here are driven by Zhang-Li torque, i.e., spin transfer torque (STT) delivered by an in-plane current (CIP) that is applied directly in the FM layer rather than the HM layer. Besides, when the skyrmions cross the interface where the DMI changes, the applied current J_{STT} maintains its value of 15 MA cm^{-2} [see Fig. 3(b)]. If the current density is too high, the skyrmions pass quickly through the interface, leading to a small displacement along the y direction that is not enough to realize the required function.

However, this scheme has several shortcomings. First, the stability and power efficiency are affected by the crushing of skyrmions. Second, deflection toward the $-y$ direction at the interface can be achieved only when the skyrmions are driven by the Zhang-Li torque (see Appendix C for simulation results for the SOT-driven case and the Discussion for an explanation), which consumes more energy and time than in the SOT-driven case. In addition, the skyrmion displacement in the y direction is inversely proportional to the damping [45], which indicates that the damping should be relatively low (a damping
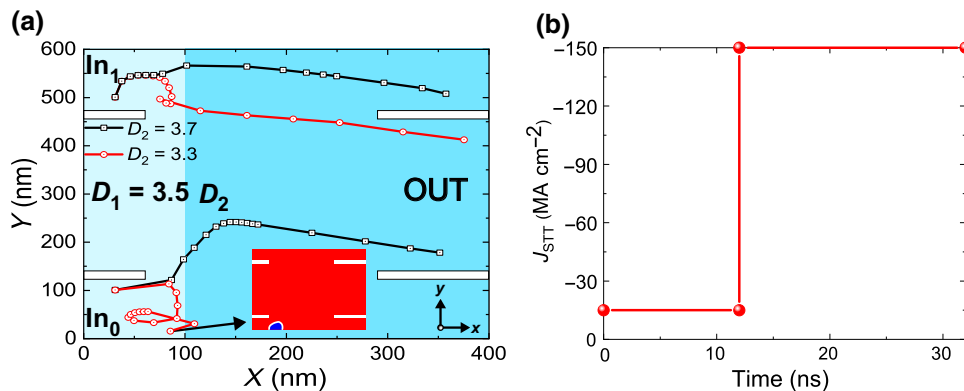

FIG. 3. Skyrmionic MUX logic device driven by Zhang-Li torque. (a) Schematic illustration of the proposed device, where the DMIs in the left panel (D_1) and right panel (D_2) are different. There are two input lanes (In$_0$, In$_1$), and one output lane (OUT) to export the selected data. Trajectories of skyrmions are indicated by the black and red symbols for $D_2 = 3.35$ and 3.65 mJ m^{-2}, respectively, while D_1 is fixed at 3.5 mJ m^{-2}. (b) Profile of driving in-plane-polarized current J_{STT}. A damping $\alpha = 0.1$ is used in the simulations for (a) to obtain a large enough skyrmion deflection.
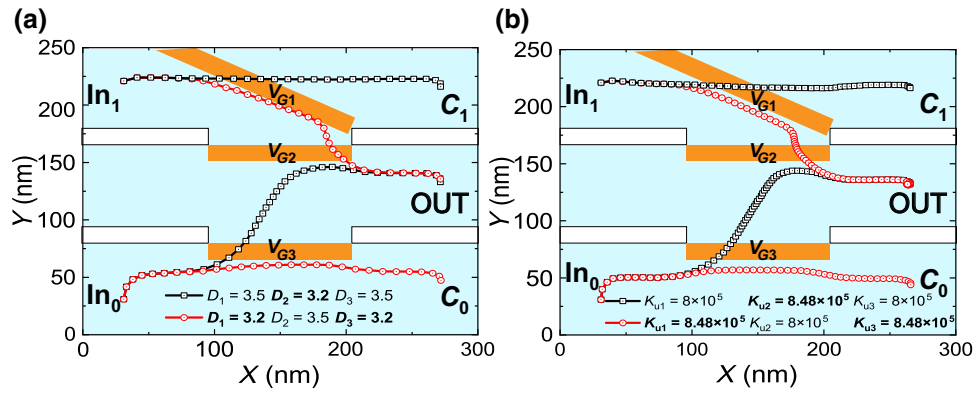
FIG. 4. Skyrmionic MUX logic devices driven by SOT. Schematic illustration of the proposed devices where the energy landscape is dynamically changed through (a) the VCDMI effect and (b) the VCMA effect. Three electrode gates (with voltages V_{G1}, V_{G2}, and V_{G3}) and an oblique interface are introduced to guide skyrmion motion. Trajectories of skyrmions when data are selected from different lanes are indicated by the blue and red symbols. The J_{SOT} applied in (a) and (b) is 6.1 MA cm^{-2} and 4.0 MA cm^{-2}, respectively.

$\alpha = 0.1$ is used in our simulations) to enable sufficient displacement. But, in the widely studied Pt/Co system, the damping is usually larger than 0.1 [46].

Therefore, we propose another scheme for a skyrmionic MUX logic device where skyrmions are driven by the SOT. In addition, there are two copy lanes (C_1, C_0), outputting the data that is not selected by S. As shown in Fig. 4(a), an oblique interface is introduced to guide the skyrmion motion. Three electrode gates (with voltages V_{G1}, V_{G2}, and V_{G3}) are used to lower the DMI value of the FM layer beneath the electrode gates through the VCDMI effect [40]. The voltages V_{G1} and V_{G3} are always the same, and are used to select the input skyrmion from In$_1$. In contrast, a voltage different from V_{G1} and V_{G3} is applied to gate 2 to select a skyrmion from In$_0$. The select signal S can be produced electronically by a stochastic number generator (SNG) [47] where the probability of "1" is 0.5, as done in our simulations. S can also be produced by skyrmionic devices or a SNG based on a superparamagnetic magnetic tunnel junction [48,49]. Recently, energy-efficient SC has been demonstrated via superparamagnetic magnetic tunnel junctions [50]. The optimal approach is to utilize a stochastic skyrmion stream that already exists in the stochastic computing system, such as the output bit streams in Fig. 2(d), to achieve an "all-skyrmionic" implementation; however, this needs further investigation. When the random number from S is 0, D_2 decreases to 3.2 mJ m^{-2}, creating a high energy barrier to guide skyrmions from In$_0$ to enter the OUT lane. In the meantime, D_1 and D_3 remain unchanged (at the default value $D = 3.5$ mJ m^{-2}). Therefore, skyrmions from In$_1$ are output from C_1. When the random number is 1, only gates 1 and 2 are selected, lowering D_1 and D_3 to 3.2 mJ m^{-2} simultaneously. Therefore, skyrmions from In$_1$ eventually move to the OUT lane, while skyrmions from In$_0$ are blocked by gate 3 and enter the C_0 lane. The trajectories of skyrmions

under different circumstances are explicitly shown in Fig. 4(a).

During the operation, the 0.3 mJ m^{-2} difference in the DMI can sustain a maximum current density of $J_{SOT} = 6.1$ MA cm^{-2}. If the current is higher, skyrmions from In$_1$ go through the region of gate 1 and enter the C_1 lane, leading to the wrong logic output. In addition to the VCDMI effect, the VCMA effect can also be used to change the local potential energy. Figure 4(b) shows a schematic illustration of a skyrmionic MUX device using VCMA. Similarly to Fig. 4(a), three voltage gates are placed to modify the energy landscape in the device. In our simulations, we apply a voltage of $+1$ V to the electrode gates to increase the local PMA energy density from 0.8 to 0.848 MJ m^{-3}. In this case, the maximum current density is $J_{SOT} = 3.0$ MA cm^{-2}, otherwise skyrmions will enter the wrong lanes. Materials with a higher VCMA coefficient for higher voltages can be used to improve the device speed.

Based on the MUX device using VCMA, we design a 3-bit stochastic adder. Figure 5(a) shows a schematic illustration of a computation of the exact addition $(1/2)(7/8 + 3/8)$ performed by a MUX device. The structure of the proposed 3-bit skyrmionic stochastic adder is shown in Fig. 5(b). Following the timing diagram in Fig. 5(c), the proposed skyrmionic MUX logic device can select skyrmions from In$_1$ or In$_0$ depending on the sequence S produced by the SNG. Similarly to the 3-bit stochastic multiplier, a high current $J_{SOT} = 10$ MA cm^{-2} is applied for 2.2 ns every 17.2 ns to enable skyrmions to cross the notches and to synchronize the skyrmions. Therefore, the time required to complete the 3-bit MUX logic is 137.6 ns. Figure 5(d) shows snapshots of the magnetization configuration at selected times. We can see that there are five skyrmions in the OUT lane, denoting a probability $P_{out} = 5/8$, which is exactly the half sum of the two input probabilities $P_1 = 7/8$ and $P_0 = 3/8$.
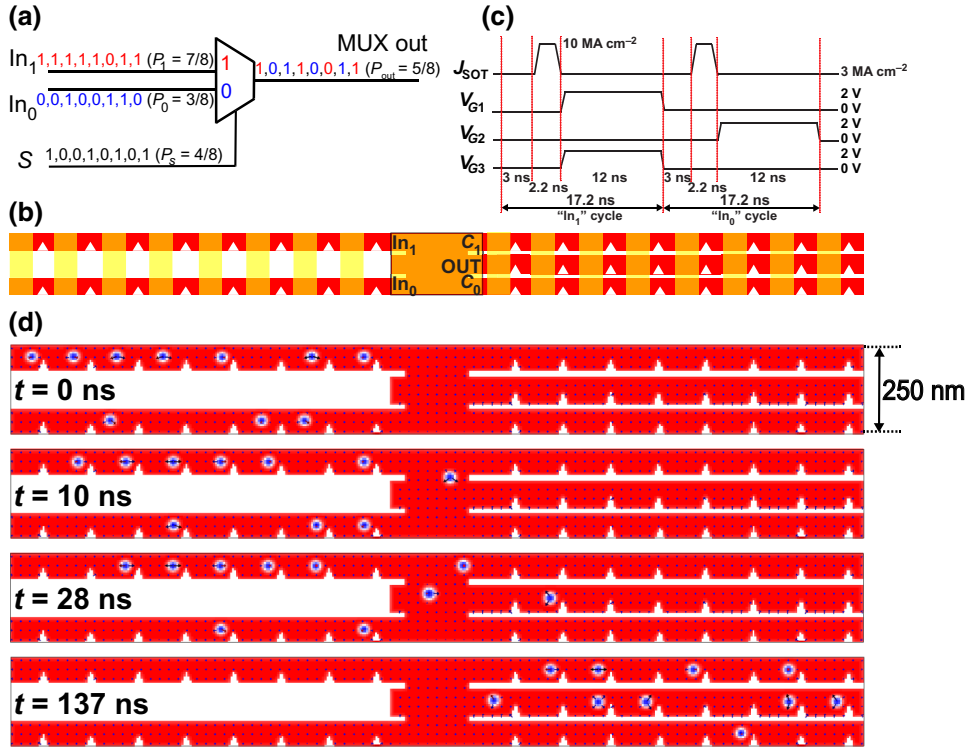
FIG. 5. 3-bit skyrmionic MUX logic device used as a stochastic adder. (a) Schematic illustration of the exact computation of the addition $(1/2)(7/8 + 3/8) = 5/8$ implemented by a MUX device. (b) Schematic illustration of the proposed 3-bit stochastic adder. (c) Profile of driving current density (J_{SOT}) and voltages applied to the three electrode gates (V_{G1}, V_{G2}, and V_{G3}) in an operation cycle. (d) Snapshots of magnetization configuration of the 3-bit stochastic multiplier at selected times. At $t = 0$ ns, the skyrmions distributed in the two input lanes represent probabilities $P_1 = 7/8$ and $P_0 = 3/8$. After 137 ns, the OUT lane outputs the binary sequence "1, 0, 1, 1, 0, 0, 1, 1", i.e., a probability $P_{\mathrm{out}} = 5/8$, which denotes half the sum of the two inputs.

IV. DISCUSSION

A. Skyrmion dynamics at an interface where the DMI changes

To understand the skyrmion dynamics in the two proposed MUX logic devices, we investigate the trajectories of skyrmions driven by the Zhang-Li torque and the SOT based on the Thiele equation, which assumes that the skyrmions are rigid during steady motion.

We first analyze the dynamics of skyrmions driven by the Zhang-Li torque. The Thiele equation for this case reads [51]

$$\mathbf{G} \times (\mathbf{v} - \mathbf{u}) - \alpha D \mathbf{v} + \mathbf{F}_i = 0. \quad (1)$$

Here, $\mathbf{G} = (0, 0, G)$ is the gyromagnetic coupling vector, where $G = (M_s t_F / \gamma) 4\pi Q$, with the saturation magnetization being M_s, the FM layer thickness t_F, the gyromagnetic ratio γ, and the skyrmion number $Q = -(1/4\pi) \iint \mathbf{m} \cdot [(\partial \mathbf{m}/\partial x) \times (\partial \mathbf{m}/\partial y)] dS$; $\mathbf{v} = (v_x, v_y, 0)$ is the motion velocity of the skyrmion; $\mathbf{u}$ is a vector along the direction of electron motion, with amplitude u; α is the damping constant; $D = (M_s t_F / \gamma) \iint (\partial \mathbf{m}/\partial x)^2 dS$ is the dissipative force; and $\mathbf{F}_i = -\nabla V(\mathbf{r})$ is the force induced by the interface where the DMI changes, with $V(\mathbf{r})$ denoting the system energy when a skyrmion is located at position $\mathbf{r}$. Assuming that we apply an in-plane current along the $-x$ direction and the interface is exactly along the y direction as shown in Fig. 3(a), the solution to Eq. (1) is

given by

$$\begin{cases} v_x = \frac{\alpha D F_i + G^2 u}{G^2 + (\alpha D)^2}, \\ v_y = \frac{G(F_i - \alpha D u)}{G^2 + (\alpha D)^2}, \end{cases} \quad (2)$$

where F_i denotes the magnitude of the force $\mathbf{F}_i$.

If $D_1 = D_2$ or the skyrmions are far away enough from the interface, we can set $F_i = 0$ in Eq. (2). As a consequence, we obtain $v_x = G^2 u/[G^2 + (\alpha D)^2]$ and $v_y = -\alpha D G u/[G^2 + (\alpha D)^2]$. This result illustrates that skyrmions gain a velocity along the $+x$ direction in this case, which is a feature of domain-wall dynamics driven by the Zhang-Li torque. In contrast, whether skyrmions move toward the $+y$ or $-y$ direction depends on the sign of the skyrmion number Q. In our simulations, we get $Q = 1$ because the magnetization of the background FM layer points along the $+z$ direction. Therefore, v_y is negative, which agrees with the trajectories shown in Fig. 3(a). Further, the skyrmion Hall angle θ_{sk}, which describes the deviation of skyrmions from the x direction, is given by $\theta_{\mathrm{sk}} = \mathrm{atan}(v_y/v_x) = -\mathrm{atan}(\alpha D/G)$. If the skyrmion radius R is larger than the domain-wall width Δ, θ_{sk} can be simplified well enough to $-\mathrm{atan}(\alpha R/2\Delta)$ [52]. Taking the parameters used in Fig. 3(a), θ_{sk} is estimated as $-16°$, corresponding well to the simulation results. When $D_1 \neq D_2$ and the skyrmions are near the interface, F_i cannot be left out in Eq. (2). As illustrated later in Fig. 7(c), F_i is positive if $D_1 < D_2$, and vice

versa. From the expression for v_y, we can see that the skyrmion deflection can be changed by varying the magnitudes of F_i and αDu. Once $D_1 < D_2$ and $F_i > \alpha Du$, the skyrmions move toward the $+y$ direction. Otherwise, the skyrmions still bend over toward the $-y$ direction. Our first proposed MUX logic device is based on exactly this property.

In contrast, the Thiele equation for the SOT-driven case reads [43]

$$\mathbf{G} \times \mathbf{v} - \alpha D\mathbf{v} + \mathbf{F}_{\text{SHE}} + \mathbf{F}_i = 0, \qquad (3)$$

where $\mathbf{F}_{\text{SHE}} = F_{\text{SHE}}\hat{x}$ is the force induced by the SOT, with magnitude F_{SHE}, the sign of which depends on the spin polarization direction $\boldsymbol{\sigma}$. Solving Eq. (3), we find

$$\begin{cases} v_x = \dfrac{\alpha D(F_{\text{SHE}} + F_i)}{G^2 + (\alpha D)^2}, \\ v_y = \dfrac{G(F_{\text{SHE}} + F_i)}{G^2 + (\alpha D)^2}. \end{cases} \qquad (4)$$

If $D_1 < D_2$, F_{SHE} and F_i are both positive, and thus the skyrmion Hall angle is given by $\theta_{\text{sk}} = \text{atan}(v_y/v_x) = \text{atan}(G/\alpha D)$, which means that skyrmions can bend only toward the $+y$ direction when approaching the interface from In_0 or In_1. According to the expression for θ_{sk}, the skyrmion Hall effect should be remarkable in the SOT-driven case, agreeing well with the trajectories in Fig. 4(a). If $D_1 \geq D_2$, $F_{\text{SHE}} + F_i = 0$ can be achieved when the skyrmions gradually approach the interface. Thereafter the skyrmions remain static, as indicated in Fig. 7(a) later. Therefore, in the MUX logic device displayed in Fig. 3(a), where the interface is along the y direction, only the Zhang-Li torque can be used to realize the required function.

If an oblique interface is introduced, as is the case in Fig. 4(a), $\mathbf{F}_i$ can be expressed as $\mathbf{F}_i = (F_{ix}, F_{iy}, 0)$. Therefore, the solution to Eq. (3) becomes

$$\begin{cases} v_x = \dfrac{\alpha D(F_{\text{SHE}} + F_{ix}) - GF_{iy}}{G^2 + (\alpha D)^2}, \\ v_y = \dfrac{G(F_{\text{SHE}} + F_{ix}) + \alpha DF_{iy}}{G^2 + (\alpha D)^2}. \end{cases} \qquad (5)$$

To guide the skyrmions so that they move along the interface, we must have $F_{\text{SHE}} > 0$, $F_{ix} < 0$, and $F_{iy} < 0$, i.e., $D_1 > D_2$. Assuming that the interface makes an angle δ with the $-y$ direction, we have $k = \tan(\delta) = -(v_x/v_y) = (F_{iy}/F_{ix})$. Then, we can obtain

$$F_i = -\frac{\alpha D + kG}{\alpha D\sqrt{1 + k^2}}F_{\text{SHE}}. \qquad (6)$$

Therefore, we can guide the skyrmion motion along a designed interface when an appropriate SOT current is applied. Since F_i can also be generated at an interface where the PMA changes, the VCMA effect can be used to realize a similar function, as shown in Fig. 4(b). Note that if the applied SOT current is too strong, the F_i provided by the interface may fail to satisfy Eq. (6). In this circumstance, skyrmions can pass through the electrode-gated region, resulting in a wrong output.

B. Performance evaluation of SC implemented with skyrmionic logic devices

As shown above, we can implement SC with skyrmionic logic devices. We now evaluate the performance of skyrmionic logic devices. The energy consumption of the elementary skyrmionic AND-OR and MUX logic gates is 7.19 and 7.29 fJ, respectively (see Appendix D for the method of calculation of the energy consumption), while the time delays are 8 and 15 ns, respectively. The synchronization clock times of the 3-bit stochastic multiplier and adder are 19.6 and 17.2 ns, respectively, which indicates a time for the whole operation of about 20 μs if the stochastic number is 10. From the point of computing, a skyrmion lifetime of approximately 1 ms may be sufficient. But it is still necessary to enhance the thermal stability of the skyrmions if the stochastic number is increased or we utilize these skyrmions for storage in the meantime.

The device performance can be further optimized via adopting advanced materials such as ferrimagnets [32] and SAFs [33], where the skyrmion velocity can be much enhanced. For example, our simulations of devices in a SAF (see Appendix E) show that the energy consumption of the proposed skyrmionic logic devices can be reduced by about 2 times with nearly the same operation speed. It is also confirmed that the proposed skyrmionic logic gates can be achieved without the skyrmion Hall effect, differently from previous proposals.

Regarding the area, the device area depends on the skyrmion size. For the parameters used in our simulations, which mimic the Pt/Co system, the diameter of a skyrmion is approximately 20 nm. Though skyrmions of this size may encounter thermal-stability issues in ferromagnetic thin films (for example, researchers have identified only skyrmions of size approximately 100 nm in Pt/Co/MgO at room temperature [53]), skyrmions as small as 20–30 nm in radius have been found in Pt/Co-based synthetic anti-ferromagnets even at $T = 420$ K [33], where the thermal stability of skyrmions can be enhanced by increasing their volume while the demagnetization field is cancelled in the system [31,33–35]. Micromagnetic simulations further predict the potential of such a system to host sub-10-nm skyrmions at room temperature [33]. The parameters adopted in this paper correspond to a practical material system that could be used to realize skyrmionic logic gates. In the meantime, a recent study has demonstrated

skyrmions with a diameter as small as approximately 1 nm [3]. Though such small skyrmions have been identified only at low temperature, the huge progress made during the past ten years in stabilizing small skyrmions at room temperature, even with sizes below 10 nm [32], indicates that smaller skyrmions can be anticipated, and there is still much room or potential for improvement in device area and power consumption.

In addition, owing to the nonvolatility of skyrmions, there is no static power consumption for skyrmionic logic devices, while that for a CMOS AND gate is approximately 0.9 nW [54], resulting in non-negligible energy waste in the static state. In addition to driving skyrmions in an electrical manner, magnonic [55] and/or caloritronic [56] driving methods may open up feasible avenues for transferring our work to applications, but this is beyond the scope of this paper, and details will be omitted here. Therefore, although more effort is required, our proposed skyrmionic logic design demonstrates good prospects as an alternative way to implement SC.

V. CONCLUSION

In this paper, we propose a skyrmionic AND-OR logic device and two types of skyrmionic MUX logic device to implement SC. Thanks to an energy landscape designed by use of the VCMA or VCDMI effect, precise control of skyrmion-skyrmion collisions is not required in our devices, thus enabling high operational robustness. Based on these devices, we demonstrate a 3-bit stochastic multiplier and adder. Performance evaluation shows that our proposed skyrmionic logic devices are promising for executing SC in terms of energy consumption, time delay, and area with advances in materials. The work presented here reveals the great potential of skyrmionic logic devices for implementing SC.

APPENDIX A: SIMULATION METHODS

Micromagnetic simulations are performed by utilizing the GPU-accelerated simulation software package Mumax3 [57]. The dynamics at each site are depicted by the following Landau-Lifshitz-Gilbert equation [4,43]:

$$\frac{\partial \mathbf{m}}{\partial t} = -\gamma \mu_0 (\mathbf{m} \times \mathbf{H}_{\text{eff}}) + \alpha \left(\mathbf{m} \times \frac{\partial \mathbf{m}}{\partial t} \right) + \tau_{\text{SOT}} + \tau_{\text{CIP}},$$

where H_{eff} is the effective field, including contributions from the anisotropy field, exchange field, DMI field, demagnetization field, and thermal field (when $T \neq 0$ K). $\mathbf{m} = \mathbf{M}/|M_s|$ is the reduced magnetization, with M_s being the saturation magnetization, α the damping constant, γ the gyromagnetic ratio, and μ_0 the vacuum magnetic permeability. $\tau_{\text{SOT}} = \gamma (J_{\text{SOT}} \theta_{\text{SH}} \hbar/2edM_s)(\mathbf{m} \times \boldsymbol{\sigma} \times \mathbf{m})$ denotes the SOT exerted on the magnetization when a SOT current J_{SOT} is applied, where $\boldsymbol{\sigma}$ is the spin polarization direction, θ_{SH} is the spin Hall angle, e is the elementary charge, d is the thickness of the FM layer, and $\hbar$ is the reduced Planck constant [43]. $\tau_{\text{CIP}} = u[\mathbf{m} \times (\partial \mathbf{m}/\partial x) \times \mathbf{m}]$ is the Zhang-Li torque exerted when an in-plane-polarized current is applied, where $u = \gamma (J_{\text{STT}} P \hbar/2eM_s)$, with J_{STT} being the current density and P the spin polarization [41,43].

Unless specified, the following material parameters are adopted in our simulations: exchange stiffness $A = 15$ pJ m^{-1}, Gilbert damping $\alpha = 0.3$, saturation magnetization $M_s = 580$ kA m^{-1}, spin polarization $P = 0.4$, spin Hall angle $\theta_{\text{SH}} = 0.4$, PMA constant of the FM layer $K_u = 0.8$ MJ m^{-3}, DMI constant $D = 3.5$ mJ m^{-2}, and VCMA coefficient $\xi = 48$ fJ V^{-1} m^{-1} [34,35,40]. The simulation area is divided into a cubic grid of size 2 nm $\times$ 2 nm $\times$ 1 nm.

APPENDIX B: SKYRMIONIC AND-OR FUNCTIONS PERFORMED AT $T = 250$ K

We enlarge the area of the device and adjust the timing diagram [see Figs. 6(a) and 6(b)] to enable fluctuations of the skyrmions because of the high operational robustness of skyrmions in a wider racetrack [58]. Figures 6(c)–6(e) show the simulation results for different inputs. The volume of a skyrmion increases dramatically and fluctuates a lot at $T = 250$ K, which limits the current density that can be applied to drive the skyrmions. Basically, $J_{\text{SOT}} = 4.2$ MA cm^{-2} is applied to drive skyrmion motion, but a lower current is used ($J_{\text{SOT}} = 2.9$ MA cm^{-2}) when the second skyrmion moves to the AND lane. This is because the second skyrmion is more likely to be crushed at the edge while it is fluctuating at $T = 250$ K. The operation time becomes longer because of the larger size of the device as well as the lower driving current. But the AND-OR function can still be achieved, indicating the high operational robustness of our device.

APPENDIX C: SIMULATION RESULTS FOR SOT-DRIVEN SKYRMION MOTION AT AN INTERFACE WHERE THE DMI CHANGES

We investigate SOT-driven skyrmion motion at different interfaces where the DMI changes. A constant SOT current $J_{\text{SOT}} = 4$ MA cm^{-2} is applied along the $+x$ direction to drive skyrmion motion. As shown in Fig. 7(a), where
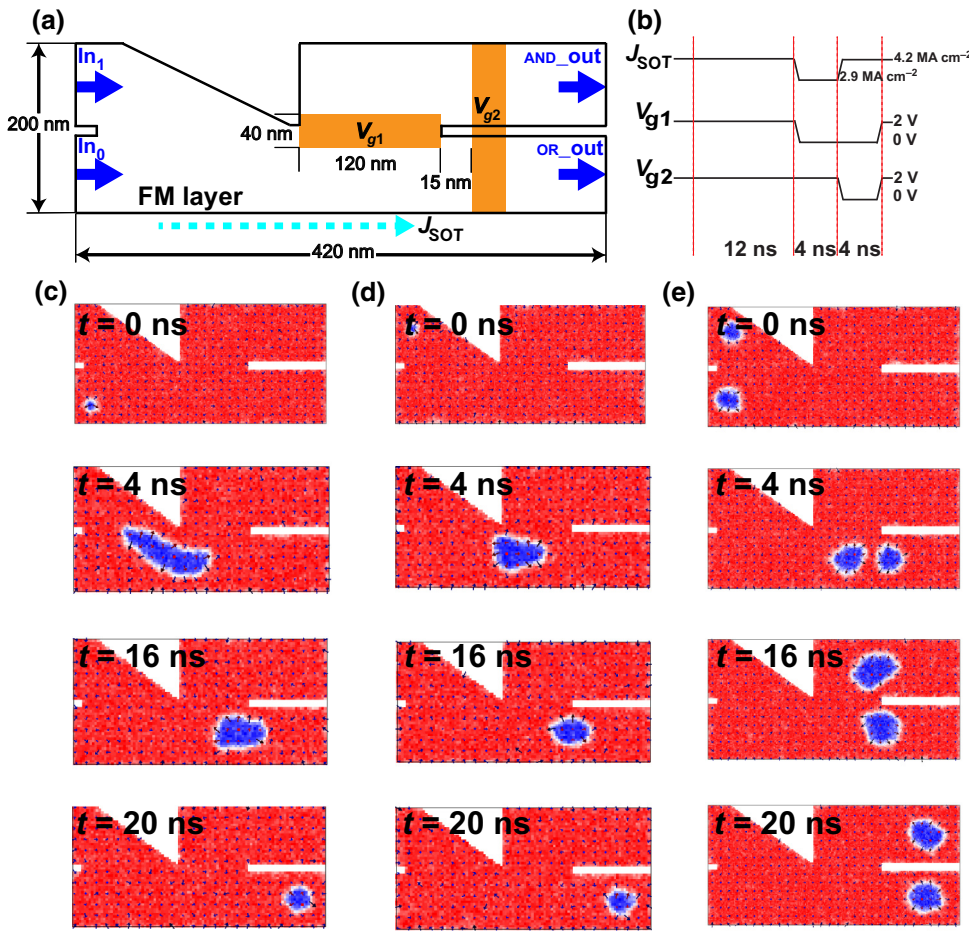
FIG. 6. Skyrmionic AND-OR logic device operated at $T = 250$ K. (a) Device structure, which is larger than the device in Fig. 1(a). (b) Profile of J_{SOT} and electrode voltages. (c)–(e) Three cases of inputs and the corresponding simulation process and results.

the interface is exactly along the y direction, the skyrmion deflection is along the $+y$ direction when $D_1 \leq D_2$. However, the skyrmions stop at the interface when $D_1 > D_2$. In contrast, in Fig. 7(b), we find that an oblique interface can guide skyrmions along the $-y$ direction, which can be utilized to perform the MUX function. We evaluate the effect of different DMIs on the potential energy. We initialize a skyrmion at the left side of the nanotrack shown in Fig. 7(c). Along this nanotrack, the DMI strength D increases from $3.2\,\mathrm{mJ\,m^{-2}}$ on the left side to $3.8\,\mathrm{mJ\,m^{-2}}$ on

the right side. Because of the DMI gradient, the skyrmion moves freely to the right side, and the energy is measured at each position. We can see that the potential energy in the region with the lower DMI is higher, which can be used to guide the motion of skyrmions. Besides, the energy difference between the two regions is nearly proportional to the difference in the DMI. By increasing the DMI difference between two adjacent regions, we can regulate the skyrmions in a more stable manner, and a higher current can be used to drive the skyrmions.
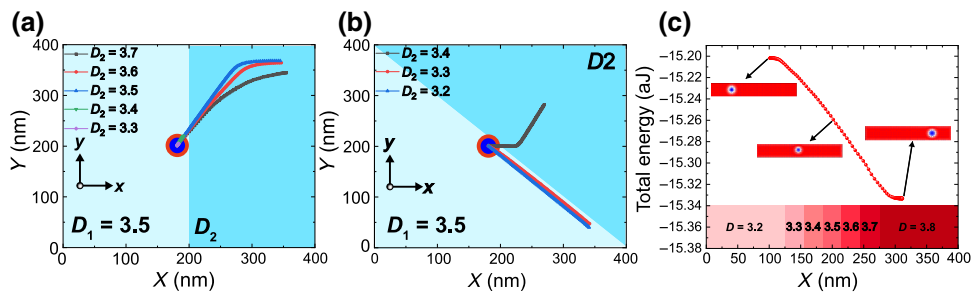

FIG. 7. (a),(b) Trajectories of a SOT-driven skyrmion for different values of D_2 when a y-direction or oblique interface is introduced. $D_1 = 3.5\,\mathrm{mJ\,m^{-2}}$ and $J_{SOT} = 4\,\mathrm{MA\,cm^{-2}}$. (c) Effect of DMI on the energy of a nanotrack system. The DMI strength increases from $3.2\,\mathrm{mJ\,m^{-2}}$ on the left side to $3.8\,\mathrm{mJ\,m^{-2}}$ on the right side, generating a force that drives the skyrmions along the $+x$ direction. At each position, the energy of the system is recorded.

TABLE I. Parameters of HM layer for AND logic operation.

J_i (MA cm^{-2})	S_{HM} (nm^2)	ρ (Ω m)	l (nm)	T_i (ns)
$i = 1$ 6	480	1.8×10^{-6}	2400	3
$i = 2$ 10	480	1.8×10^{-6}	2400	2
$i = 3$ 6	480	1.8×10^{-6}	2400	3

APPENDIX D: EVALUATION OF ENERGY CONSUMPTION

The energy consumed in the AND-OR and MUX logic operations is calculated from

$$W = J^2 S_{HM} \rho l T,$$

where J is the SOT current density flowing in the HM layer, S_{HM} is the y-z cross-sectional area of the HM layer, ρ is the resistivity of the HM layer [59], l is the length of the HM layer in the x direction, and T is the time duration. According to the time diagram shown in Fig. 1(b), different current densities J_i ($i = 1, 2, 3$) are applied for different time durations T_i. The corresponding parameters are listed in Table I. Note here that the capacitive charging and discharging energy of the VCMA gates is not included in the energy analysis, as this energy is generally negligible compared with the ohmic losses.

Therefore, the energy consumption of the AND-OR and MUX logic gates [Fig. 4(b)] is 7.19 and 7.29 fJ respectively, while their operation speeds are 8 and 15 ns, respectively. Following this method, the power consumption of the 3-bit stochastic multiplier and adder is evaluated as 1.264 and 1.224 pJ, respectively.

APPENDIX E: SIMULATION OF SKYRMIONIC LOGIC DEVICES IN A SAF

We also adopt trilayer SAF systems to improve the performance of our devices [34]. A trilayer SAF system consists of two FM layers that are antiferromagnetically exchange coupled through a nonferromagnetic spacer. The initial magnetization of the top FM layer is along $+z$, while that of the lower FM layer is along $-z$. Because there is no skyrmion Hall effect in such a system, we adjust the location of the electrodes based on our proposed MUX device as shown in Fig. 4, while the size remains unchanged. For the skyrmionic AND-OR logic device, we slightly extend the size along the x direction (from 200 to 240 nm) to get more space for skyrmion motion. The simulation results (Fig. 8) show that the skyrmions in the SAF system can move about 2 times faster than the skyrmions in the FM system given the same energy consumption. Similarly, the performance of the MUX logic gate is optimized as well in the SAF system. Although the DMI strength used in our simulations, which is also adopted in Refs. [34] and [35], is higher than that obtained in experiments [60], it
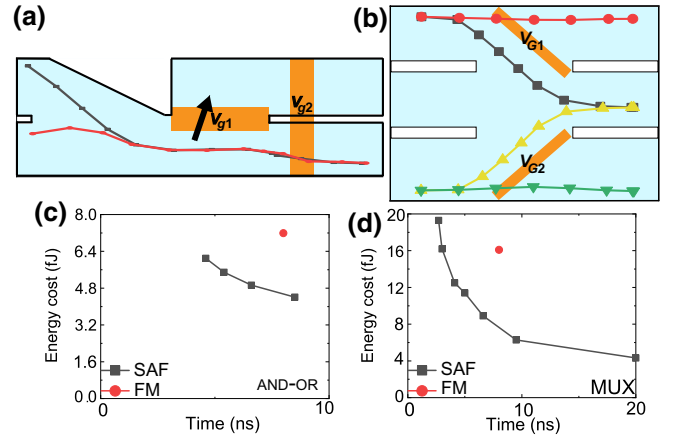

FIG. 8. (a),(b) Trajectories of skyrmions in skyrmionic logic devices in a SAF. (c),(d) Comparison of the energy cost and time delay of our skyrmionic logic devices between a SAF and a FM material.

could be optimized further in the long term. Besides, by increasing the number of layers in a SAF system, the DMI required to stabilize skyrmions with a size below 10 nm at room temperature can be made lower than $1 \, \text{mJ m}^{-2}$ [33], which further indicates the feasibility of our method. Therefore, our simulations of devices in a SAF show that our scheme corresponds to a practical material system, i.e., a Co-based synthetic antiferromagnet. It will also be interesting to demonstrate our schemes in ferrimagnets, another promising material system, where Büttner *et al.* [30] and Caretta *et al.* [32] have done much pioneering work.

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