Editors' Suggestion

Valley-Spin Logic Gates

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Valleytronics is an emerging field of research utilizing the valley-pseudospin degree of freedom. In this work, we propose to exploit spin-valley locking in two-dimensional materials, such as silicene, germanene, stanene, and 1T' transition-metal dichalcogenides, to realize the logic devices with multiple voltage-controlled gate contacts. These materials possess space-inversion and time-reversal symmetries and have two valleys at the non-time-reversal invariant momenta, K and K', related by time-reversal symmetry. Due to these properties, the valley-spin polarization in these materials can be switched by electric field, and the device conductance and the output voltage can be controlled by the polarity of the input gate voltage. Based on the explicit quantum-transport calculations, we demonstrate the realization of seven logic gates, namely NOT, XNOR, XOR, AND, NAND, OR, and NOR.

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I. INTRODUCTION

Spintronics exploits the spin degree of freedom in electronic devices [1,2]. Such devices have aroused considerable interest due to their nonvolatility, high integration densities, and low-power operation. Several spin-logic devices have been theoretically proposed [3–6] and experimentally demonstrated [7–10]. For example, Ney *et al.* [3] proposed a programmable spin logic based on a single magnetoresistive element whose inputs are represented by the input current directions, while the logic outputs are represented by the device resistance states. Dery *et al.* [4] reported a spin-logic gate based on a semiconductor structure with multiple magnetic contacts. The logic inputs are encoded in the magnetization directions, while the logic output is defined by a transient current response. Behin-Aein *et al.* [5] proposed all-spin logic, where input and output information is represented by the magnetization of nanomagnets that communicate through spin-coherent channels. Wan *et al.* [8] demonstrated spin-logic operations in magnetized trilayer Pt/Co/MgO via the spin Hall effect. Manipatruni *et al.* [9] proposed a scalable spintronic logic device that operates via spin-orbit transduction combined with magnetoelectric switching. Spin-logic gates were also theoretically proposed utilizing graphene nanoribbons [11] and molecular magnets [12] via the electrical control of spin-polarized current. Recently, spin-logic gates were also proposed utilizing a kagome spin ice [13] and polarized spin waves [14]. However, many of the proposed spin-logic gates suffer from a concatenation problem when integrated into circuits. Due to the logic input and output being encoded in different physical quantities [3,4,11,12], the logic output cannot be used as the input of the successive gate. Solving this problem is important for device cascading in integrated circuits.

More recently, valleytronics—a field of research based on exploitation and manipulation of the valley-pseudospin degree of freedom—has attracted great attention [15,16]. In addition to the rich valley physics [17,18], the valley pseudospin can be utilized to design promising valley-based devices. For example, in analogy to the spin-valve effect [19,20], the valley-valve effect, i.e., the change of electrical resistance between two values due to the valley-dependent transport, has been predicted in graphene nanoribbons [21,22] and WS_2/MoS_2 van der Waals heterostructures [23]. In addition, valley-based logic gates have been proposed in a quasi-two-dimensional (2D) system with merging Dirac cones, which reveal all-electric-controlled valley-filter and valley-valve effects [24].

Recently, we have proposed a valley-spin valve (VSV), which exploits the spin-valley locking in 2D materials, such as silicene, germanene, stanene, and 1T' transition-metal dichalcogenides [25]. These materials possess space-inversion and time-reversal symmetries and have two valleys at the non-time-reversal invariant momenta, K and K', related by time-reversal symmetry. The valley-spin polarization in these materials can be switched by an electric field, which enables functionalities of a valley-spin polarizer or a valley-spin analyzer. When placed in series, they constitute the VSV—a device whose conductance state is *on* or *off* depending on the relative valley-spin

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polarization of the polarizer and the analyzer [25]. In this work, we utilize the predicted giant VSV effect to design valley-spin logic gates, which enable various logic operations, such as NOT, XNOR, XOR, AND, NAND, OR, and NOR. Since both logic input and output are encoded by the polarity of voltage, the cascading is thus realized.

II. THEORETICAL FORMALISM

Without losing generality, we consider stanene as a representative channel material for the proposed devices. The low-energy tight-binding Hamiltonian is given by [26–28]

$$H = -t\sum_{\langle i,j\rangle\alpha} c^{\dagger}_{i\alpha}c_{j\alpha} + i\frac{\lambda_{SO}}{3\sqrt{3}}\sum_{\langle\langle i,j\rangle\rangle\alpha,\beta} \nu_{ij}c^{\dagger}_{i\alpha}\sigma_z^{\alpha\beta}c_{j\beta} + i\lambda_{R1}\sum_{\langle i,j\rangle\alpha,\beta} c^{\dagger}_{i\alpha}(\boldsymbol{\sigma}\times\hat{\mathbf{d}}_{ij})^z c_{j\beta} - i\frac{2\lambda_{R2}}{3}\sum_{\langle\langle i,j\rangle\rangle\alpha,\beta}\xi_i c^{\dagger}_{i\alpha}(\boldsymbol{\sigma}\times\hat{\mathbf{d}}_{ij})^z c_{j\beta} + lE_z\sum_{i\alpha}\xi_i c^{\dagger}_{i\alpha}c_{i\alpha}, \tag{1}$$

where the first term is the nearest-neighbor hopping, $c^{\dagger}_{i\alpha}$ ($c_{j\alpha}$) is an electron creation (annihilation) operator at the site i (j) with spin $\alpha=\uparrow,\downarrow$, t is the hopping parameter, and $\langle i,j\rangle$ denotes the sum over the nearest-neighbor sites. The second term represents the intrinsic spin-orbit coupling (SOC) with strength λ_{SO}, $\langle\langle i,j\rangle\rangle$ denotes the sum over the next-nearest-neighbor sites, σ_z is the z component of the Pauli matrix, and $\nu_{ij}=+1$ (–1) selects anticlockwise (clockwise) hopping with respect to the z axis. The third term represents the Rashba SOC induced by an external electric field, and the fourth term is the intrinsic Rashba SOC. Our previous work demonstrates that λ_{R1} is significantly smaller than λ_{SO}, and the intrinsic Rashba SOC (λ_{R2}) has a negligible effect [25]. Both Rashba terms are therefore ignored in this work. The last term arises from the applied electric field E_z, $\xi_i=+1$ (–1) distinguishes site $i=$ A (B), and 2 l is the buckling height. According to Eq. (1), when $\lambda_{R1}=\lambda_{R2}=0$, $[\sigma_z, H]=0$, and the spin component σ_z is a good quantum number. In the calculations, we use the tight-binding parameters: $t=1.3$ eV, $\lambda_{\mathrm{SO}}=0.1$ eV, and $l=0.4$ Å, appropriate for stanene [29].

Conductance G at energy E is calculated by using the Landauer-Büttiker formula [30]

$$G(E)=\frac{e^2}{h}\sum_{\sigma,k_y}T_{\sigma}(E,k_y), \tag{2}$$

where e the is electron charge, h Planck's constant, T_{σ} is the transmission for spin σ. k_y is the transverse Bloch wave vector, which is conserved in the transports process. For the numerical calculations, we set the gate width $d_1=40a$, separation distance $d_2=20a$ (where a is the lattice constant), the Fermi energy $E_F=0.01$ eV, and calculate G using 101 irreducible k_y points.

III. RESULTS AND DISCUSSION

Figure 1 shows the calculated band structure around the valleys K and K' for positive and negative E_z. Although the net spin polarization in the system is zero, the spin polarization around each valley is 100%. Importantly, such a valley-dependent spin polarization can be reversed by an electric field, which can be understood as follows. The band energies around the valleys are given by [27]

$$\varepsilon^{\pm}_{\eta s}=\pm\sqrt{3a^2t^2q_{\eta}^2/4+(\eta s\lambda_{\mathrm{SO}}-lE_z)^2}, \tag{3}$$

where $\eta=\pm1$ and $s=\pm1$ are valley and spin indices, respectively, and $q_{\eta}=|k-K_{\eta}|$ is the wave vector measured from the K (K') point. It is seen that the band energies are spin degenerate if either $E_z=0$ or $\lambda_{\mathrm{SO}}=0$. If both E_z and λ_{SO} are finite, the bands are spin split at the K (K') valley. From Eq. (3), $\varepsilon^{\pm}_{\eta\uparrow}=\varepsilon^{\pm}_{-\eta\downarrow}$; hence, the spin polarization is opposite between the K and K' valleys. In addition, $\varepsilon^{\pm}_{\eta\uparrow}(+E_z)=\varepsilon^{\pm}_{\eta\downarrow}(-E_z)$, and hence the polarity of the valley-dependent spin polarization can be switched by changing the sign of E_z.

Figure 2(a) schematically shows a prototype four-terminal building block for the design of XNOR and XOR gates. The device has a source and a drain connected by a 2D channel, whose transport properties are controlled by gates A and B. Positive and negative voltages on gates A and B are the logic inputs 1 and 0, respectively. As a result of the VSV effect [25], depending on the relative voltage polarities on gates A and B, the device conductance is high (*on* state) or low (*off* state). This is due to the spin and pseudospin (valley) conservation in the transport process, which makes the transmission high (low) when the gate polarities are the same (opposite), as illustrated in Fig. 2(b).

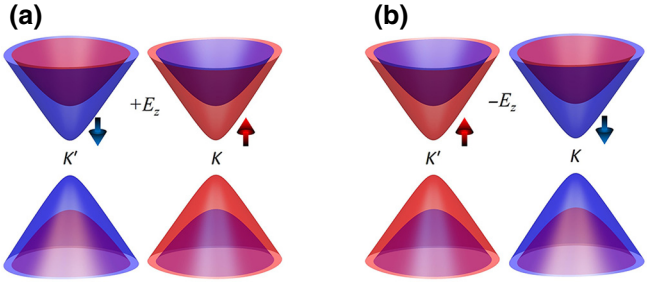

FIG. 1. Calculated band structure of stanene around the K and K' valleys for the electric field (a) $E_z=1.25$ V/nm and (b) $E_z=-1.25$ V/nm. Red and blue colors represent spin-up and spin-down branches, respectively. Arrows denote the spin directions. The energy range in the plot is $[-0.3, 0.3]$ eV.

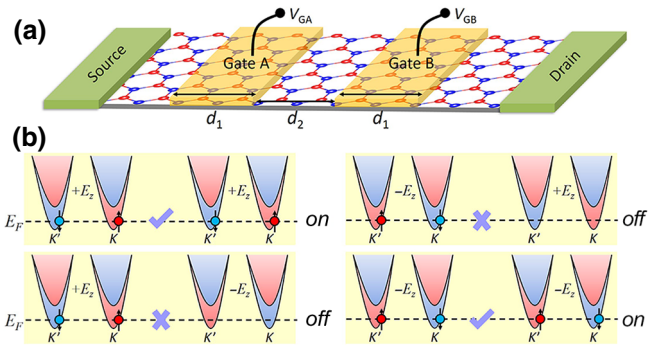

FIG. 2. (a) Schematic of the four-terminal device model with two gates A and B. d_1 and d_2 denote the gate width and gate separation distance, respectively. The source and drain are directly connected to the 2D channel, while there is an insulating dielectric layer between the gate and 2D channel. (b) Band alignments at the gate regions for different gate polarities determined by the electric field E_z. Dashed lines denote the Fermi energy E_F. Electrons (filled circles) can be transmitted (*on* state) or blocked (*off* state) depending on E_z in the gated regions.

Figure 3(a) shows the calculated zero-bias conductance as a function of the input gate A when B is set to negative. For a positive gate A voltage (logic input A = 1), the device is in the low conductance state. For a negative gate A voltage (logic input A = 0), the device is in the high-conductance state. For the parameters used in the calculation, the on:off conductance ratio exceeds 300. This value can be further enhanced by increasing gate width d_1 (e.g., the on:off ratio is enhanced by a factor of 10 when d_1 is increased from $40a$ to $50a$) [25]. Figure 3(b) shows the dependence of zero-bias conductance on the two logic inputs A and B. It is seen that A = B = 1 or A = B = 0 yields the high-conductance state. In all other cases, the device is in the low-conductance state.

Although the device of Fig. 2(a) has logic functionalities, it cannot be used for cascading. While the logic input is the voltage supplied by the source, the logic output is the device conductance, which is not suitable as an input of the successive gate. A similar problem has been encountered in the previously proposed devices [3,4], where the logic input and output were encoded in different physical quantities.

To address this problem, we design XNOR and XOR logic gates, as schematically shown in Fig. 4. This design satisfies the concatenation requirement where the output voltage of the logic gate can be used as the logic input for the successive gate. As seen from Fig. 4, each gate represents two circuits, upper and lower, with VDD (–VDD) supply voltage on the upper (lower) circuit and a common output. Gate A serves as a topgate or backgate (i.e., connected to the top or bottom of the 2D channel), providing an invert of A input in the latter case. It is to be noted that the upper and lower channels are directly connected to the output and VDD, while there is an insulating layer between the gate and channel. As seen from Fig. 4(a), when A = B, the top circuit is in *on* state, while the bottom circuit is in *off* state, and the output voltage is positive, corresponding to logic state 1. When A ≠ B, the top circuit is in *off* state, while the bottom circuit is in *on* state, and the output voltage is negative, corresponding to logic state 0. The XNOR logic operation is thus realized. The XOR gate is obtained from the XNOR gate by changing gate A to be a backgate on the upper circuit and a topgate on the lower circuit [Fig. 4(b)]. The NOT gate can be realized from the XNOR gate by setting A to 0 or from the XOR gate by setting A to 1.

The design of AND and NAND gates requires a five-terminal building block shown in Fig. 5(a), which involves three gates A, B, and C. Figure 5(b) shows the relative band alignment between the three gated regions. As is evident from this figure, depending on the relative input polarities of the gates, electrons can be efficiently transmitted through the intravalley transport or blocked, which gives rise to the corresponding *on* and *off* conductance states.

Figures 6(a) and 6(b) show the calculated conductance as a function of gate inputs. When gate C is set to positive [Fig. 6(a)], only the input A = B = 1 gives rise to the high-conductance state, while all other inputs yield the low-conductance state, in agreement with Fig. 5(b). When gate C is set to negative [Fig. 6(b)], only the input

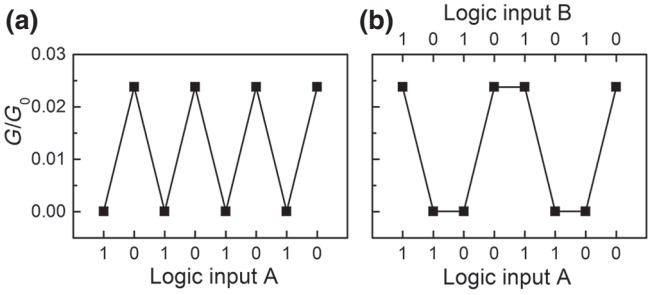

FIG. 3. (a), (b) Total conductance in units of $G_0 = 2e^2/h$ as a function of logic inputs on gates A and B (bottom and top axes, respectively). In (a), gate B is set to negative (B = 0). $|E_z| = 1.25$ V/nm.

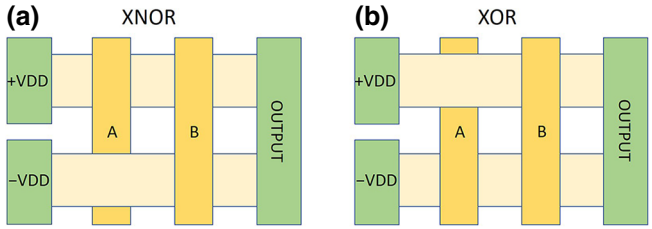

FIG. 4. Schematics of (a) XNOR and (b) XOR gates. The light-yellow regions represent 2D channels. Gates A and B act as two logic inputs. Gate A serves as a topgate or backgate, providing an invert of A input in the latter case. VDD is the supply voltage, providing +VDD (–VDD) voltage in the upper (lower) circuit.

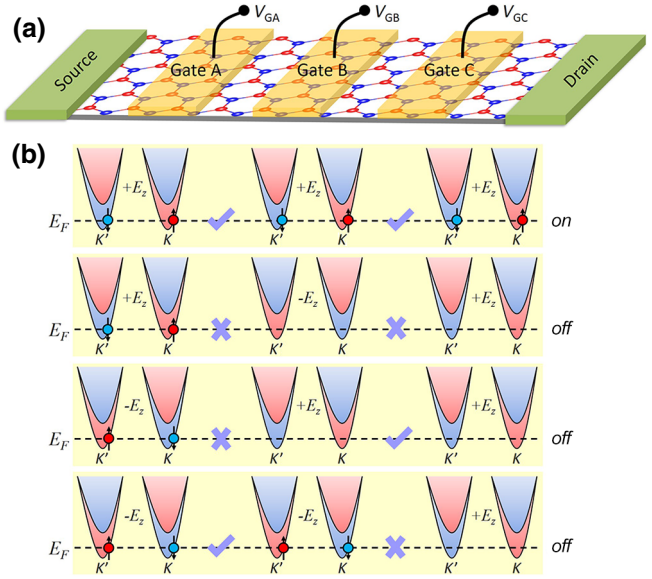

FIG. 5. (a) Schematic of the five-terminal device model with three gates A, B, and C. The source and drain are directly connected to the 2D channel, while there is an insulating dielectric layer between the gate and 2D channel. (b) Band alignments at the gate regions for different gate polarities determined by the electric field E_z. Dashed lines denote the Fermi energy E_F. Electrons (filled circles) can be transmitted (*on* state) or blocked (*off* state) depending on E_z in the gated regions.

A = B = 0 gives rise the high-conductance state, while all other inputs yield the low-conductance state.

Based on this conductance behavior, we design AND and NAND logic gates that provide the concatenation requirement, as shown in Fig. 7. In Fig. 7(a), control gate CTRL is set to +VDD, and when A = B = 1 (+VDD), the two upper devices are in *off* state while the lower is in *on* state. Hence, the output voltage is going to be close to +VDD, resulting in logic state 1. In all other cases, the lower device is in *off* state, and the output voltage is –VDD, resulting in logic state 0. The AND logic operation is thus realized. The NAND gate is obtained by swapping the VDD and –VDD contacts [Fig. 7(b)]. The OR and NOR gates can be realized

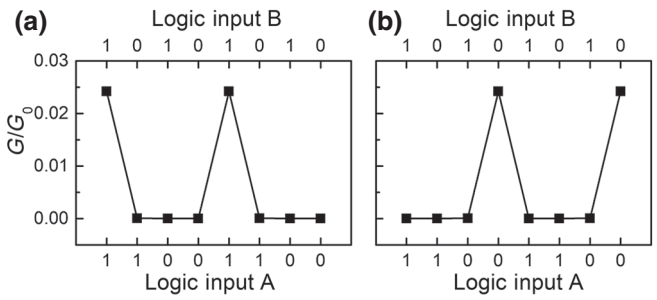

FIG. 6. (a), (b) Total conductance in units of $G_0 = 2e^2/h$ as a function of logic inputs on gates A and B (bottom and top axes, respectively). Gate C is set to (a) positive and (b) negative. $|E_z| = 1.25$ V/nm.

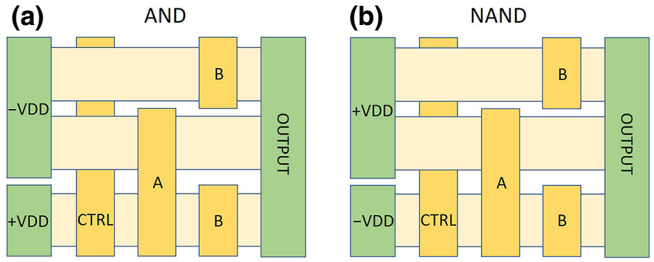

FIG. 7. Schematics of (a) AND and (b) NAND gates. The light-yellow regions represent 2D channels. Gates A and B act as two logic inputs. Gate CTRL = +VDD serves as a topgate or backgate, providing an invert of CTRL input in the latter case. VDD is the supply voltage.

from the NAND and AND gates, respectively, by setting CTRL to be –VDD.

A common figure of merit to characterize the field-effect transistor performance is a subthreshold swing, which is how much change in the gate voltage is required to alter the drain current by one decade. We estimate this quantity by calculating the conductance of the device of Fig. 2(a) in the *off* state as a function of applied electric field E_z. We find that conductance changes by an order in magnitude with $E_z \sim 0.12$ V/nm. Assuming the channel thickness of 1 nm, this transforms to a subthreshold swing approximately 120 mV/dec, which is larger than that of the ultimate MOSFET performance of 60 mV/dec at room temperature. We note, however, that the estimated subthreshold swing is strongly reduced with increasing d_1. Thus, amending the geometry of the device allows further improvement of the subthreshold swing. On the other hand, our calculation does not take into account disorder and phonon scattering, which are expected to reduce the on:off ratio due to intervalley scattering. However, the two K and K' valleys are well separated by a wavevector comparable to the size of the Brillouin zone. Thus, intervalley scattering is equivalent to a large momentum transfer, which requires a very strong random potential. We expect therefore that the on:off ratio is largely robust against this scattering [25].

In addition to silicene, germanene, and stanene, a 1T'-MX_2 monolayer [31] (M = Mo, W; X = S, Se, Te) and a 2H-MX_2 bilayer [32] represent other promising candidates for valley-spin logic gates, due to their electrically controllable valley-spin polarization. The proposed design rules for the valley-spin logic gates are universal for all these 2D materials.

IV. CONCLUSIONS

In summary, we propose the design of valley-spin logic gates based on 2D materials, which support the VSV effect. The proposed devices utilize multiple gate contacts acting as logic inputs, while the output logic states are encoded in the output voltage. Through the analysis of the relative band alignment and the calculated conductance,

we demonstrate the realization of seven logic gates namely NOT, XNOR, XOR, AND, NAND, OR, and NOR. Our proposed valley-spin logic gates satisfy the concatenation requirement, where the output voltage of the logic gate can be used as the logic input of successive gate. Our results validate the practical use of the electrically controlled valley-spin locking in emerging 2D materials in logic devices.

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