Designing sub-10-nm Metal-Oxide-Semiconductor Field-Effect Transistors via Ballistic Transport and Disparate Effective Mass: The Case of Two-Dimensional BiN

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In the post-Moore era, improving energy efficiency is an urgent requirement for microelectronics moving towards the Internet of Things, artificial intelligence, and 5G. In particular, two-dimensional (2D) materials with natural passivation, gate electrostatics, and high mobility have attracted significant attention for integrated circuits in the race towards next-generation field-effect transistors (FETs). Here, by coupling first-principles and nonequilibrium-Green's-function approaches, we obtain a physical understanding of the ballistic transport properties of a V-V binary bismuth nitride (BiN) material. Promisingly, monolayer BiN has sharp conduction-band and flat valence-band edges, which exhibit disparate effective masses. Simulated sub-10-nm monolayer BiN transistors show potential device performance and fulfill the high-performance and low-power requirements of the goals of the International Technology Roadmap for Semiconductors 2028 with their optimal parameters. Furthermore, by comprehensively analyzing the effective mass, density of states, *on*-state current, subthreshold swing, etc., we show that materials whose band dispersions have an extreme character have advantages for transistors. Also, benchmarking of the energy-delay product confirms that BiN FETs possess sufficient competitiveness against other 2D FETs. We believe that this could be a guide for designing potential channel materials for next-generation FETs.

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I. INTRODUCTION

Moore's law, as a technoeconomic model, has supported the global information-technology industry in nearly doubling the performance and functionality of integrated circuits every 18 (or 24) months within the limitation of a fixed cost and area. In the post-Moore era, it is critical to propel device performance to high performance (HP) and low power (LP) for highly demanding applications, such as the Internet of Things, artificial intelligence, and 5G. However, with the development of Moore's law, the trend of node progression and size reduction is becoming slower, and it is difficult for silicon-based semiconductors to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS) [1]. Therefore, technological innovation is key to providing diversified development routes for microelectronics in the post-Moore era, especially in terms of channel materials [2–5]. Recently, two-dimensional (2D) semiconductor materials have received extensive attention [6–11]. Since traditional semiconductors cannot reach the ultrathin limit, 2D materials with natural passivation, gate electrostatics, and high mobility will play a critical role in next-generation electronics [12–18].

Disappointingly, it is still a challenge to design 2D channel materials that could meet the ITRS requirements of HP and LP. Two-dimensional MoS_2, an emerging 2D channel material for field-effect transistors (FETs), is subject to low mobility and a small *on*-state current, indicating inadequacy for HP FETs [19,20]. As another promising 2D material, black phosphorene has attracted much attention due to its high mobility and excellent electronic properties, but its device performance is easily degraded as a result of

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from instability in the ambient environment [21]. Therefore, various tunable technologies have been employed to enrich the properties and expand the applications of 2D materials. Notably, following the path opened up by the transition-metal dichalcogenides, 2D V-V binary materials are receiving increasing attention, and are a promising type of material for next-generation microelectronic devices. Compared with 2D group-VA materials (such as phosphorene and antimonene), they can not only maintain intrinsic excellent electronic properties but also offer further improved stability. For example, due to moderate band gaps and high carrier mobility, 2D AsP has been proved to be a promising alternative material for optoelectronic applications [22–24]. However, the research on this kind of material has not been sufficient. Thus, it is crucial to explore their quantum transport properties and application performance in electronic devices at the atomic level.

Here, through a multiscale approach coupling density-functional theory (DFT) and the nonequilibrium Green's function (NEGF), we obtain a physical understanding of the ballistic transport properties of the V-V binary material BiN, which shows disparate band structures at the conduction-band minimum (CBM) and valence-band maximum (VBM). Notably, the calculated electron effective mass is quite light, with a value of 0.23 m_0, while the hole effective mass is heavy, up to 2.00 m_0, leading to a room-temperature (300 K) mobility of 3.49×10^3 and $0.938\ \mathrm{cm^2\ V^{-1}\ s^{-1}}$ for electrons and holes. Simulated sub-10-nm monolayer BiN double-gated (DG) metal-oxide-semiconductor FETs (MOSFETs) show good device performance and can fulfill the goals of ITRS with their optimal parameters. In particular, by analyzing the effective mass, density of states (DOS), *on*-state current (I_{on}), subthreshold swing (SS), etc., we show that a material whose band dispersion has an extreme character has advantages for use in transistors. Besides, benchmarking of the energy-delay product (EDP) with other 2D FETs also indicates that BiN FETs possess sufficient competitiveness with other 2D FETs. These factors cause the band dispersion to be a criterion for designing potential channel materials.

II. COMPUTATIONAL DETAILS

The geometric-optimization, electronic-structure, and transport-property calculations are performed with the Quantum ATK 2019 package [25]. The generalized gradient approximation in the form of the Perdew-Burke-Ernzerhof functional is adopted to describe the exchange and correlation interaction [26]. The density-mesh cutoff is set to 105 hartree. For structural relaxation, the force tolerance is set to 1×10^{-2} eV/Å, and the stress-error tolerance is set to 0.1 GPa. The Brillouin zone is sampled by using $11 \times 11 \times 1$ Monkhorst-Pack k-points for the monolayer BiN model. A large vacuum layer, of over 25 Å, is employed to avoid interactions between periodic images. The phonon-limited carrier mobility of the monolayer is obtained by solving the Boltzmann transport equation in the relaxation-time approximation,

$$\mu = -e\frac{\sum_{k,n} \tau_{k,n} v_{k,n}^2\, \partial f\,(\varepsilon_{k,n})/\partial \varepsilon_{k,n}}{\sum_{k,n} f\,(\varepsilon_{k,n})},$$

where $\tau_{k,n}$ is the momentum relaxation time for electrons in the state $|k, n\rangle$, $v_{k,n}$ is the group velocity, $\varepsilon_{k,n}$ is the band energy, and f is the Fermi-Dirac distribution. The phonon dispersion and electron-phonon interaction are obtained from an $11 \times 11 \times 1$ supercell calculation in the case of monolayer BiN. The performance of monolayer BiN is evaluated using a DG two-probe MOSFET model. Ballistic transport properties are computed by the DFT and the NEGF methods. The k-point meshes for the central region and the electrodes are sampled with $30 \times 1 \times 1$ and $30 \times 1 \times 100$ points, respectively. The drain current is calculated with the Landauer-Büttiker formula [27],

$$I_d(V_b, V_{GS}) = \frac{2e}{h}\int_{-\infty}^{+\infty} \{T(E, V_b, V_{GS}) \times [f_S(E-\mu_S) - f_D(E-\mu_D)]\}\, dE$$

where $T\ (E,\ V_{GS},\ V_b)$ is the transmission probability at a given gate voltage V_{GS} and bias voltage V_b, f_S and f_D are the Fermi-Dirac distribution functions for the source and drain electrodes, respectively, and μ_S and μ_D are the electrochemical potential of the source and drain electrodes, respectively. The transmission coefficient $T(E)$ is the average of the k-dependent transmission coefficients $T^{k_\parallel}(E)$ over the Brillouin zone. The k-dependent transmission coefficient at energy E is $T^{k_\parallel}(E) = \mathrm{Tr}\{\Gamma_L^{k_\parallel}(E) G^{k_\parallel}(E) \Gamma_R^{k_\parallel}(E) [G^{k_\parallel}(E)]^\dagger\}$, where $G^{k_\parallel}(E)$ and $[G^{k_\parallel}(E)]^\dagger$ are the retarded and advanced Green functions, respectively, and $\Gamma_{L(R)}^{k_\parallel}(E) = i\left[\sum_{L(R)}^{k_\parallel} - \left(\sum_{L(R)}^{k_\parallel}\right)\right]$ is the level broadening originating from the left (right) electrode, expressed by the electrode self-energy $\sum_{L(R)}^{k_\parallel}$. The temperature of the device simulation is set to 300 K, and the tolerance is set to 1×10^{-4} with the Pulay mixer algorithm for device iteration control.

III. RESULTS AND DISCUSSION

As shown in Fig. 1(a) and Fig. S1(a) in the Supplemental Material [28], monolayer BiN has a hexagonal crystal structure with space group $P3m1$ (no. 156). This is similar to the β-bismuthene structure [29,30], but the unit cell of monolayer BiN contains one Bi atom and one N atom with an optimized lattice parameter of 3.47 Å and a Bi-N bond length of 2.26 Å. From an analysis of electron localization functions, a substantial concentration of electrons is located around atoms, indicating ionic bonding, which is

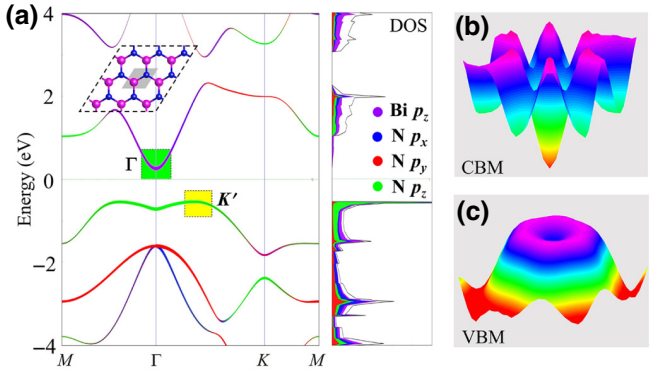

FIG. 1. (a) Orbital-resolved band structures and density of states of monolayer BiN. The inset shows the crystal structure of monolayer BiN. (b),(c) Corresponding projection drawings of the (b) CBM and (c) VBM over the Brillouin zone.

shown in Fig. S1(b) [28]. Then, the deformation electronic density of 2D BiN is calculated to further study the nature of its chemical bonding. As shown in Fig. S1(c) [28], there is a remarkable electron transfer from the p orbitals of the Bi atoms to those of the N atoms. The transferred electrons are localized around the N atoms, and this illustrates the ionic character of the Bi-N bonds. Moreover, to confirm the kinetic stability properties, we perform a calculation of the phonon spectrum of monolayer BiN. As shown in Fig. S1(d) [28], the absence of an imaginary phonon mode indicates that the BiN structure is kinetically stable [31].

The electronic properties of monolayer BiN are displayed in Fig. 1(a), which reflects that it is a semiconductor with an indirect band gap of 0.8 eV. The CBM is located at the Γ high-symmetry point. Notably, the VBM is between the Γ and K high-symmetry points (at the K' point), and the valence band is shaped like a Mexican hat because the energy of the highest occupied state near the Γ point is suppressed. Resembling the shape of a van Hove singularity near the Fermi level, a small dispersion in the top valence band is observed close to the Γ point, resulting in sharp peaks in the DOS [32]. By contrast, the DOS of the CBM is relatively smooth due to the strong conduction-band dispersion. To investigate the origin of these band structures in monolayer BiN, we compute partial densities of states (PDOSs) and compare the valence- with the conduction-band edge. The CBM is contributed mainly by the Bi p_z orbitals, while the VBM state contains the p_z orbitals of the N atoms, which corresponds with the results for the orbital-resolved band structures.

Also, we compare the band structures and densities of states of monolayer BiN without and with spin-orbit coupling (SOC). As shown in Fig. S2(a) [28], for the conduction band, BiN exhibits a small Rashba-type splitting, with the crossing point at about 180 meV. By evaluating the characteristic parameters quantifying the strength of the Rashba splitting, we find that the momentum offset k_0 is only 0.010 $Å^{-1}$ along the Γ-K direction, and the Rashba energy E_R is just 15.5 meV. As exhibited in Table S1 [28], these values are significantly smaller than those in other Rashba-splitting 2D materials [33–37]. Also, we calculate the DOS of BiN with and without the SOC effect in Fig. S2(b) [28], which also indicates the shape of the valence- and conduction-band extrema. The change in the total DOS near the Fermi level is very subtle. Specifically, we compute the PDOSs of BiN. The PDOS spectra projected on Bi p_z orbitals indicate that there is little change in the DOS at the conduction-band edge before and after considering the SOC effect. Therefore, the spin-orbit splitting has very little effect on the band structure.

To give a more in-depth insight into the band-dispersion relation around the Fermi level, as shown in Figs. 1(b) and 1(c), we plot projection drawings for the CBM and VBM of BiN over the Brillouin zone. The energy-dispersion plot in three-dimensional k-space demonstrates significant isotropy of the valence- and conduction-band edges, which eventually generate isotropy of the effective mass along any direction. Furthermore, we study the matrix elements of the electron-phonon interaction for three acoustic branches: the out-of-plane acoustic (ZA), transverse acoustic (TA), and longitudinal acoustic (LA) phonons. In 2D BiN, the electron-phonon interaction is provided dominantly by ZA phonons. Figure 2 shows the matrix elements of the electron-phonon interaction obtained for the electrons at the CBM and VBM k-points as a function of the ZA-phonon wave vector $\mathbf{q}$. Notably, the average interaction strength at the VBM is larger than that at the CBM. The difference indicates that there are more phonons that have a large interaction strength with electrons at the VBM than that at the CBM, and also suggests that the electron mobility should be higher than the hole mobility in 2D BiN.

Moreover, we compute the carrier effective mass and carrier mobility of BiN. The calculated effective masses of the electrons (m_e^*) and holes (m_h^*) at the edges of the band structure are summarized in Table S2 [28]. Since the electrons are quite light, with $m_e^* = 0.23m_0$, and the holes are very heavy, with a mass of up to $2.00m_0$, the mobility of the electrons should be much higher than that of the holes. The intrinsic acoustic-phonon-limited mobilities of BiN computed at room temperature (300 K) are approximately 3.49×10^3 and 0.938 $cm^2\ V^{-1}\ s^{-1}$ for electrons and holes, respectively [as seen in Fig. 2(c)]. The electron mobility is about two orders of magnitudes higher than the hole mobility in BiN, which is in good agreement with our above analysis of the band dispersion and effective mass. The effects of SOC on the band edges and effective mass are also evaluated. As exhibited in Table S3 [28], the conduction-band edge with SOC is slightly lower than that without SOC ($\Delta E_C = 0.05$ eV), and the valence-band edge with SOC is slightly higher than that without SOC ($\Delta E_V = 0.05$ eV). Furthermore, the changes

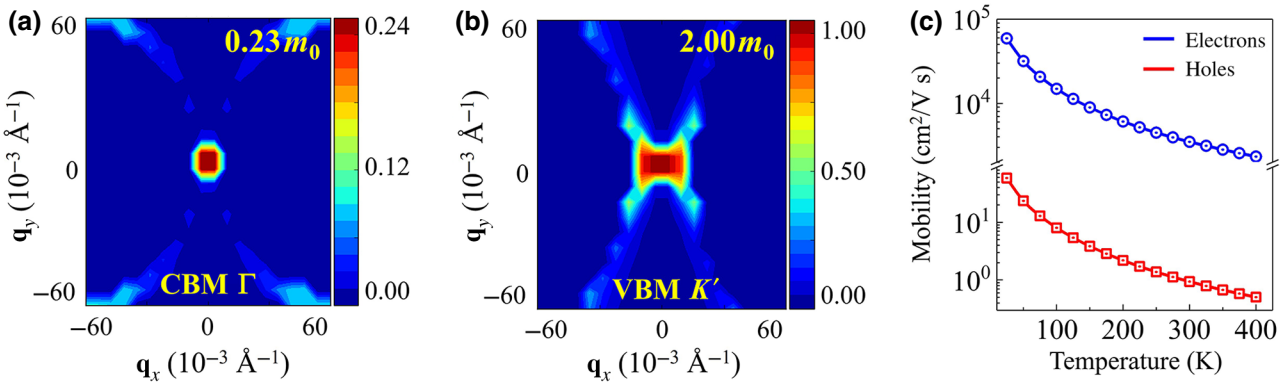

FIG. 2. (a),(b) Matrix elements of electron-phonon interaction in monolayer BiN. The interaction is illustrated as a function of the phonon wave vector **q** for k at the CBM and VBM k-points. (c) Phonon-limited electron and hole mobilities at different temperatures.

in effective mass are also very tiny ($0.14m_0$ for the holes and $0.04m_0$ for the electrons). As a result, it is found that the spin-orbit splitting has a weak effect on the shape of the valence- and conduction-band extrema for monolayer BiN.

A sketch of the device investigated is shown in Fig. 3(a). A DG FET is considered, with a monolayer BiN channel embedded in SiO_2 at the top and bottom, with a thickness of 4.5 Å and a dielectric constant $\varepsilon = 3.9$, which are adapted to the requirements of the ITRS 2013 edition [38]. Figure 3(b) shows the transfer characteristics of n-type (left, doping concentration 10^{13} cm^{-2}) and p-type (right, doping concentration 2×10^{14} cm^{-2}) FETs, where a drain-to-source voltage $V_b = 0.64$ V is applied and the gate length ranges from 2 to 10 nm. The *on*-state current ($I_{\rm on}$) is obtained at the *on*-state voltage V_{GS} (on) $= V_{GS}$ (off) $+ V_{\rm dd}$ in the transfer curves, where $V_{\rm dd}$ (voltage drain drain) is the supply voltage of 0.64 V ($V_{\rm dd} = V_b$). Through evaluating the performance of BiN FETs as a function of the gate length L_G, we first study the impact of source-to-drain tunneling. In all cases, the characteristics are almost identical except for the case of a 2-nm gate length, for both n- and p-type FETs. It is observed that source-to-drain tunneling strongly degrades the subthreshold slope and the $I_{\rm on}/I_{\rm off}$ ratio as the gate length decreases. The primary role of the SS (equal to $\partial V_{GS}/\partial L_G I_{DS}$) is to describe the subthreshold characteristics, which reflect the ability of the gate to control the device in the subthreshold region. The value of the SS for the BiN FETs obviously increases as the value of L_G decreases, as shown in Fig. 3(b). In the case of a 2-nm gate length, the SS of the FET is much larger, indicating the poor gate-controllability of BiN devices with an ultrashort channel in the subthreshold region. Corresponding representations of the transfer curves on a linear scale are exhibited in Fig. S3 [28].

As can be seen, the behavior of the BiN FETs is relatively impressive for a variety of gate lengths, meaning that a sufficient length of the channel region is necessary. Notably, due to the lower carrier effective mass, the SS degradation of the n-type FETs is more evident than that of the p-type FETs. For the n-type FET with $L_G = 10$ nm, the value of $I_{\rm off}$ for the BiN FETs is small enough to fulfill the requirements for the off-state current of both the HP (0.1 μA/μm) and the LP (2×10^{-5} μA/μm) criteria of the ITRS. The SS is 73 mV/dec and $I_{\rm on}$ is 714 μA/μm for the HP criterion, which are close to the HP ITRS 2028 goals in the 2013 edition [38]. In contrast, it is found that the SS of p-type FETs is 146 mV/dec, showing some degradation for the p-type FET with $L_G = 10$ nm, and the

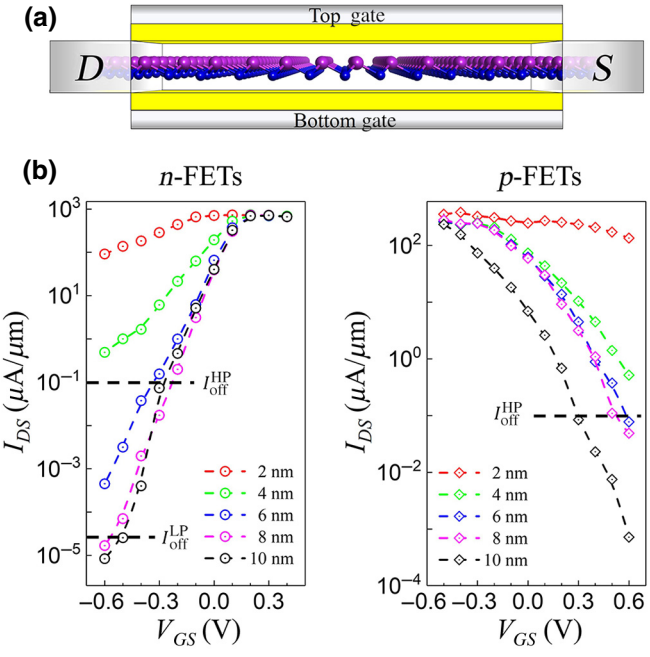

FIG. 3. (a) Schematic illustration of monolayer BiN double-gated FET. (b) Transfer characteristics of n- and p-type FETs with different gate lengths for $V_b = 0.64$ V.

value of I_{on} (72 μA/μm) is hardly enough to fulfill the HP requirements.

Moreover, when the doping concentration reaches $N_e = 2 \times 10^{13}$ cm^{-2}, the drain current is enhanced due to more efficient carrier injection. As shown in Fig. S4 [28], the BiN n-type FETs have values of I_{on} of more than 2000 μA/μm, which are larger than the HP ITRS goal. Also, since underlap structures increase the required channel length and reduce the coupling of the source and drain to the channel, we also introduce underlap structures (2 nm) in the 2D BiN FETs, which significantly lower the tunneling leakage current and suppress short-channel effects (as can be seen in Fig. S5 [28]). However, for p-type FETs with a long gate length, the effect of the underlap structure is negative due to a reduced gating capability. Besides, for the purpose of structural integrity of FETs, a small strain of a few percent is generally applied to the channel for strain engineering of devices in CMOS technology. Therefore, we evaluate the impact on the performance of 8-nm FETs of different strains, ranging from -5 to $+5$%, as shown in Fig. S6 [28]. We observe that, for both n- and p-type FETs, the drain current is marginally increased with the application of a 5% uniaxial strain, while I_{on} shows an opposite change. When a -5% uniaxial strain is applied, the performance of p-type FETs is certainly improved, while n-type FETs show a marginal degradation.

Next, as an example, the local density of states (LDOS) of the n-type FETs with gate lengths of 4 and 8 nm in the *on* and *off* states is provided in Figs. 4(a) and 4(b), to illustrate the gate-modulation mechanism. Brighter colors correspond to higher LDOS values. The maximum barrier height ϕ_m is defined as the energy barrier to transport from the source to the drain. The barriers for all the source carriers inside the bias window are no larger than ϕ_m. In the *off* state ($V_{GS} = -0.4$ V), the 4-nm-gate-length device achieves an effective barrier height $\phi_m = 0.12$ eV [as seen in Fig. 4(a)]. As V_{GS} increases, ϕ_m decreases significantly and drops to zero at $V_{GS} = 0.2$ V (*on* state), and the current increases logarithmically to saturation with it. In the case of a gate length of 8 nm, I_{off} is lower because the barrier is high enough that the supply voltage cannot drive the conduction-band edge downward enough to reduce the barrier [as seen in Fig. 4(b)].

The gate modulation of the BiN p-type FETs is similar to that of the n-type FETs. For p-type FETs, the short gate length is significantly affected by the gate electrode. In the *off* state, the gate voltage does not effectively push the edge of the valence band near the left region of the drain, leaving a small ϕ_m of 0.11 eV. Moreover, ϕ_m increases to 0.22 eV when the gate length increases from 4 to 8 nm (as seen in Figs. S7(a) and S7(b) [28]), which significantly suppresses the thermionic current. By comparison, ϕ_m nearly vanishes in the *on* state due to the collective effect of the small ϕ_m in the *off* state, which is distinctly

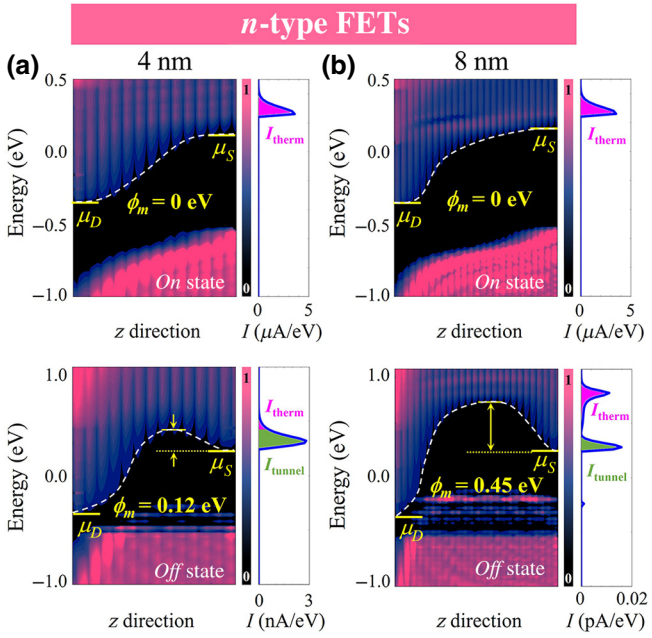

FIG. 4. Spatially resolved LDOS and spectral currents for n-type FETs in the *on* and *off* states with (a) 4-nm and (b) 8-nm gate length.

revealed by the valence-band profiles. Also, an analysis of the corresponding transmission eigenstates is exhibited in Fig. S8 [28]. The eigenstates in the *on* state possess nearly total transmission, revealing a full-phase oscillation and a uniform electron density. In comparison, a dramatic decrease appears in the transmission eigenvalue and there is nearly zero transmission in the *off* state for both n- and p-type FETs. These results agree well with the analysis of previous LDOSs of devices.

The total spectral current is composed of a tunneling current (I_{tunnel}) and a thermionic current (I_{therm}) out of the bias window, as shown in Fig. 4. The maximum of ϕ_m separates I_{tunnel} and I_{therm}. Compared with the 8-nm FETs, the spectral currents of the 4-nm FETs in the *off* state increase sharply by several orders of magnitude. In the *on* state of the BiN n-type FETs, the gate voltage reduces the upward slope of the CBM of the channel and diminishes ϕ_m, while I_{therm} dominates the total current. Notably, although the CB is connected to the VB at the left edge of the gate, no current component is observed in this energy range [39]. The reason is that local and discontinuous states in the VB impede the movement of electrons from the LDOS in Fig. 4(b). As is known, the SS can be expressed as $S_s = r_{tunnel} S_{s_{tunnel}}^{-1} + (1 - r_{tunnel}) S_{s_{therm}}^{-1}$, where S_s is the SS, and r_{tunnel} is the percentage of the tunneling current (I_{tunnel}) in the total current [40]. Therefore, for the n-type FETs with longer channels studied here, the intraband tunneling is suppressed, and the SS is close to the ideal value, with a large I_{on}/I_{off} ratio. Besides, on account of the large hole

effective mass, the p-type FETs also show a strong suppression of the source-to-drain tunneling, which is disabled only for the p-type FET with a 2-nm gate length.

In Fig. 5, taking the 8-nm FET as an example, the critical figures of merit for ballistic-transport performance are benchmarked against the ITRS requirements for LP devices. Firstly, a large enough *on*-state current is critical for logic switches to have a high switching speed and competitive performance in digital devices. From Fig. 5(a), the 8-nm BiN n-type FET has a value of I_{on} of 724 μA/μm, which is larger than the LP ITRS requirement. For the p-type FET, it can be seen that its I_{on} is less than that of the n-type device and has a value of 101 μA/μm. The reason lies in the larger carrier effective mass and the slower carrier velocity in the p-type FETs. The effective mass is proportional to the reciprocal of the curvature of the band-dispersion spectrum. As exhibited in Fig. 1, the effective mass of the holes is larger than that of the electrons in BiN. According to the formula $v = (1/h)(dE/dk) = (\hbar k/m^*)$, a larger effective mass decreases the carrier velocity, and thus the *on*-state current. On the other hand, because $I_{\text{tunnel}} \propto e^{-l\sqrt{m^*\phi_m}}$, where l is the width of the barrier, I_{tunnel} decreases exponentially with the effective mass. Therefore, the larger effective mass easily suppresses the tunneling leakage. As a result, the BiN p-type FET exhibits a smaller I_{tunnel} than does an n-type FET.

Also, the ability to handle rapid operations is another significant factor in the performance of digital circuits. In this context, the gate capacitance (C_G) and the intrinsic delay time (τ) are two fundamental factors. C_G is calculated from $C_G = \partial Q_{\text{ch}}/\partial V_{GS}$, where Q_{ch} is the total charge in the channel region. As shown in Fig. 5(b), the values of C_G (0.18 fF/μm) for the n- and p-type BiN FETs with an 8-nm gate length can meet the LP ITRS goal. The switching speed can be directly evaluated from the intrinsic delay time τ, by the formula $\tau = C_G V_{\text{dd}}/I_{\text{on}}$. In this case, the calculated values of τ for the n- and p-type FETs are 0.14 and 0.44 ps, respectively [as seen in Fig. 5(c)], which could also achieve the LP ITRS requirements for the next decade. Benefiting from a small τ, both n- and p-type BiN FETs could be potential logic transistors with a fast switching speed. The power dissipation $D_P = V_{\text{dd}} I_{\text{on}} \tau$ is also a vital index concerning the switching energy. From Fig. 5(d), all of the calculated values of D_P for the 8-nm BiN FETs (0.075 and 0.13 fJ/μm) are much lower than the maximum value of the LP ITRS requirement. Similarly, related figures of merit of BiN 8-nm FETs with different doping concentrations are also benchmarked against the ITRS requirements for HP devices (as seen in Figs. S9 and S10) [28]. The results indicate that the metrics of highly doped (2×10^{13} cm^{-2}) FETs can meet the HP ITRS requirements.

Moreover, it is noteworthy that the CBM is relatively sharp, while the VBM is very flat. Interestingly, the two kinds of FET, with their optimal parameters, also demonstrate competitive performance. A band edge with an extreme character (either very sharp or flat) is beneficial for obtaining better performance. To investigate the inherent relation between electronic properties and device performance, monolayer PN (phosphorus nitride) is selected as a reference for comparison. The crystal structure and space group of PN are the same as those of BiN. Also, phosphorus and bismuth both belong to group VA, and the compounds BiN and PN belong to the same group of isoelectronic derivatives. Compared with compounds of different main-group elements, BiN and PN possess more similar electronic properties, which introduces as few variables as possible.

For different 2D semiconductors, the carrier effective mass is the primary difference in the context of application in FETs. The band gap also plays an important role in electronic devices. However, if the band gap is large enough to suppress minority-carrier leakage, this becomes a secondary issue [41]. In this case, monolayer PN has an indirect band gap of 1.75 eV, which is in a suitable range for use as a channel material for FETs. As presented in the green region in Fig. S11(a) [28], compared with 2D PN, the CBM structure of BiN is relatively sharp, causing a smaller DOS and electron effective mass. Moreover, we consider the electron-phonon interaction for the electrons here. Because of the smaller effective mass, the electron-phonon interaction in BiN is weaker than that in PN. This difference indicates less scattering in BiN, and so the electron mobility in BiN should be higher than in PN. As discussed above, a smaller effective mass makes it easier

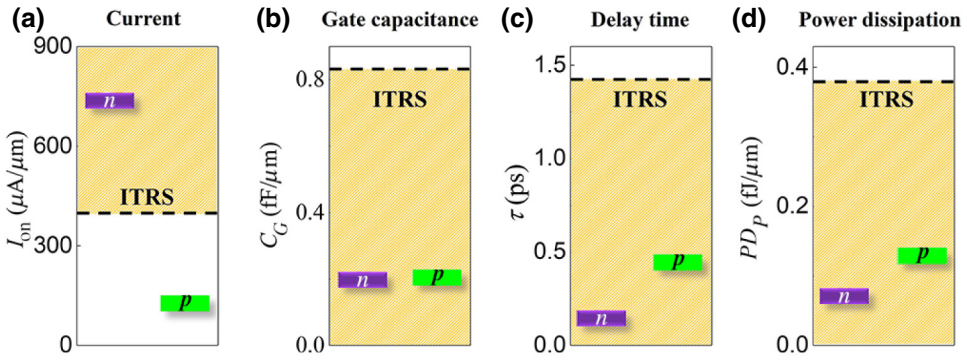

FIG. 5. (a) *On*-state current, (b) gate capacitance, (c) delay time, and (d) power dissipation of n- and p-type BiN FETs with 8-nm gate length. The black dashed lines show the LP ITRS requirements.

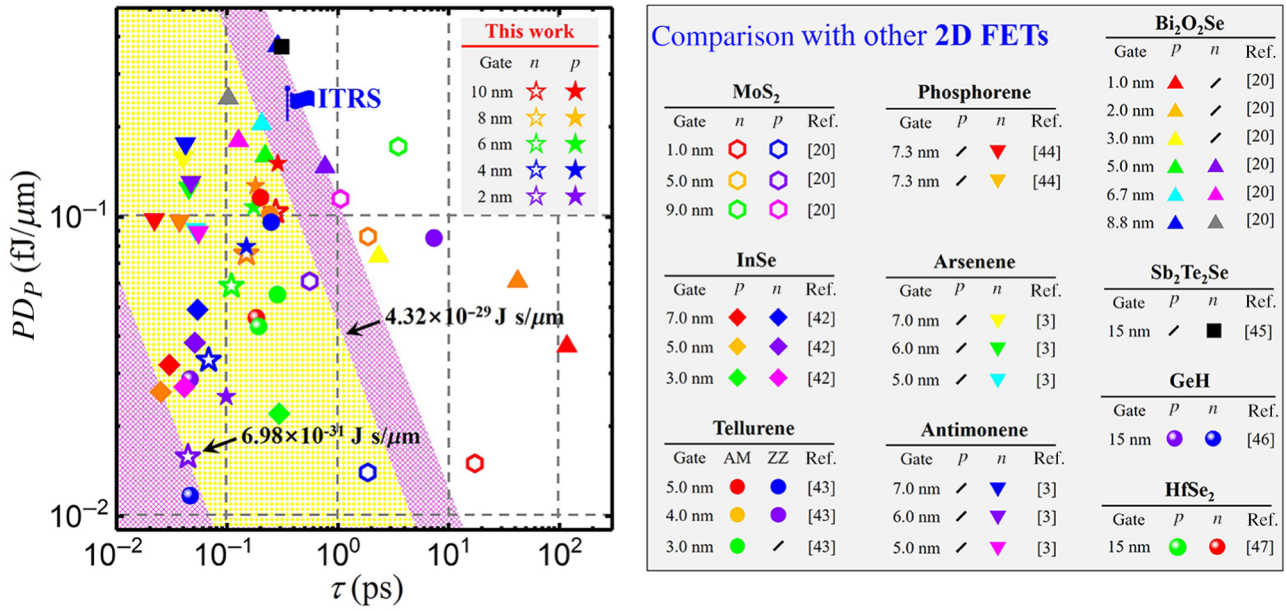

FIG. 6. Power dissipation versus delay time for FETs composed of 2D BiN and other 2D FETs. The boundaries of the colored regions correspond to specific values of the EDP. AM, armchair direction; ZZ, zigzag direction.

to generate a high carrier velocity, and hence a high *on*-state current. Indeed, the value of I_{on} in *n*-type BiN FET is larger than that in PN (as seen in Fig. S11c [28]). Hence, the conduction-band dispersion of 2D BiN, which shows a very sharp character, is more suitable for *n*-type FETs than that of PN.

In contrast, for the valence-band edge, monolayer PN exhibits an evident dispersion, resulting in a smaller DOS around the Fermi level. As shown in Fig. S11(b) [28], the larger hole effective mass (2.00 m_0) leads to a more significant electron-phonon interaction in monolayer BiN. Furthermore, we compare the device performance, including the *on*-state current, SS, and I_{on}/I_{off} ratio. According to the formula for the DOS $(g_s g_v/2\pi\hbar^2)\sqrt{m_x^* m_y^*}$, where g_s and g_v are the spin and valley degeneracies, respectively, a large DOS could guarantee a sufficient current (I_{on}) in a channel material (as seen in Fig. S11d [28]). Also, due to the reduced probability of carriers tunneling through the potential barrier, the heavy effective mass could avoid a source-to-drain current I_{tunnel} and improve the SS in a BiN *p*-type FET. Therefore, a valence-band dispersion with a very flat character is also a characteristic of potential 2D BiN materials for sub-10-nm channels.

Furthermore, to evaluate the performance of BiN FETs more intuitively, we extract the power dissipation D_P versus the delay time τ for comparison with other 2D FETs in Fig. 6, namely devices made from MoS_2 [20], InSe [42], tellurene [43], phosphorene [44], arsenene [3], antimonene [3], Bi_2O_2Se [20], Sb_2Te_2Se [45], GeH [46], and $HfSe_2$ [47]. The EDP (equal to $D_P \times \tau$) is a key figure of merit that considers both performance (speed) and energy dissipation simultaneously, and it is vital to seek the minimum EDP to obtain the optimum operational conditions. Since all of the devices are simulated with heavy doping in the electron regions and ohmic contact resistance is ignored, the results correspond to the upper limit of performance. As shown in Fig. 6, all EDPs of the BiN FETs (6.98×10^{-31}–4.32×10^{-29} J s/μm) are below the ITRS 2028 requirement (1.02×10^{-28} J s/μm), indicating an appealing future for 2D transistors. In particular, the EDP of a BiN *n*-FET with an 8-nm gate length is 1.12×10^{-29} J s/μm, which is lower than the values reported for MoS_2 (2.61×10^{-29}–6.03×10^{-28} J s/μm), tellurene (1.56×10^{-29}–6.27×10^{-28} J s/μm), and Bi_2O_2Se (2.27×10^{-29}–4.33×10^{-27} J s/μm) FETs. Accordingly, the EDP of BiN FETs shows sufficient competitiveness among 2D FETs.

IV. CONCLUSION

To summarize, we predict the performance limit of sub-10-nm 2D BiN MOSFETs through DFT and NEGF simulations. The 2D BiN material shows disparate band structures for the conduction- and valence-band edges, and the calculated small electron effective mass ($0.23m_0$) indicates that a high phonon-limited mobility (3.49×10^3 cm^2 V^{-1} s^{-1}) can potentially be obtained. Then, we simulate sub-10-nm monolayer BiN MOSFETs, which emerge with a performance compliant with industry requirements for ultrascaled channel lengths. With the optimal parameters, the results show good device performance and fulfill the HP and LP requirements of the

ITRS 2028 goals for digital circuits. To study whether the band edges of BiN, with their extreme character, are beneficial for obtaining high performance, we choose 2D PN as a reference substance for comparison with BiN. Based on an analysis of the effective mass, DOS, I_{on}, SS, etc., we obtain the result that a material whose band dispersion has an extreme character has advantages for sub-10-nm FETs. Also, benchmarking the EDP against other 2D FETs reveals that BiN FETs possess sufficient competitiveness. We expect that our predictions will provide a strong motivation for designing potential channel materials for next-generation FETs in the post-Moore era.

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