Reduced Thermal Variation of Perpendicular Magnetic Anisotropy in Magnetically Stiffened Dual-W Composite Storage Layer for Spin-Transfer-Torque Magnetic Random-Access Memory

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State-of-the-art spin-transfer-torque magnetic random access memory (STT MRAM) is based on out-of-plane magnetized magnetic tunnel junctions (pMTJ), which commonly comprise a composite storage layer (CSL) of the form $Fe_{72}Co_8B_{20}$/nonmagnetic spacer (e.g., Ta, W, Mo)/$Fe_{72}Co_8B_{20}$. Because STT MRAM has to operate over a wide range of temperature (e.g., −40 °C to 150 °C for automotive applications), it is desirable to minimize the temperature variation of the magnetic and transport properties of pMTJs. In this context, we report an alternative design of a dual-W CSL of the form "$Fe_{72}Co_8B_{20}$/W/ferromagnet/W/$Fe_{72}Co_8B_{20}$", which brings additional degrees of freedom, to further improve the performance of the storage layer. In particular, this design reduces the thermal variation of magneto-transport properties of dual-W CSL. A detailed investigation of the thermal variation of magnetic and electrical properties of such dual-W CSLs for various ferromagnet insertions, as characterized by different exchange stiffnesses, is reported. In particular, cobalt insertion between two W laminations significantly enhances the effective perpendicular anisotropy (K_{eff}) at room temperature, relative to that of the conventional composite storage layer ($Fe_{72}Co_8B_{20}$/W/$Fe_{72}Co_8B_{20}$), and reduces the relative thermal variation of K_{eff} in the range 300–400 K. Moreover, STT MRAM cells with diameters of 80 nm comprising Co inserted into dual-W CSL exhibit, on average, 15% and 38% higher thermal stability factors, as well as 26% and 15% higher tunneling magnetoresistance ratios at room temperature and 110 °C, respectively, than those of conventional CSLs. These observations are interpreted in terms of magnetic stiffening of the storage layer achieved thanks to the very high Curie temperature (1388 K) of cobalt.

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I. INTRODUCTION

Spin-transfer-torque magnetic random access memory (STT MRAM) based on out-of-plane magnetized MTJs (pMTJs) is one of the most promising emerging technologies of nonvolatile memory. Indeed, it gathers a unique combination of assets: quasi-infinite write endurance, high speed, low power consumption, and scalability. Embedded STT MRAM is about to enter into volume production for e-FLASH and L3 static random access memory (SRAM) replacement [1].

STT MRAM uses a pMTJ as a storage element. In pMTJs, the magnetization of the storage layer is pulled out-of-plane thanks to a perpendicular magnetic anisotropy (PMA), which exists at the Fe-Co-B/MgO interfaces due to the electronic hybridization effect [2]. This interfacial PMA is partially balanced by a bulk easy-plane shape anisotropy, which tends to bring back the magnetization of the storage layer to the plane of the layer. This results in a net effective anisotropy barrier separating the two stable magnetic states (magnetization up and down), which can be written $\Delta E = [-(1/2)\mu_0 {M_s}^2 t + K_u t + K_s]A$, where M_s and t are the saturation magnetization and thickness of the storage layer, respectively; μ_0 is the vacuum permeability; A is the cell area; K_u stands for a possible magnetocrystalline or magnetoelastic bulk anisotropy, which is often considered to be negligible in a conventional Fe-Co-B-based storage layer; and K_s is the interfacial anisotropy, which originates at the Fe-Co-B/MgO interface [2,3]. Because of competition between interfacial PMA and bulk easy-plane anisotropy, the thickness of the storage layer cannot be increased above a critical thickness, at which anisotropy undergoes a reorientation from out-of-plane to in-plane. This critical thickness is around 1.5 nm if

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the storage layer is in contact with only one MgO tunnel barrier and can be increased slightly above 2 nm if it is sandwiched between two MgO layers [4–6]. In the latter case, the lamination of a boron-absorbing nonmagnetic material (e.g., Ta [7], W [8–10], Mo [11]) is generally introduced into the central part of the storage layer to attract boron away from the MgO interfaces upon postdeposition annealing.

In all of these pMTJs, the storage layer remains quite thin and, consequently, is prone to the development of thermal fluctuations as the temperature increases. Indeed, it is known that, due to reduced coordination at the surfaces, thin magnetic layers exhibit a reduced Curie temperature (T_c) [12] or become superparamagnetic at lower temperatures, which is different from that of thicker films of the same composition [13,14]. As a result, in conventional STT MRAM, the anisotropy and tunnel magnetoresistance ratio (TMR) strongly depend on temperature. The anisotropy can typically decrease by 50–80% over 100 K [15], whereas the TMR can vary by 20–40% in relative value [16]. This has strong drawbacks for STT MRAM, which has to operate over a wide range of temperatures, in particular, for automotive applications (−40 °C to 150 °C). To guarantee the required data retention at the highest possible operating temperature (T_{max}), the memory array must fulfill $K_{\mathrm{eff}}(T_{\mathrm{max}})V > 80k_BT_{\mathrm{max}}$, where K_{eff} and V are the effective perpendicular anisotropy and volume of the storage layer, respectively [1]. In addition, according to the macrospin model, the write voltage of STT MRAM (beyond the ballistic regime) is proportional to the anisotropy barrier $\Delta E = K_{\mathrm{eff}}V$:

$$V_{P\rightarrow \mathrm{AP}} = -V_{\mathrm{AP}\rightarrow P} = \alpha \frac{4eR_{\perp}}{\hbar P_R} K_{\mathrm{eff}}(T)V, \qquad (1)$$

where α is the Gilbert damping constant of the storage layer; $R_{\perp}$ is the resistance of the tunnel junction for a 90° angle between the storage layer and reference layer magnetization; P_R is the spin polarization of the current emitted from the reference layer; and e and $\hbar$ are the electron charge and reduced Planck constant, respectively [17]. As a result, the write voltage can significantly increase at the lowest possible operating temperature (T_{min}), due to the large increase in $K_{\mathrm{eff}}(T)$ from T_{max} to T_{min}. This implies a larger write current, and therefore, the need to overdesign the selection transistors, so that they can deliver the required current at the lowest possible operating temperature. It may also reduce the barrier endurance if the write voltage exceeds about 0.5 V. This problem also concerns the solder reflow compliance, which is often required for microcontroller memory. Considering this thermal variation of anisotropy, the practical STT efficiency for STT MRAM, which has to operate over a temperature window from T_{min} to T_{max}, is actually $\Delta(T_{\mathrm{max}})/I_{c0}(T_{\mathrm{min}})$, where Δ and I_{c0} are the thermal stability factor and critical switching current, respectively, as expressed by the equations $\Delta = \Delta E/k_BT$ and $I_{c0} = V_{P\rightarrow AP}/R_{\perp}$. It is therefore highly desirable to develop a STT MRAM that possesses a much reduced temperature variation of its magnetic and transport properties and, in particular, of its storage layer anisotropy. We demonstrate that this can be achieved in a composite storage layer (CSL) comprising double refractory metal laminations ($Fe_{72}Co_8B_{20}$/W/ferromagnet/W/$Fe_{72}Co_8B_{20}$) by magnetically stiffening the central part of the storage layer with a material having a higher Curie temperature, such as $Co_{60}Fe_{20}B_{20}$ or cobalt. This dual-W CSL is sandwiched between two MgO barriers and comprises two Fe-rich $Fe_{72}Co_8B_{20}$ layers next to the MgO interfaces to maximize the interfacial anisotropy. We show that the perpendicular magnetic anisotropy of dual-W CSL with $Co_{60}Fe_{20}B_{20}$ and Co insertion are, respectively, 5% and 24% higher than that of a conventional CSL at room temperature and 5% and 40% higher at 400 K. Moreover, STT MRAM cells with diameters of 80 nm comprising Co-inserted dual-W CSLs exhibit higher Δ and TMR over the investigated temperature range (300–400 K) than those of conventional CSLs. In addition, the practical STT efficiency, $\Delta(T)/I_{c0}(25\,^{\circ}\mathrm{C})$ of memory cells with Co-laminated dual-W CSL remains similar to that of conventional CSLs.

II. EXPERIMENTS, RESULTS, AND DISCUSSION

A. Magnetic properties of composite storage with a single W spacer

At first, a CSL with only one W lamination is sputter-deposited to incorporate $Co_{60}Fe_{20}B_{20}$ into the middle of the composite storage layer, while keeping $Fe_{72}Co_8B_{20}$ layers above and below the MgO barrier and cap layers, respectively. The idea is to insert a magnetic layer with a higher Curie temperature to improve the PMA not only at room temperature, but also at higher operating temperatures. These investigated storage electrodes, with only one W lamination in the CSL, have the following compositions: Ta 3/$Fe_{72}Co_8B_{20}$ 0.3/Mg 0.7/oxidation 30 s/Mg 0.5/CSL/Mg 0.4/oxidation 10 s/Mg 0.4/W 2/Pt 3 nm, in which three compositions of CSL are compared, such as {$Fe_{72}Co_8B_{20}$ 1.1/W 0.2/$Fe_{72}Co_8B_{20}$ 0.8}, {$Fe_{72}Co_8B_{20}$ 0.7/$Co_{60}Fe_{20}B_{20}$ 0.4/W 0.2 /$Fe_{72}Co_8B_{20}$ 0.8} and {$Fe_{72}Co_8B_{20}$ 0.4/$Co_{60}Fe_{20}B_{20}$ 0.7/W 0.2/$Fe_{72}Co_8B_{20}$ 0.8}. They are used to investigate the magnetic properties at various annealing stages. The 0.3 nm $Fe_{72}Co_8B_{20}$ layer underneath the bottom MgO barrier is magnetically dead at room temperature. It is introduced to improve the structural similarity between these initially studied structures, which focus on the magnetic properties of the CSL and full pMTJ stacks incorporating a synthetic antiferromagnetic reference layer, which is described in section B.

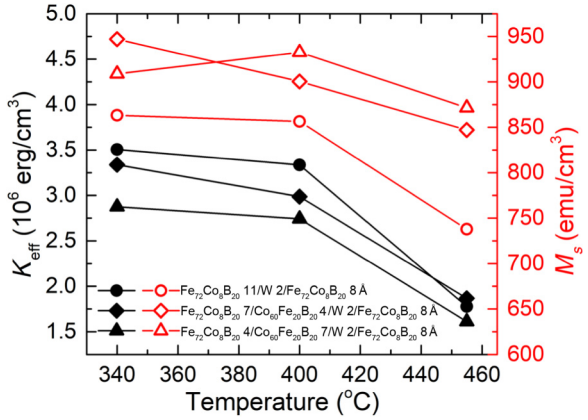

FIG. 1. Effective perpendicular magnetic anisotropy (K_{eff}) and saturation magnetization (Ms) of three CSLs at different annealing temperature. The composition of the samples is mentioned in the figure.

Figure 1 shows K_{eff} and M_s as a function of annealing temperature for all abovementioned CSLs. For the calculation of K_{eff} and M_s, the nominal thicknesses of the magnetic layers are considered. When a 7 or 4 Å $Co_{60}Fe_{20}B_{20}$ layer is inserted between $Fe_{72}Co_8B_{20}$ and W, the resulting K_{eff} values after annealing at 340 °C and 400 °C are slightly lower than that comprising only $Fe_{72}Co_8B_{20}$. K_{eff} is most likely reduced due to intermixing of $Co_{60}Fe_{20}B_{20}$ with $Fe_{72}Co_8B_{20}$, resulting in a MgO/$Fe_{72}Co_8B_{20}$ interface relatively higher in Co content. According to *ab initio* calculations, a higher Co concentration at the interface reduces the interfacial anisotropy compared with that of MgO/Fe [3]. The saturation magnetization for samples with $Co_{60}Fe_{20}B_{20}$ insertion is higher than the one with only the $Fe_{72}Co_8B_{20}$-based storage layer. There can be two reasons behind the enhancement of saturation magnetization. (i) From a Stater-Pauling curve, we know that a maximum of saturation magnetization for Fe-Co alloy occurs at 30 at. % atomic percentage of Co. After complete boron extraction, $Fe_{72}Co_8B_{20}$ and $Co_{60}Fe_{20}B_{20}$ layers should theoretically become $Fe_{90}Co_{10}$ and $Co_{75}Fe_{25}$. During annealing, intermixing and interdiffusion of $Co_{60}Fe_{20}B_{20}$ and $Fe_{72}Co_8B_{20}$ take place, so that a reduction of the Fe atomic percentage in $Fe_{90}Co_{10}$ is highly possible, resulting in an increase of the saturation magnetization. (ii) The enthalpy of formation of Fe-W (−554 meV/atom) is more negative than that of Co-W (−84 meV/atom) [18].

Therefore, during sputtering and postdeposition annealing, a solid solution of Fe-W can be more easily formed than that of Co-W, which significantly reduces the magnetization. When $Co_{60}Fe_{20}B_{20}$ is inserted, it hinders the mixing between Fe and W and therefore, increases the magnetic moment.

These results indicate that it is difficult to improve the magnetic properties of CSL using only one W lamination due to significant interdiffusion taking place within the CSL between Fe-Co-B layers of different compositions, as well as between Fe and W.

B. Stack configuration and magnetic properties of dual-W composite storage layers

To reduce interdiffusion between Fe-Co-B layers of different compositions, different CSLs with dual-W laminations are deposited and magnetically characterized. The storage electrodes have the following composition, as shown schematically in Fig. 2: Ta 3/$Fe_{72}Co_8B_{20}$ 0.3/Mg 0.7/oxidation 30 s/Mg 0.5/dual-W CSLs /Mg 0.45/oxidation 10 s/Mg 0.4/$Fe_{72}Co_8B_{20}$ 0.3/W 2/Pt 3 nm. Six different configurations of dual-W CSLs are implemented with different types of central magnetic layer: $Fe_{72}Co_8B_{20}$, $Co_{60}Fe_{20}B_{20}$, or Co, and two different thicknesses of W laminations (0.1 or 0.15 nm), namely, (i) $Fe_{72}Co_8B_{20}$ 0.9/W 0.1/$Fe_{72}Co_8B_{20}$ 0.5/W 0.1/$Fe_{72}Co_8B_{20}$ 0.8 nm, (ii) $Fe_{72}Co_8B_{20}$ 0.9/W 0.15/$Fe_{72}Co_8B_{20}$ 0.5/W 0.15/$Fe_{72}Co_8B_{20}$ 0.8 nm, (iii) $Fe_{72}Co_8B_{20}$ 0.9/W 0.1/$Co_{60}Fe_{20}B_{20}$ 0.5/W 0.1/$Fe_{72}Co_8B_{20}$ 0.8 nm, (iv) $Fe_{72}Co_8B_{20}$ 0.9/W 0.15 /$Co_{60}Fe_{20}B_{20}$ 0.5/W 0.15/$Fe_{72}Co_8B_{20}$ 0.8 nm, (v) $Fe_{72}Co_8B_{20}$ 0.9/W 0.1/Co 0.5/W 0.1/$Fe_{72}Co_8B_{20}$ 0.8 nm, and (vi) $Fe_{72}Co_8B_{20}$ 0.9/W 0.15/Co 0.5/W 0.15/$Fe_{72}Co_8B_{20}$ 0.8 nm. These samples are used to investigate the magnetic and transport properties after annealing at 400 °C, which is the back-end-of-line process temperature to integrate STT MRAM devices with complementary metal-oxide-semiconductor (CMOS). They are compared to two reference conventional

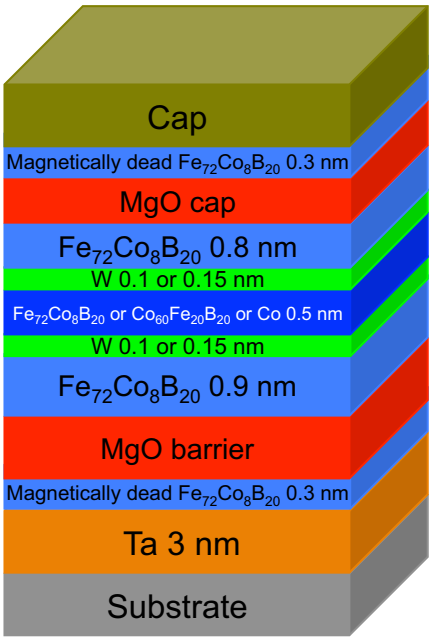

FIG. 2. Schematic representation of a dual-W CSL comprising two W laminations sandwiching a metallic magnetic material (e.g., $Fe_{72}Co_8B_{20}$, $Co_{60}Fe_{20}B_{20}$, or Co).

CSLs with the following structures: Ta 3/$Fe_{72}Co_8B_{20}$ 0.3/Mg 0.7/oxidation 30 s/Mg 0.5/CSL/Mg 0.45/oxidation 10 s/Mg 0.4/$Fe_{72}Co_8B_{20}$ 0.3/W 2/Pt 3 nm, where CSL is $Fe_{72}Co_8B_{20}$ 1.4/W 0.2/$Fe_{72}Co_8B_{20}$ 0.8 or $Fe_{72}Co_8B_{20}$ 1.3/W 0.2/$Fe_{72}Co_8B_{20}$ 0.9, which have only one W lamination and slightly different $Fe_{72}Co_8B_{20}$ thicknesses. Full pMTJ stacks are also grown with these storage layers for TMR characterization using the current-in-plane tunneling (CIPT) technique [19]. These full pMTJs have the composition Si/CIPT-bottom electrode/Pt 5/[Co 0.5/Pt 0.25]$_6$/Co 0.5/Ru 0.9/[Co 0.5/Pt 0.25]$_3$/Co 0.5/Ta 0.3/$Fe_{72}Co_8B_{20}$ 1.0/Mg 0.7/oxidation 30 s/Mg 0.5/CSL/Mg 0.4/oxidation 10 s/Mg 0.4/W 2 nm/top electrode. All investigated samples are deposited using an academic-grade Actemium sputtering tool with a base pressure in the order of about 10^{-8} Torr. After deposition, they are annealed at 400 °C. The resistance area (RA) product of pMTJs with conventional CSLs or dual-W CSL configurations, as measured by the CIPT technique, is 9 $\Omega\,\mu m^2$.

Figure 3 shows the M_s, K_{eff}, and TMR of the above-mentioned samples at room temperature. M_s and K_{eff} are calculated from the hysteresis loops measured by VSM. For the calculation of M_s and K_{eff}, the dead layer thickness is considered to be 3 Å. Dual-W CSLs with 1.5 Å W laminations exhibit lower magnetization than those with 1 Å W because thicker W yields more intermixing with magnetic layers. Therefore, the TMR is also lower in the case of 1.5 Å W laminations, compared with that of 1 Å W. Similarly, the lower magnetization observed in the samples with dual-W laminations compared with that in the corresponding ones with a single-W lamination in the CSL can be explained by a reduced intermixing of Fe with W in the latter case.

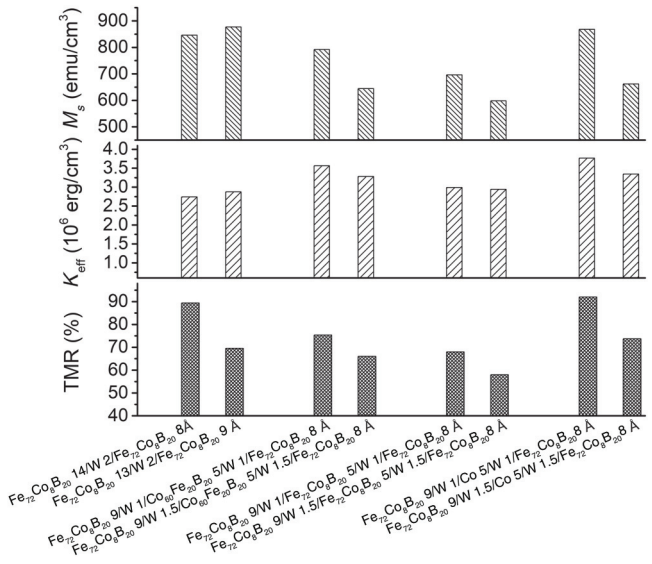

FIG. 3. Saturation magnetization (M_s), effective perpendicular magnetic anisotropy (K_{eff}), and TMR for the different configurations of the composite storage layer with single-W lamination and dual-W laminations. Samples are annealed at 400 °C for 10 min.

Among the three different magnetic insertions ($Fe_{72}Co_8B_{20}$, $Co_{60}Fe_{20}B_{20}$, and Co) investigated in dual-W CSLs, the one with Co insertion has the highest saturation magnetization, PMA, and TMR. This can be due, on one hand, to the reduced boron content in this sample and to the higher Curie temperature of the cobalt layer ($T_{c\text{Co}} = 1388$ K). Thus, 1 Å W dusting layers seem to be sufficient to absorb boron from the $Fe_{72}Co_8B_{20}$ layers and prohibit Co atoms from the central layer intermixing with the $Fe_{72}Co_8B_{20}$ layers and eventually reaching the MgO/$Fe_{72}Co_8B_{20}$ interfaces during annealing.

C. Temperature-dependent magnetic properties of dual-W composite storage layers

The magnetic properties of four selected samples (three dual-W CSLs with 1 Å W and one reference sample with the central part consisting of $Fe_{72}Co_8B_{20}$ 1.4/W 0.2/$Fe_{72}Co_8B_{20}$ 0.8 nm) are investigated by using a superconducting quantum interference device SQUID, as a function of measurement temperature, to demonstrate the beneficial influence of magnetically stiffening the central part of the CSL. First, the saturation magnetization is measured as a function of temperature from 50 to 650 K to extract the Curie temperature by fitting with the Bloch $T^{3/2}$ equation, $M_s = M_0[1 - (T/T_c)^{3/2}]$, where M_0 represents the saturation magnetization at 0 K. The result is shown in Fig. 4(a). From the intercept with the temperature axis, the Curie temperatures are 994 ± 19 K for the reference sample and 928 ± 18 K, 873 ± 23 K and 993 ± 16 K for dual-W CSLs with central magnetic components of $Co_{60}Fe_{20}B_{20}$, $Fe_{72}Co_8B_{20}$, and Co, respectively. Notably, the magnetization departs from the Bloch law and sharply increases below 200 K. For each material, this is interpreted as the temperature below which the dead layer becomes ferromagnetic; this gives an additional contribution to the net magnetization of the storage layer. The Curie temperature of the reference CSL (blue curve in Fig. 4) is high (994 K) because of the larger thickness of the $Fe_{72}Co_8B_{20}$ layer above the MgO barrier. Compared to $Fe_{72}Co_8B_{20}$ insertion, dual-W CSLs, with Co-rich $Co_{60}Fe_{20}B_{20}$ or pure Co insertions have higher T_c values.

Although the CSL with single-W insertion has a large T_c, similar to that of the Co-inserted dual-W CSL, the K_{eff} is comparatively much lower in the former, as shown in Fig. 4(b). Moreover, its in-plane $M(H)$ loops exhibit two linear regions, as shown in Fig. 5(a); this signifies a weak coupling between the two magnetic layers across the 2 Å W lamination and/or a second-order anisotropy contribution [20]. In contrast, the three configurations with dual-W CSLs exhibit a linear in-plane hysteresis loop, as displayed in Figs. 5(b)–5(d), which suggests strong ferromagnetic coupling across the two extremely thin W

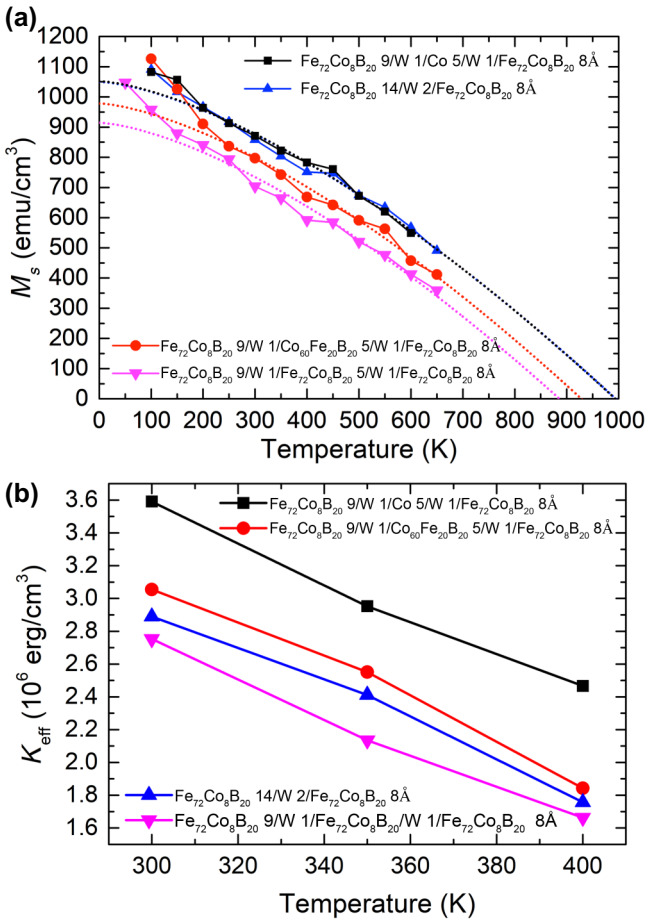

FIG. 4. (a) Saturation magnetization as a function of temperature. The dotted lines are fits according to Bloch $T^{3/2}$ law to extract Curie temperatures for each storage layer. (b) Effective perpendicular anisotropy energy density as a function of temperature for 300, 350, and 400 K.

laminations and negligible contribution from second-order anisotropy. Notably, from Fig. 4(b), the PMA of dual-W CSLs with $Co_{60}Fe_{20}B_{20}$ and Co insertion are, respectively, 5% and 24% higher than that of the conventional CSL at room temperature. Among the three types of dual-W CSLs, the one with Co insertion provides the highest PMA at room temperature and at high temperature (400 K). Moreover, it has the highest T_c (994 K) and exhibits the highest TMR among all of the configurations. These features are ascribed to the high Curie temperature of the Co layer, which is higher than that in all other investigated magnetic materials (700–1000 K). Co magnetically stiffens the magnetization of the CSL, which reduces the density of thermal fluctuations at room temperature. Moreover, the total amount of boron is reduced by 23% in the Co-inserted dual-W CSL, compared with the other studied structures, which reduces the remaining boron content at the $MgO/Fe_{72}Co_8B_{20}$ interfaces after annealing.

As a result, K_{eff} is significantly increased and the thermal decrease of the M_s, K_{eff}, and TMR between 4 K and 300 K is weaker in the dual-W CSL containing a Co insertion than that in the other samples. Hence, a dual-W CSL comprising a central layer of Co constitutes a promising storage layer for STT MRAM applications operating over a wide range of temperature, such as automotive applications.

D. Thermal variation of magnetotransport properties of STT MRAM cells

After an investigation of the magnetic properties at wafer level, memory cells are patterned out of two pMTJ wafers, one with the reference CSL and the other one with the Co-inserted dual-W CSL. To compare magnetic stiffness between the above two types of storage layer in the patterned STT MRAM cells with different diameters, resistance versus magnetic field [$R(H)$] loops are measured from room temperature to 110 °C. Fig. S1 within the Supplemental Material [21] shows temperature-dependent normalized coercivity (H_C) as a function of temperature for various cell diameters. Because of temperature limitation of the electrical characterization setup, H_C is measured up to 110 °C. This plot is then extrapolated by using Eq. (2) to extract the blocking temperature (T_B) at which the storage layers of the cells become superparamagnetic at the characteristic timescale of the measurement (i.e., ms) [22].

$$H_C(T) = H_C(0)\left[1 - \left(\frac{T}{T_B}\right)^{0.5}\right]. \tag{2}$$

The calculated blocking temperatures as a function of electrical cell diameters are presented in Fig. 6. T_B reduces with cell diameter, as expected. Co-inserted dual-W CSLs exhibit comparatively higher T_B values than those of the reference CSLs, which suggests that they also have higher Δ values, since they are proportional to T_B. For confirmation, the thermal stability factor of memory cells with a diameter of 80 nm are calculated from statistical measurements of the resistance versus magnetic field [$R(H)$] loops using the switching field distribution model [23,24]. Following this model, the switching probability of the cells is fitted to derive Δ:

$$P_{\text{sw}}(H) = 1 - \exp\left\{-\frac{f_0 H_k}{2r}\sqrt{\frac{\pi}{\Delta}}\,erfc\left[\sqrt{\Delta}\left(1 - \frac{H}{H_k}\right)\right]\right\}. \tag{3}$$

where f_0, r, and H_k are the attempt frequency (1 GHz), field sweep rate (typically 40 kOe/s), and anisotropy field, respectively. For each memory cells, 100 $R(H)$ loops are measured at different temperatures. Values of Δ in parallel and antiparallel configurations are calculated for about 100 memory cells. Figure 7(a) shows the distribution of Δ

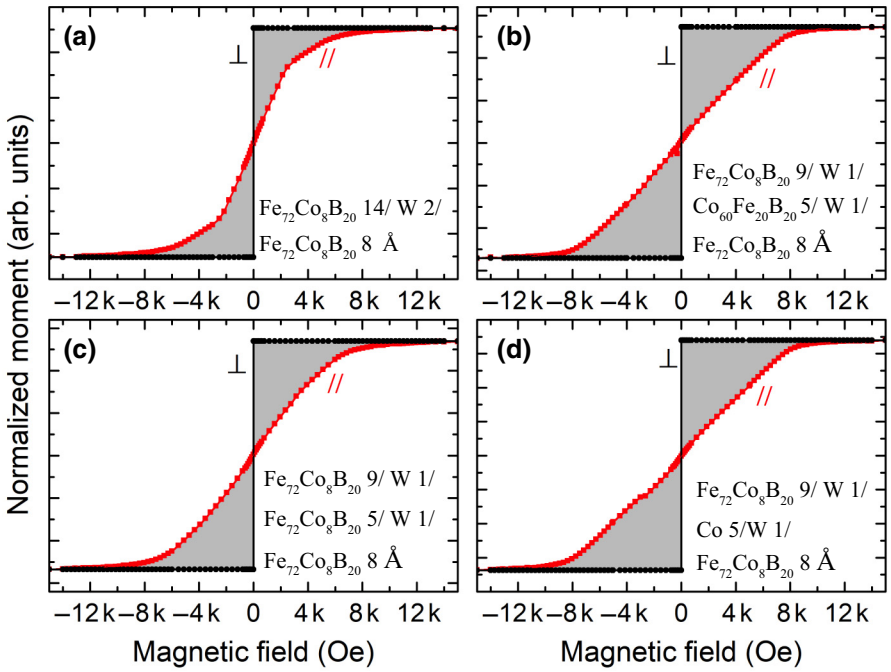

FIG. 5. (a–d) Measured in-plane $M(H)$ loops (//) in red at 300 K and assumed out-of-plane $M(H)$ loops (⊥) in black for the four different storage layers. Gray region is the area between in-plane and out-of-plane loops, which is measured to calculate K_{eff} in Fig. 4(b).

(average value and distribution width are represented on the graph by the error bars) as a function of temperature of memory cells comprising a reference CSL and Co-inserted dual-W CSL. To select samples with the same diameter (80 nm), the electrical diameters (D) are determined from the resistance of the devices and the wafer-level RA product of the pMTJ stacks, which is measured by the CIPT method prior to patterning. The TMR of memory cells with diameters of about 80 nm is also derived from the $R(H)$ loops measured at different temperatures above room temperature and are plotted in Fig. 7(b). Both Δ and TMR of the memory cells with Co-laminated dual-W CSL are, respectively, 17% and 23% higher, on average, than those of the reference CSL at 50 °C. Linearly extrapolating towards higher temperature, these enhancement factors are expected to be 50% and 12%, respectively, on average, at 150 °C. We use linear fitting and extrapolation of the TMR because it is found that the magnon-interaction model [25,26] of TMR deviates from linearity by less than 2.5% up to 150 °C, as explained in Fig. S2 within the Supplemental Material [21]. The rate of thermal decrease

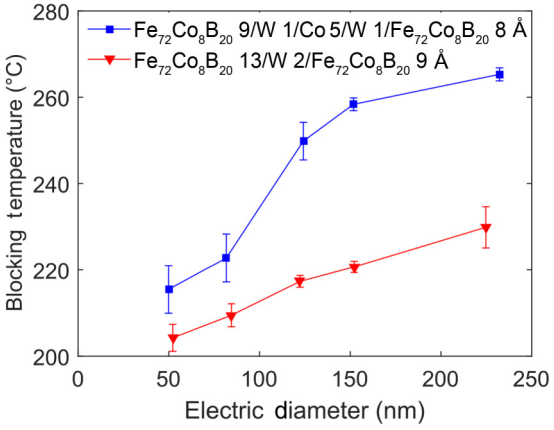

FIG. 6. Blocking temperature as a function of electrical diameter of memory cells comprising the reference CSL and the Co-laminated dual-W CSL. Blocking temperature is derived from $H_C(T)$, according to Eq. (2).

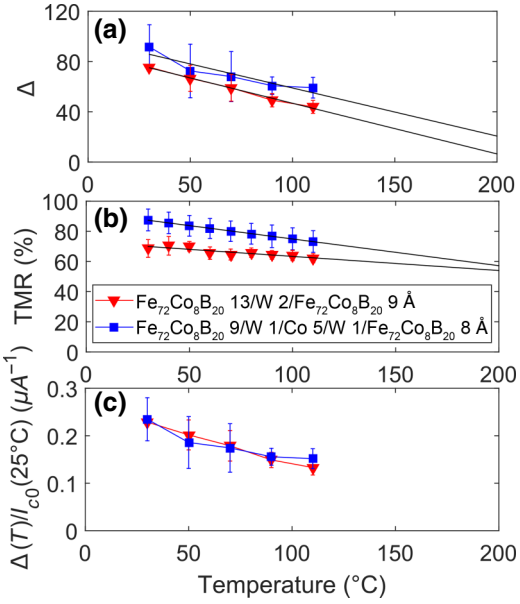

FIG. 7. (a) Thermal stability factor (b), TMR, and (c) practical STT efficiency as a function of temperature of memory cells of 80 nm diameter for reference CSL and Co-laminated dual-W CSL.

of Δ (i.e., $d\Delta/dT$) is comparable for both storage layers, similarly to the rate of variation of K_{eff} versus temperature (Fig. 4). However, the rate of thermal decrease of TMR in the patterned memory cells, as presented in Fig. 7(b), is slightly larger for the dual-W CSL than that for the CSL with single-W lamination. This indicates that the TMR is more sensitive to thermal fluctuations of the magnetic layer adjacent to the MgO barrier, due to its interfacial character, whereas the thermal stability also involves the bulk properties of the storage layer. We believe that the thermal decrease of TMR and Δ can be reduced by slightly increasing the thickness of the $Fe_{72}Co_8B_{20}$ layer above the MgO barrier. The practical STT efficiency $[\Delta(T)/I_{c0}(25\,^{\circ}\text{C})]$ is calculated and plotted in Fig. 7(c). The critical switching current (I_{c0}) at room temperature ($\sim$25 °C) is calculated by the voltage-field phase diagram method, which is detailed in Figs. S3 and S4 within the Supplemental Material [21]. Although I_{c0} for the dual-W CSL (390 μA) is larger than that of the reference (330 μA), the STT efficiency is similar due to a larger gain in Δ.

III. CONCLUSIONS

We demonstrate that the proposed dual-W CSL design brings extra freedom to sandwich different magnetic materials between two W laminations to further optimize the magnetotransport properties of STT MRAM cells. Co- and $Co_{60}Fe_{20}B_{20}$-inserted dual-W CSLs result in higher PMA at room temperature and up to 110 °C, compared with that of the conventional single-W inserted composite storage layer. Moreover, patterned STT MRAM cells with diameters of 80 nm, comprising Co-inserted dual-W CSL, exhibit higher Δ and TMR values than those of conventional CSLs over the investigated temperature range without any loss in STT efficiency. These improvements are ascribed to prohibition of Co interdiffusion towards $Fe_{72}Co_8B_{20}$/MgO interfaces thanks to the W laminations, reduction of overall residual boron content at the $Fe_{72}Co_8B_{20}$/MgO interfaces, and, most importantly, to an overall magnetic stiffening of the whole storage layer associated with the high Curie temperature of cobalt. Therefore, MTJs comprising such dual-W lamination CSLs with Co-rich inserted layers can be advantageous for STT MRAM that is required to operate over a wide range of temperature, such as for automotive applications.

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