Memcomputing and Nondestructive Reading in Functional Ferroelectric Heterostructures

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Multiple nonvolatile and well-separated capacitive states can be obtained in a two-terminal ferroelectric capacitor setup by fine tuning the polarization switching process. This approach allows for the implementation of memcomputing (same platform for storage and computing) capable ferroelectric structures. Digital and analog storage modes are exemplified in this work together with an algorithm for simple binary computation functions such as OR/NOR and AND/NAND for data processing on the same device. Results are obtained by controlling the polarization switching process in ferroelectric multilayers such as $Pb(Zr_{0.2}Ti_{0.8})O_3/SrTiO_3/Pb(Zr_{0.2}Ti_{0.8})O_3$ and $Pb(Zr_{0.2}Ti_{0.8})O_3/BaTiO_3/Pb(Zr_{0.2}Ti_{0.8})O_3$. Besides memcomputing, these results can be used for nondestructive capacitive reading of information in simple ferroelectric capacitors or can open the way toward applications such as neuromorphic and chaotic circuits.

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I. INTRODUCTION

One of the realities of present and future technologies is the ever-increasing need for computing speed and high-density information storage. This technological race gives rise to numerous challenges related to various limitations of Moore's law, such as the rising cost of chip manufacturing and physical limitations due to size reduction [1]. For these reasons the concept of memcomputing is gaining traction since the processing and storing of information is performed on the same physical platform [2,3]. This new paradigm relies on passive circuit elements with memory function, such as memristors, memcapacitors and meminductors [4,5]. Unfortunately, there are only a small number of systems exhibiting capacitive switching behavior [6–11]. Conceptually, memcapacitors are different from already existing electrically programmable capacitors such as varactors and typical ferroelectric capacitors: the set capacitance values are maintained without a power supply and, most importantly, the read operation for each state is nondestructive [12].

Ferroelectric materials have shown great promise for nonvolatile memory applications, considering that the two polarization orientations can be associated to the two Boolean bits used in digital computing. The exploitation of commercial ferroelectric random access memory to its full potential is severely hindered by the destructive reading process of the stored information, which requires multiple rewriting operations. These repeated cycles will eventually alter the stability of the ferroelectric phase and compromise device operation [13,14]. A nondestructive capacitive reading will resolve this disadvantage; however, inducing different capacitive states in a ferroelectric structure can be associated with the partial switching of polarization or with a shifting of a capacitance-voltage loop due to an internal field, leading to different capacitance values for the two stable polarization states. Unfortunately, the first case is a transitory phenomenon for ideal structures, and for the second case the capacitance difference between the two values is insignificant and cannot be used effectively. Currently, the link between the memcomputing field and ferroelectric materials is realized with ferroelectric-based memory structures exhibiting resistive switching behavior [15–20]. For logic gates, ferroelectric-based structures (e.g., graphene-ferroelectric metamaterials and organic ferroelectric multilayers) can be used for digital computing [21,22].

In this article we demonstrate memcapacitive effects in structures based on ferroelectric-insulator-ferroelectric (F-I-F) thin-film layers. The findings are corroborated by repeatable experimental measurements and theoretical modeling demonstrating the presence of multiple, stable and individually addressable capacitive states. In addition, the capacitance states for these structures depend on the past states along the system evolution path. This property can be harnessed for logic operations such as OR/NOR and AND/NAND while storing the result on the same physical device, in accordance with the parallel computation

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philosophy [23]. Finally, it is shown that intermediate capacitance states can be obtained in between two extreme values, which is the equivalent of an analog-type memory, a behavior that can be exploited in neural networks mimicking the functionality of the brain.

II. THEORETICAL ASPECTS

Sequential switching of ferroelectric polarization in three-layer structures such as $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT)/$SrTiO_3$ (STO)/$Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) was demonstrated both experimentally and theoretically in [24]. It was shown that there are four different polarization states that are stable in time and available for information storage. The theoretical arguments for proving the multi-polarization states in the *F-I-F* structures are based on the Landau-Ginzburg-Devonshire (LGD) model [24].

The free energy of the three-layer structure was obtained as a function of the polarization state in each ferroelectric layer, revealing that the *F-I-F* device studied has four equilibrium states with distinct polarizations [Fig. 1(a)]. In addition, it will be shown below that this setup also has distinct capacitance states. Starting from a given state of the structure, it is possible to map its evolution as the voltage is modified. Figure 1(b) shows the positive branch of the theoretical hysteresis curve obtained using the LGD theory detailed in [24]. In order to prove the nondestructive reading operation in the *F-I-F* structure, one must obtain different capacitance values between the available polarization states. If the system is initially set in a stable state where the polarizations in both ferroelectric layers are set to point in the upward direction (toward the top electrode), as the voltage is continuously increased, the system will

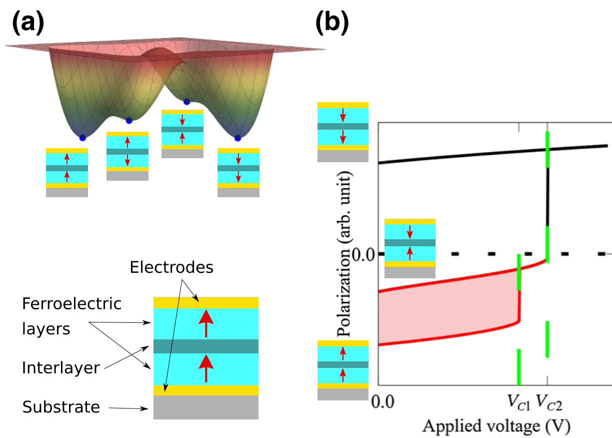

FIG. 1. The theoretical description of stable ferroelectric states and the switching between them based on the LGD model. (a) The free-energy landscape (energy vs polarization of each ferroelectric layer) of an *F-I-F* structure in equilibrium. (b) The positive polarization hysteresis branch of an *F-I-F* heterostructure and the schematic representation of the polarization orientation in each ferroelectric layer for different states.

remain in the initial state [see the corresponding minimum of the free-energy function in Fig. 1(a)] until $V = V_{C1}$. At this point the system is able to switch to the next available equilibrium state that corresponds to the case where the polarization in each ferroelectric layer has different orientation (i.e., one is pointing downwards while the other is point upwards). One important note is that the new state is considered stable because it is maintained when the voltage is slowly returned to 0 [see the red curve hysteresis in Fig. 1(b)]. Continuing to increase the voltage beyond V_{C1}, the system will eventually reach its final state where the two polarizations are pointing downwards at $V = V_{C2}$. By approximating the entire structure with an equivalent circuit of three capacitors connected in series one can write the total equivalent dielectric constant of the three-layer structure as follows:

$$\varepsilon(V) = (d_1 + d_i + d_2)\left[d_1\left(\frac{1}{\varepsilon_0}\frac{dP_1(V)}{dE_1(V)} + 1\right)^{-1} + \frac{d_i}{\varepsilon_i} + d_2\left(\frac{1}{\varepsilon_0}\frac{dP_2(V)}{dE_2(V)} + 1\right)^{-1}\right]^{-1}, \quad (1)$$

where ε_i is the dielectric constant of the insulator interlayer, and $P_1(V)$, $E_1(V)$, $P_2(V)$, and $E_2(V)$ are the polarizations and electric fields in the two ferroelectric layers. Using Eq. (1) and the theoretical model for the three-layer heterostructure [24], one can determine that the partial reversal of polarization [i.e., the intermediate state in Fig. 1(b)] leads to an increased dielectric constant of the structure compared to the initial and final states. This result is fundamentally different than the simple ferroelectric capacitor case where the two available polarization states have indistinguishable capacitance values. Thus the theoretical description demonstrates the existence of *four* stable polarization states and, more crucially, two distinct capacitance states: a high capacitance state (HCS) and a low capacitance state (LCS).

III. THE MEMCAPACITIVE EFFECT

It is now clear from the theoretical results that the nondestructive reading process could be achievable in *F-I-F* structures by a capacitance measurement that is a nondestructive process, where the amplitude of the signal is much lower than a coercive voltage; however, a more compelling argument is the experimental verification. For this reason *F-I-F* capacitors have been fabricated using $Pb(Zr_{0.2}Ti_{0.8})O_3$ as the ferroelectric material and two types of insulating materials: STO and $BaTiO_3$ (BTO). While the latter is known to be ferroelectric at room temperature, it has a much lower saturated polarization compared to the PZT layers such that its electrostatic contributions at the PZT interfaces are similar to an insulator.

The main result in Fig. 2(a) is the dynamic hysteresis measurement for the PZT-BTO-PZT structure, showing the clear decoupling of polarization switching in the two ferroelectric layers predicted by the theoretical model in Fig. 1. Changing the capacitive state can be achieved with a simple pulse sequence shown in Fig. 2(c). A negative −18-V dc pulse will set the polarization toward the top electrode interface in both ferroelectric layers, which is attributed to an LCS. The following positive +7-V dc pulse will reverse the polarization toward the bottom electrode in only one ferroelectric layer, which brings the structure to an HCS. Moreover, the two states have different dielectric losses, suggesting that the loss mechanism depends on the relative orientation of polarizations in the two PZT layers (see the Supplemental Material [25]). For a quantitative description of the differences between the dielectric properties of the two states, one can define the relative variation of capacitance between the two polarization states (RPC):

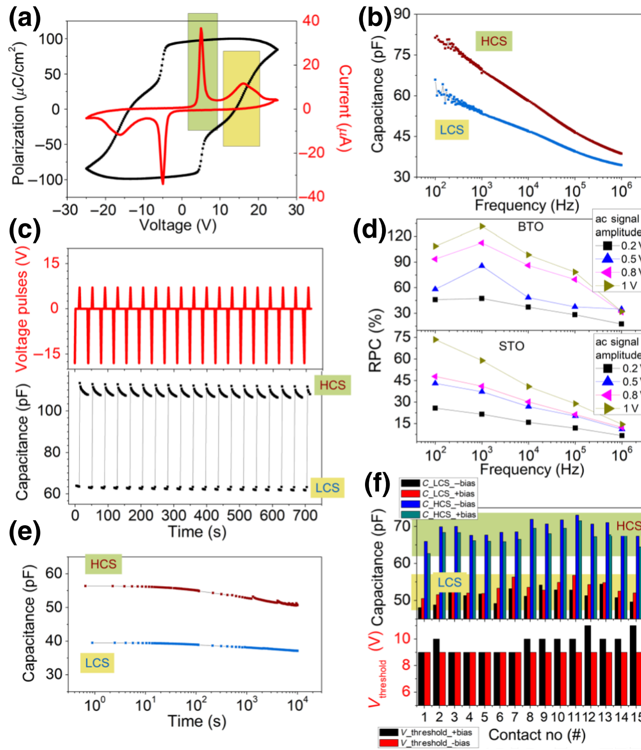

FIG. 2. Two different capacitance states. (a) The hysteresis loops obtained for a complete switching cycle for the case of a BTO interlayer exhibiting four switching peaks in current-voltage characteristics accompanied by a steplike increase in the polarization loop; the extreme peaks situated at higher voltages correspond to a totally reversed polarization, where the ferroelectric polarization is either oriented *up*, toward the top interface in both ferroelectric layers, for negative voltages, or *down*, toward the bottom electrode in both ferroelectric layers, for positive voltages; the intermediate peaks are obtained when the applied voltage changes its polarity and indicates a partial reversal of polarization in only one ferroelectric layer, generating either a head-to-head or a tail-to-tail configuration between the polarizations of the two ferroelectric layers. (b) The capacitance vs frequency, using 0.2-V ac signal, measured after setting HCS and LCS states, respectively. (c) Voltage pulse sequence, combining high-amplitude and low-amplitude pulses with 0.1 s duration, used to repeatedly change the capacitance of the system between LCS and HCS; the capacitance values are measured at 1 kHz frequency and with 0.5-V ac signal. (d) RPC ratios for the BTO and STO interlayer cases, respectively, for different frequencies and ac signal amplitudes. (e) evolution of the two distinct capacitance states, during the 104 s time period, measured at 1 kHz frequency and 0.2 V amplitude of the ac signal. (f) Distribution of capacitance values for HCS and LCS, measured at 1 kHz and 0.5-V ac signal, and distribution of the voltage threshold defined as the voltage necessary for switching from LCS to HCS for 15 different contacts.

$$\delta_{\mathrm{RPC}}(\%) = \frac{C_{\mathrm{HC}} - C_{\mathrm{LC}}}{C_{\mathrm{LC}}} \times 100, \tag{2}$$

where C_{HC} and C_{LC} are the HCS and LCS capacitance values, respectively. The RPC values for both structures are shown in Fig. 2(d) for different frequencies and amplitudes of ac signals. The BTO interlayer case has higher RPC values in the lower-frequency regime and they become approximately equal to the STO case toward 100 kHz. For both cases the RPC decreases at higher frequencies, the differentiation between the two capacitive states being significant in the low-frequency regime. The dielectric behavior of the two states is better represented as a capacitance vs frequency measurement in the 100 Hz to 1 MHz range, presented in Fig. 2(b) (the dielectric loss for the same frequency range is shown in Fig. S2 in the Supplemental Material [25]). It is clear that the most important contribution to the capacitance of the structure is achieved toward the static frequency regime due to the different relative orientations of polarization in each ferroelectric layer and the induced electrostatic boundary conditions at the interfaces. When the frequency is increased, the charges contributing to the compensation of polarization charges and associated depolarization field, as well as the space charge regions that may develop at ferroelectric-insulator or ferroelectric-electrode interfaces, cannot follow the rapid changes of the ac field, and the capacitive response is diminished, evolving toward the intrinsic dielectric properties of the constituent layers. This behavior, together with the two capacitance states with different capacitance and dielectric loss values, is observed for both the PZT-STO-PZT and PZT-BTO-PZT structures. Figure 2(d) also shows that the relative difference between LCS and HCS, measured by the RPC value, becomes larger toward higher values of the ac signal amplitude. This can be associated with the increase of capacitance as the ac signal amplitude approaches the magnitude of the coercive voltage.

An important aspect of information storage is the retention property, which was monitored over time for both the

HCS and the LCS states [see Fig. 2(e)] for up to 10^4 s. The nondestructive aspect of the reading operation is also emphasized. It can be observed that during the continuous 10^4 s capacitance measurement, there is only a 10% drop in the capacitance of HCS; however, the net difference between the two states is clearly maintained. This behavior reflects that the partially reversed states of the system, while stable from an energy point of view, will tend to evolve toward the totally reversed states that are energetically more stable and in consequence have a lower capacitance. The ability to differentiate between the HCS and LCS is repeatable for many contacts, as can be seen in Fig. 2(f).

IV. OPERATING LOGIC FUNCTIONS

As was shown above, the three-layer heterostructures clearly exhibit four polarization states but only two different capacitance states. Changing between these system states is schematically illustrated in Fig. 3.

The possibility of switching between polarization states with distinct associated capacitance values using two different voltage pulses can be used to build algorithms for logic functions. The logic operation is determined by an appropriate choice of the initial state followed by two particularly defined pulses with different amplitudes and polarities as input logic "0" (L0) or input logic "1" (L1), which can lead to stabilization of different system states that can be read nondestructively by the capacitive method. It is therefore possible to realize Boolean logic functions AND/NAND and OR/NOR using two binary input signals, as illustrated in Figs. 4(a) and 4(b).

Thus, in Fig. 4(a) the system is initially set in a low capacitive state by applying a negative high-amplitude pulse, for which the polarization is oriented in the same direction in both PZT layers. If a positive low-amplitude voltage pulse defined as L0 is applied, the system will evolve into a partially reversed polarization state with a high capacitance value. Furthermore, the system can remain in the same state if the same pulse is applied or can be changed to a totally reversed polarization state with a low capacitance value if a positive high-voltage pulse is applied, defined as L1. If the initial state is subjected to an L1 pulse, the system will change to a totally reversed state with low capacitance where it will remain whether a logic L0 or L1 pulse is further applied. Thus,

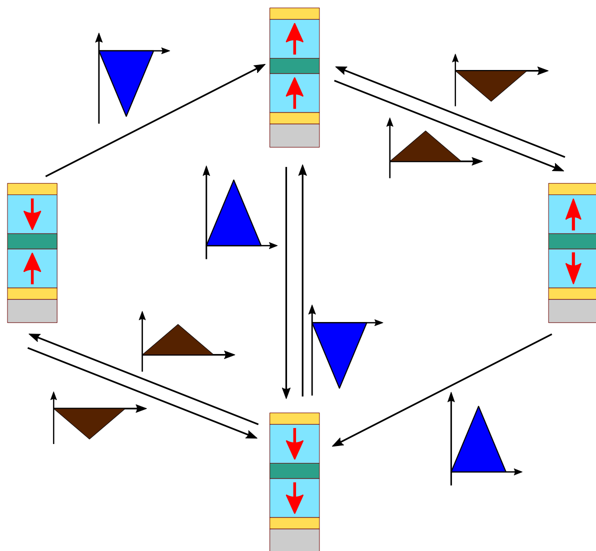

FIG. 3. Schematic representation of the switching possibilities between the four polarization states with the two different capacitive values using corresponding signals. The red and blue triangular pulses are the low- and high-amplitude voltage pulses, respectively.

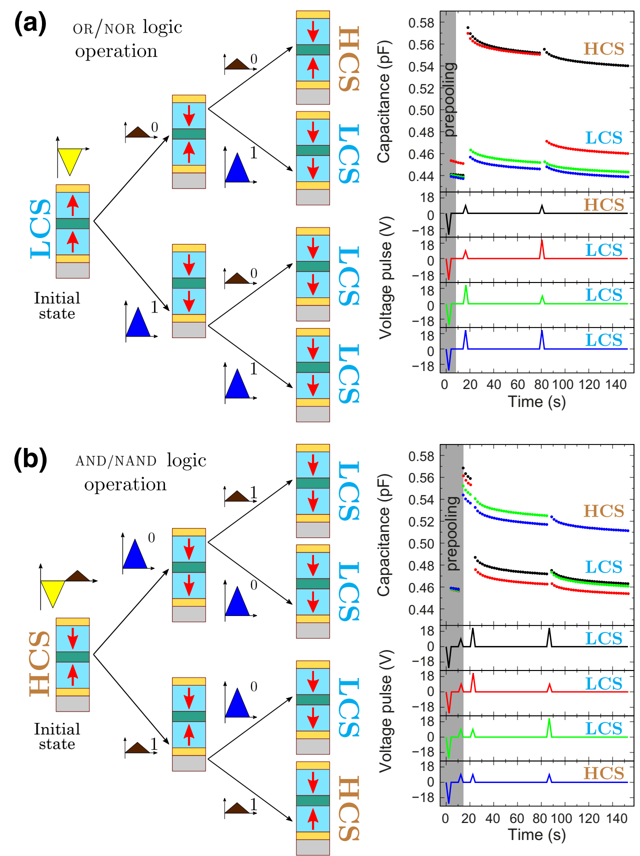

FIG. 4. Logic operation using an *F-I-F* capacitor. The representation of the polarization states in an *F-I-F* structure during different stages (initialization and computation) of a logic operation for the OR/NOR case (a) and for the AND/NAND case (b), together with the corresponding simulations of the logic operations obtained by changing the capacitance state (HCS or LCS) of the system using different combinations of pulses. The HCS and LCS states can have 0 or 1 values associated for logic operations and the results are memorized on the computation cell and can be accessed at any time.

the system will be set to an HCS if only two consecutive L0 pulses are applied, otherwise the system will be in an LCS for any other combination of two pulses. By associating the two capacitive states with Boolean values, the final states are the result of an OR(HCS, 0; LCS, 1) or NOR (HCS, 1; LCS, 0) logic operation, as summarized in Table S1 in the Supplemental Material [25]. Similarly, in Fig. 4(b) the initial state of the device is set to a partially reversed polarization configuration with a corresponding high capacitance value using a negative high-amplitude voltage pulse followed by a positive low- amplitude one. This scenario allows the implementation of an AND/NAND logic operation. The L0 and L1 are defined for this case as a positive high-amplitude voltage pulse and a positive low- amplitude voltage pulse, respectively. It is clear from Fig. 4(b) that only the consecutive appliance of two L1 inputs determines a final HCS, while for the remaining three input combinations an LCS is obtained (see also Table S2 in the Supplemental Material [25]).

At this point, the proposed *F*-*I*-*F* structure shows simultaneous information storage and computation functions, since the result of the logic OR/NOR or AND/NAND operations can be stored as HCS or LCS. Furthermore, such devices can be used to realize cascade computations for defined operations. It can be easily verified that for the case of an OR operation, multiple combinations of L1 or of L1 with L0 inputs will leave the system in a low capacitive state and only a combination of L0 inputs will change it to a high capacitive state. The same results apply for multiple AND operations.

V. ANALOG STORING SCHEME

The remarkable properties of the *F*-*I*-*F* devices presented thus far can be regarded as extreme cases, in that the multi-polarization states used until now are fully saturated.

Further investigations reveal that intermediate capacitance states can be set using different voltage amplitudes for the writing pulses [see Fig. 5(a)]. Until now, an intermediate state referred to the case where the polarizations in the two ferroelectric layers of the *F*-*I*-*F* device had opposite orientations but are fully saturated. For this case, however, the intermediate values of capacitance can be associated to the partial reversal of polarization in the two PZT layers, as schematically presented in Fig. 5, where ferroelectric layers are formed by multiple domain regions. After the −25-V prepolarization pulse, the system is in a complete reversal of polarization toward the top electrode interface. When positive voltage pulses are applied, different ferroelectric domains will start to reverse toward the bottom electrode interface. From an electrostatic point of view any combination of ferroelectric polarization orientations is possible between the monodomain ferroelectric layers, as it was shown in Secs. II and III. Thus, for any

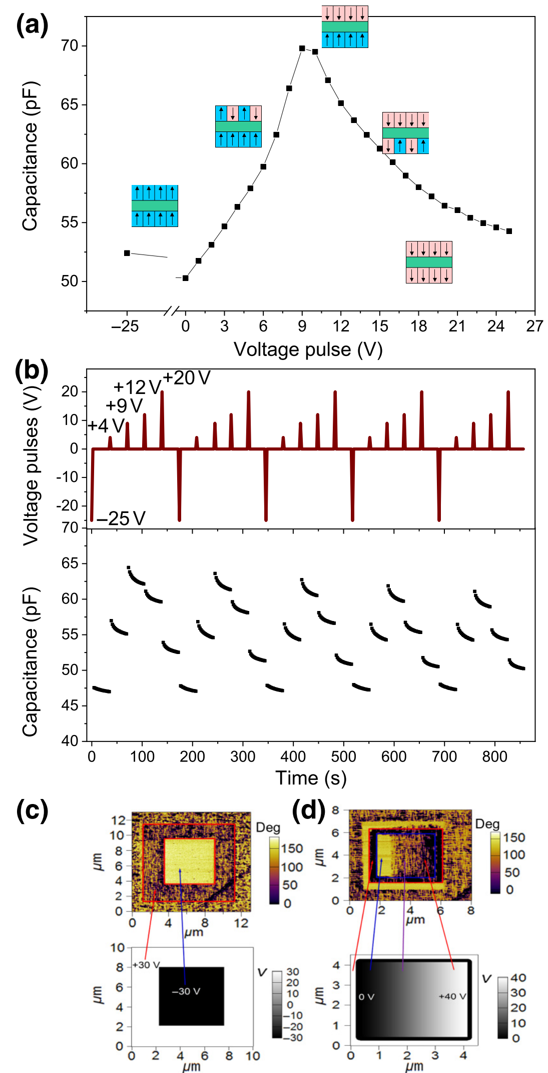

FIG. 5. Multiple stable states with continuous capacitive values. (a) A continuous spectrum of capacitance values, with stable intermediate states measured for the STO interlayer case at 1 kHz frequency with 0.5-V ac signal; insets show schematic illustrations of polarization configurations associated with distinct capacitive states. (b) An example of a voltage sequence combining pulses with different amplitudes and polarities used to access different capacitive states. (c) The piezoresponse phase signal obtained using the poling map: the upper PZT layer present totally reverses polarization toward the surface for negative applied bias (bright central rectangular zone) while for positive bias the polarization remains partially reversed, forming with 180° domain structure. (d) The piezoresponse phase signal obtained by applying the poling map with a voltage gradient on the totally reversed polarization area from (c): the switching of polarization takes place gradually with increasing the amplitude of voltage; different degrees of partial switching of polarization are obtained in the 8–37 V range.

complete or partially reversed polarization in the ferroelectric layers, the structure has areas with high capacitance states and areas with low capacitance states, respectively.

The equivalent capacitance of the structure will cover the range between the LCS and the HCS, such that

$$C_{\mathrm{LC}} \leq \alpha C_{\mathrm{LC}} + \beta C_{\mathrm{HC}} \leq C_{\mathrm{HC}}, \tag{3}$$

where $\alpha + \beta = 1$ are the ratios of the areas corresponding to LCS and HCS, respectively. The sum $\alpha C_{\mathrm{LC}} + \beta C_{\mathrm{HC}}$ is the equivalent capacitance of the structure, considering that the multiple areas with C_{LC} and C_{HC} form a parallel capacitance connected circuit. These intermediary polarization states have been evidenced in current-voltage and polarization-voltage characteristics shown in Fig. S4 within the Supplemental Material. All data exhibit different remnant polarization values, with an almost rectangular shape and no significant back-switching contribution when the voltage drops to zero. This assumption is also experimentally verified by performing piezoresponse atomic force microscopy (PFM) investigations in the three-layer structure. A special poling procedure is designed. Firstly, a rectangular area is subjected to -40 V applied voltage in order to ensure a complete reversal of polarization. After this treatment, the PFM tip is used to scan the same area from left to right while the applied voltage on the tip is gradually increased [see Fig. 5(d)]. The PFM scan in the phase mode revealed that the polarization switching, reflected in the domain structure, took place gradually from a totally up state to totally down one, with a mixed structure of 180° domains in between.

The PFM results are in very good agreement with multiple studies in the literature showing the apparition of 180° nanoscale poly-domain configurations in multilayered ferroelectric-insulator structures [26,27]. Such nonhomogeneous systems also present stable intermediary states, corresponding to incompletely switched polarization, over long periods of time, due to a wide distribution of coercive voltages in different nanoscale regions [28,29]. These results can be used for constructing an analog-type ferroelectric memory or artificial synaptic circuits, with the demonstrated property of nondestructive reading [30].

All partially switched polarization states in the head-to-head and tail-to-tail polarization configurations of the two constituent layers exhibit a relaxation on the values of the attributed capacitance with time. The drop is significant in the first seconds before converging toward a stable value. This phenomenon is related to the presence of the insulator interlayer and the discontinuity of the polarization charges, which is mandatory for obtaining this sequential polarization switching and different capacitive states. In addition, large depolarization fields are not uniformly distributed in the ferroelectric (FE) layers (since one interface is in contact with a metallic electrode and the other with an insulator layer). Also, different defects and structural differences (domains, domain walls, pinning centers, etc.) will appear in these structures compared to simple FE layers. These defects have a significant role in the switching dynamics, for example a voltage pulse sets a particular configuration of polarization and domain distribution, but reducing the voltage to zero could determine a back-switching of polarization in a certain volume of the layers in such a way that the system evolves toward a minimum energy. Another explanation could be related to the redistribution of charges inside the structures during switching in order to compensate the newly induced polarization state. This process could be continued after removing the applied voltage or could be delayed compared with the moment of the switching. Even if this relaxation seems to be a general phenomenon for all polarization states, the fact remains that these systems present a good separation and differentiation between the states at all measured moments.

One should also keep in mind that this study is a proof of concept for nondestructive reading of polarization states and many aspects such as the relaxation of the capacitance are suitable for separate study. A better choice of constituent materials, optimization of layer thicknesses and operational optimization (time duration of the voltage pulse, ac signal amplitude, frequency) could solve the capacitance relaxation problem.

VI. CONCLUSION

Information storage and processing with nondestructive reading operation are demonstrated in *F*-*I*-*F* thin-film multilayered heterostructures. Two distinct, well-separated and nonvolatile capacitive states have been obtained for two test devices, PZT-STO-PZT and PZT-BTO-PZT, associated with different polarization configurations of the two ferroelectric layers. The capacitor memory setup presented has a wide variety of uses, with demonstrated capabilities as nonvolatile memory with nondestructive reading and the ability to perform binary logic operations on the same chip. These properties open the way for building parallel computation systems extending beyond the von Neumann architecture. Also, by specially designed algorithms the current circuit architecture based on classic logic gates can be simplified and optimized, leading also to significantly reduced power consumption and reduced cost of manufacturing.

Furthermore, by switching the polarization in each ferroelectric layer gradually, quasistable states can be obtained, presenting a continuum of capacitance values. This opens the way for nonvolatile analog memory development with nondestructive reading capabilities for constructing neuromorphic or chaotic circuits.

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[1] Moore's Law Reaches Its Limit! Developing a New Architecture to Solve the Combinatorial Optimization Problem, http://journal.jp.fujitsu.com/en/2017/02/15/01/ (2017).

[2] Y. V. Pershin and M. D. Ventra, in 2014 International Workshop on Computational Electronics (IWCE) (IEEE, Paris, France, 2014), pp. 1–2.

[3] M. Di Ventra and F. L. Traversa, Perspective: Memcomputing: Leveraging memory and physics to compute efficiently, J. Appl. Phys. **123**, 180901 (2018).

[4] L. Chua, Memristor-the missing circuit element, IEEE Trans. Circuit Theory **18**, 507 (1971).

[5] M. D. Ventra, Y. V. Pershin, and L. O. Chua, Circuit elements with memory: Memristors, memcapacitors, and meminductors, Proc. IEEE **97**, 1717 (2009).

[6] Y. V. Pershin and M. D. Ventra, Memory effects in complex materials and nanoscale systems, Adv. Phys. **60**, 145 (2011).

[7] Z. B. Yan and J. M. Liu, Coexistence of high performance resistance and capacitance memory based on multilayered metal-oxide structures, Sci. Rep. **3**, 2482 (2013).

[8] H. Nieminen, V. Ermolov, K. Nybergh, S. Silanto, and T. Ryhänen, Microelectromechanical capacitors for RF applications, J. Micromech. Microeng. **12**, 177 (2002).

[9] I. Salaoru, Q. Li, A. Khiat, and T. Prodromakis, Coexistence of memory resistance and memory capacitance in TiO2 solid-state devices, Nanoscale Res. Lett. **9**, 552 (2014).

[10] Y. V. Pershin and M. D. Ventra, Memristive circuits simulate memcapacitors and meminductors, Electron. Lett. **46**, 517 (2010).

[11] J. Martinez-Rincon, M. Di Ventra, and Y. V. Pershin, Solid-state memcapacitive system with negative and diverging capacitance, Phys. Rev. B. **81**, 195430 (2010).

[12] Electrically Variable or Programmable Nonvolatile Capacitors, https://www.techbriefs.com/component/content/article/tb/techbriefs/electronics-and-computers/5773.

[13] J. F. Scott, *Ferroelectric Memories* (Springer, Berlin, New York, 2000).

[14] H. Ishiwara, M. Okuyama, and Y. Arimoto, Ferroelectric Random Access Memories: Fundamentals and Applications, Topics in Applied Physics Vol. 93 (Springer, Berlin, New York, 2004).

[15] P. Hou, J. Wang, X. Zhong, and Y. Wu, A ferroelectric memristor based on the migration of oxygen vacancies, RSC Adv. **6**, 54113 (2016).

[16] V. Garcia and M. Bibes, Ferroelectric tunnel junctions for information storage and processing, Nat. Commun. **5**, 4289 (2014).

[17] Z. Wen, C. Li, D. Wu, A. Li, and N. Ming, Ferroelectric-field-effect-enhanced electroresistance inmetal/ferroelectric/semiconductor tunnel junctions, Nat. Mater. **12**, 617 (2013).

[18] S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, S. Xavier, J. Tomas, L. Bellaiche, M. Bibes, A. Barthélémy, S. Saïghi, and V. Garcia, Learning through ferroelectric domain dynamics in solid-state synapses, Nat. Commun. **8**, 14736 (2017).

[19] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthélémy, and J. Grollier, A ferroelectric memristor, Nat. Mater. **11**, 860 (2012).

[20] Y. Nishitani, Y. Kaneko, and M. Ueda, in 72nd Device Research Conference (IEEE, Santa Barbara, CA, USA, 2014), pp. 297–298.

[21] S. Horie, K. Noda, H. Yamada, K. Matsushige, K. Ishida, and S. Kuwajima, Flexible programmable logic gate using organic ferroelectric multilayer, Appl. Phys. Lett. **91**, 193506 (2007).

[22] W. Y. Kim, H.-D. Kim, T.-T. Kim, H.-S. Park, K. Lee, H. J. Choi, S. H. Lee, J. Son, N. Park, and B. Min, Graphene-ferroelectric meta devices for nonvolatile memory and reconfigurable logic-gate operations, Nat. Commun. **7**, 10429 (2016).

[23] M. Di Ventra and Y. V. Pershin, The parallel approach, Nat. Phys. **9**, 200 (2013).

[24] A.-G. Boni, L. Filip, C. Chirila, I. Pasuk, R. Negrea, I. Pintilie, and L. Pintilie, Multiple polarization states in symmetric ferroelectric heterostructures for multi-bit non-volatile memories, Nanoscale **9**, 19271 (2017).

[25] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.12.024053 for descriptions on the materials and methods, electric and PFM measurements.

[26] C. Lichtensteiger, S. Fernandez-Pena, C. Weymann, P. Zubko, and J.-M. Triscone, Tuning of the depolarization field and nanodomain structure in ferroelectric thin films, Nano Lett. **14**, 4205 (2014).

[27] G. Liu, J. Chen, C. Lichtensteiger, J.-M. Triscone, P. Aguado-Puente, J. Junquera, and N. Valanoor, Positive effect of an internal depolarization field in ultrathin epitaxial ferroelectric films, Adv. Electron. Mater. **2**, 1500288 (2016).

[28] A. Ghosh, G. Koster, and G. Rijnders, Multistability in bistable ferroelectric materials toward adaptive applications, Adv. Funct. Mater. **26**, 5748 (2016).

[29] D. Zhao, I. Katsouras, K. Asadi, W. A. Groen, P. W. M. Blom, and D. M. de Leeuw, Retention of intermediate polarization states in ferroelectric materials enabling memories for multi-bit data storage, Appl. Phys. Lett. **108**, 232907 (2016).

[30] S. Ambrogio, P. Narayanan, H. Tsai, R. M. Shelby, I. Boybat, C. di Nolfo, S. Sidler, M. Giordano, M. Bodini, N. C. P. Farinha, B. Killeen, C. Cheng, Y. Jaoudi, and G. W. Burr, Equivalent-accuracy accelerated neural-network training using analogue memory, Nature **558**, 60 (2018).