Determining Interface Dielectric Losses in Superconducting Coplanar-Waveguide Resonators

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Superconducting quantum-computing architectures comprise resonators and qubits that experience energy loss due to two-level systems (TLSs) in bulk and interfacial dielectrics. An understanding of these losses is critical to improving performance in superconducting circuits. In this work, we present a method for quantifying the TLS losses of different bulk and interfacial dielectrics present in superconducting coplanar-waveguide (CPW) resonators. By combining statistical characterization of sets of specifically designed CPW resonators on isotropically etched silicon substrates with detailed electromagnetic modeling, we determine the separate loss contributions from individual material interfaces and bulk dielectrics. This technique for analyzing interfacial TLS losses can be used to guide targeted improvements to qubits, resonators, and their superconducting fabrication processes.

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I. INTRODUCTION

Two-level systems (TLSs) have been identified as critical contributors limiting performance in superconducting qubits and resonators [1–4]. While the microscopic origin of many TLSs are unknown, it is well established that ensembles of TLSs contribute to energy loss in superconducting devices through their interaction with the electric fields present in the bulk-dielectric materials and interfaces. Efforts to mitigate these losses have employed techniques from materials science, fabrication-process engineering, and microwave-device design. Materials improvements have focused on lowering TLS defect densities in bulk materials [5] or removing TLS-containing dielectrics [6]. Fabrication-process advancements have included steps aimed at reducing TLS loss through substrate preparation [7,8] and chemical-residue removal [9]. Design changes to qubits and resonators have reduced or shifted the electromagnetic (EM) fields interacting with surrounding material interfaces with the goal of minimizing TLS losses [10–17]. Collectively, these advances have led to qubit T_1 times exceeding 50 μs [18–20] and planar superconducting coplanar-waveguide (CPW) resonator internal quality factors (Q_i) in excess of 2 million at single-photon energy levels [16].

Further progress in reducing TLS losses has been hindered by an inability to isolate the contributions from separate sources of TLS loss. Several previous efforts to quantify interface losses have attempted to shift and reduce surface participation by using anisotropic substrate trenching. While this has reduced overall TLS loss and thereby improved T_1 and Q_i [8,15,16,21], anisotropic trenching reduces multiple sources of TLS loss by a similar amount, such that their relative contributions to total resonator loss are largely unknown. In contrast, EM simulations have shown that the losses associated with certain TLS-containing regions could be separately accentuated or suppressed through the use of isotropic etching [13]. Nevertheless, previous works have only studied changes in aggregate TLS loss or put bounds on individual interface losses and it has not been possible to distinguish and quantify loss contributions from individual dielectrics and material interfaces. Other efforts have succeeded in characterizing the loss contributions from bulk-deposited dielectrics [2,22] and superconducting metals [23], but these devices differ significantly from the modern planar circuits that are of interest for superconducting quantum-computing circuit architectures. In general, no method has yet been identified that can accurately quantify the individual contributions to aggregate dielectric losses in superconducting quantum circuits.

In this work, we use statistical characterization of sets of four different CPW-resonator designs with isotropically

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etched substrates, combined with detailed EM modeling, to determine the individual contributions to aggregate TLS losses of multiple-material-interface dielectrics and the bulk-silicon substrate. We then perform additional characterization of a series of devices with widely varying losses and EM participation ratios in order to verify a participation-ratio-based loss model. Additionally, we apply this technique to assess the increased losses that result from oxygen-plasma ashing the device metal surface and perform analyses to estimate the measurement resources required to isolate individual interface losses within a certain tolerance. These results present the simultaneous extraction of multiple separate-interface and bulk-dielectric contributions to aggregate device loss. Ultimately, this technique can provide critical insight into the origins of loss sources in modern superconducting quantum circuits.

II. RESULTS

A. Dielectric-loss model

TLS-related losses in superconducting CPW resonators can be analyzed by applying an EM-participation-ratio model similar to those used in Refs. [12,14–16,24]. In this model, the losses associated with TLSs, Q_{TLS}^{-1}, in a given device are a linear combination of the product of the loss tangents ($\tan\delta_i$) associated with each dielectric region i and their associated participation ratio p_i, the fraction of the total electric field energy stored in that region. Each interface contains an unknown combination of dielectrics and fabrication residues and, in our analysis, we assign a unique $\tan\delta_i$ to each interface that is exposed to a distinct fabrication process. We represent our device interfaces using four dielectric regions, as shown in the cross section in Fig. 1: metal-to-substrate (MS, red), substrate-vacuum or substrate-air interface (SA, blue), metal-vacuum or metal-air interface (MA, purple), and bulk silicon (Si, green). These regions are generally expected to have distinct dielectric values, thicknesses, and loss tangents. In this work, we alternatively describe device-region losses using scaled participation ratios P_i and "loss factors" x_i, which are normalized by the dielectric constant and thickness of the defect regions, as detailed in Ref. [16] or the Supplemental Material [25], and represented as follows:

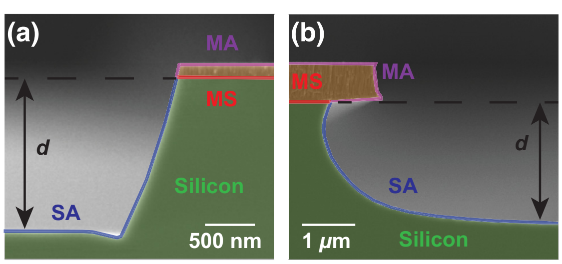


FIG. 1. Cross-section scanning-electron-microscope (SEM) images of (a) an anisotropically etched TiN resonator and (b) an isotropically etched TiN resonator. The dielectric regions are false colored: the metal-to-substrate interface (MS, red), the substrate-vacuum or substrate-air interface (SA, blue), the metal-vacuum or metal-air interface (MA, purple), and the bulk-silicon substrate (Si, green). The trench depth is d.

$$\frac{1}{Q_{\mathrm{TLS}}} = \sum_i p_i \tan\delta_i = \sum_i P_i x_i. \tag{1}$$

The x_i are of the form

$$x_{i,\parallel} = \frac{(t_i/t_{\mathrm{nom},i})}{(\epsilon_{\mathrm{nom},i}/\epsilon_i)} \tan\delta_i \tag{2}$$

or

$$x_{i,\perp} = \frac{(t_i/t_{\mathrm{nom},i})}{(\epsilon_i/\epsilon_{\mathrm{nom},i})} \tan\delta_i, \tag{3}$$

for the electric field components parallel and perpendicular to the dielectric interfaces, respectively. t_i and ϵ_i represent the true interface thicknesses and dielectric constants, while $t_{\mathrm{nom},i}$ and $\epsilon_{\mathrm{nom},i}$ are the values used in the COMSOL participation-ratio simulations. These "scaled" loss tangents can be written as coefficients of the participation-vector components, because the surface-field approximation [24] holds for the thin layers present on superconducting device interfaces. The loss factors are equal to the material loss tangent when the true layer thickness and dielectric constant match the simulated values. Regardless, for the purpose of isolating the overall loss contributions from distinct sources, it is the product $P_i x_i$ that is of interest; the details of the layer thickness and dielectric constant are only relevant for determining the loss tangent of the dielectric layer.

We can generate a matrix representation of Eq. (1) for multiple distinct device geometries sharing a common set of interface properties. For this case, a column vector of device inverse Q_{TLS} values is determined by a participation matrix $\boldsymbol{P}$ consisting of rows of device-participation ratios multiplied by a loss-factor column vector $\vec{x}$. The device Q_{TLS} values are derived from measurement, while the participation ratios of the dielectric regions in our devices are determined from two-dimensional electrostatic simulations using COMSOL [26]. With these values, we extract the loss factors in Eq. (1) using a linear least-squares fit constrained such that each $x_i > 0$.

We have previously used the EM participation model [Eq. (1)] to analyze aggregate TLS losses in CPW resonators with anisotropically etched silicon substrates [16], such as the one shown in Fig. 1(a). Anisotropic trenching leads to lower overall surface participation, but the participation ratios of each of the interface dielectric regions are reduced by a similar amount as the trench depth d

is increased. This nearly proportional scaling of the participation ratios results in an ill-conditioned participation matrix used to solve Eq. (1). As a result, the generated loss-factor solutions are highly sensitive to variations in the input Q_{TLS}, leading to large uncertainty when estimating the losses associated with each individual dielectric region. Accordingly, the precise assignment of loss-factor values to individual interfaces is practically infeasible. While it is technically possible to reduce the solution uncertainty by reducing the error in the estimates of Q_{TLS}, this improves only as $\sqrt{N}$, where N is the number of devices measured, resulting in prohibitively large measurement-resource requirements. In this work, we instead focus on creating a better-conditioned participation matrix through the use of isotropically etched CPW resonators.

An example cross section of an isotropically etched TiN resonator is shown in Fig. 1(b). The false-colored scanning-electron-microscope (SEM) image also depicts the four dielectric regions that we analyze: MS, SA, MA, and Si. The simulated participation-ratio vectors associated with isotropically etched resonators indicate that these vectors scale with the device geometry (center trace width w, gap to ground g, and etch depth d) less proportionally than anisotropically trenched devices of comparable size [13,15,24] (for details, see the Supplemental Material [25]). This nonproportional scaling has a significant impact on the metrics that quantify the singularity of the participation matrix; in particular, the condition number $\kappa(\boldsymbol{P})$. The condition number $\kappa(\boldsymbol{P})$ of the participation matrix $\boldsymbol{P}$ in Eq. (1) relates the uncertainty in the mean Q^{-1} values to the uncertainty in the extracted loss factors. For the case of four geometries and four loss factors, the ideal participation matrix is a 4×4 identity matrix with a condition number equal to 1. In this case, the uncertainty in the extracted loss factors is equal to the uncertainty of the mean measured Q^{-1} values in Eq. (1). In general, participation matrices with larger condition numbers generate solutions with greater uncertainty than would be determined solely by measurement statistical variance [27].

For the case of trenched CPW resonators, we determine that isotropic trenching greatly reduces our participation-matrix condition number $\kappa(\boldsymbol{P})$ as compared to the case of anisotropically trenched devices. We perform a constrained search over the range of geometries accessible to our isotropic-etch fabrication process (trench depth $d \leq 11\ \mu$m) in order to determine a set of four structures that minimize $\kappa(\boldsymbol{P})$. The cross sections of these four CPWs are shown in Figs. 2(a)–2(d). Figure 2(a) shows the $(w, g, d) = (6\ \mu\mathrm{m}, 3\ \mu\mathrm{m}, 0.28\ \mu\mathrm{m})$ CPW cross section, designed to be "MS heavy" because it maximizes the MS-interface-region participation relative to the other regions. The shallow trenching in this geometry forms an essentially planar structure comparable to untrenched planar qubits [28] and CPW resonators [7]. The CPW cross sections shown in Fig. 2(b) $[(w, g, d) = (6\ \mu\mathrm{m}, 1\ \mu\mathrm{m}, 4.5\ \mu\mathrm{m})]$ and Fig. 2(d) $[(w, g, d) = (28\ \mu\mathrm{m}, 14\ \mu\mathrm{m}, 10.9\ \mu\mathrm{m})]$ rely on deep trenching to achieve "SA-heavy" and "Si-heavy" structures, respectively, by varying the center trace dimension and gap-to-ground spacing. The "MA-heavy" cross section shown in Fig. 2(c) $[(w, g, d) = (8\ \mu\mathrm{m}, 1\ \mu\mathrm{m}, 4.5\ \mu\mathrm{m})]$ differs compared to the others shown in Fig. 2 in that its signal line is completely undercut for a significant fraction (approximately 85%) of the total resonator length and the suspended structure is supported with periodically placed Si posts. These suspended CPWs shift a greater fraction of the total participation to the MA interface than is possible with anisotropic or isotropic etching alone (for details, see the Supplemental Material [25]). The condition number $\kappa(\boldsymbol{P})$ of the participation matrix generated by these four isotropically etched CPW-resonator geometries is reduced to $\kappa(\boldsymbol{P}) = 2001$ from $\kappa(\boldsymbol{P}) = 110,201$ for an optimal set of anisotropically trenched devices, an improvement of a factor of approximately 55.

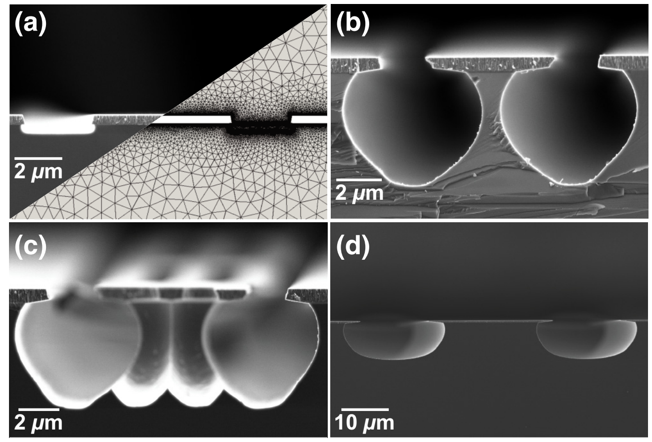


FIG. 2. Cross-section SEM images of isotropically etched TiN CPW resonators. (a) A MS-heavy resonator $(w, g, d) = (6\ \mu\mathrm{m}, 3\ \mu\mathrm{m}, 0.28\ \mu\mathrm{m})$ and the corresponding COMSOL simulation mesh. (b) A SA-heavy resonator, $(w, g, d) = (6\ \mu\mathrm{m}, 1\ \mu\mathrm{m}, 4.5\ \mu\mathrm{m})$. (c) A MA-heavy partially suspended resonator, $(w, g, d) = (8\ \mu\mathrm{m}, 1\ \mu\mathrm{m}, 4.5\ \mu\mathrm{m})$. (d) A Si-heavy resonator, $(w, g, d) = (28\ \mu\mathrm{m}, 14\ \mu\mathrm{m}, 10.9\ \mu\mathrm{m})$.

B. Experimental methods

The isotropically etched CPW devices shown in Figs. 1 and 2 are fabricated using a subtractive-etch process on high-resistivity ($\geq 3500\ \Omega$ cm) 200-mm (001) silicon substrates, similar to the process described in Ref. [16]. In this work, however, we use a metal thickness of 450 nm or 750 nm, and adjust the total chlorine-based etch time such that, regardless of the TiN thickness, the substrate is minimally etched. Then, instead of immediately stripping the photoresist, we rinse the wafer in deionized water and subject it to a second fluorine-based plasma etch to isotropically etch the underlying silicon substrate. The total isotropic etch time is adjusted to control the trench depth d and the amount of undercutting. The remaining photoresist is then stripped using a combination of ashing solvent resist strips. The final solvent resist strip etches the metal surface very slightly (a few nanometers), justifying the assumption that the entire MA interface exhibits the same surface properties after processing. Aside from varying the etch time and using two metal thicknesses, we use a nominally identical fabrication process for all devices. After fabrication, each device geometry is characterized using cross-sectional SEM to refine the simulation geometry input into COMSOL. This improves the physical accuracy of the participation matrix $\boldsymbol{P}$ in Eq. (1). We do not observe any discermable variability in the etch cross section between several devices taken from different positions across the wafer. The cross section in Fig. 2(a) also shows the COMSOL mesh used for the CPW in the right half of the figure.

In order to account for device-to-device variation and generate the statistics necessary to estimate the uncertainty in the extracted interface losses, we characterize many nominally identical copies of each resonator. This is achieved by frequency multiplexing five resonators in the 5–6 GHz range with the same width, gap, and trench depth on 5 mm $\times$ 5 mm chips and measuring many such identical chips within individual microwave-connectorized, gold-plated copper enclosures in a single dilution refrigerator cool-down. The dilution refrigerator contains two independent measurement chains consisting of microwave attenuators, filters, 1 $\times$ 6 coaxial switches, isolators, directional couplers, and amplifiers (one Josephson traveling-wave parametric amplifier [29] and one high-electron-mobility-transistor amplifier). A vector-network analyzer is used to measure each resonator's microwave-transmission spectrum over a range of internal circulating photon numbers n_p at 25 mK in a magnetically shielded light-tight environment. These transmission spectra are then fitted to determine the intrinsic quality factor of the resonator in the low-power limit ($n_p \sim 1$), where Q_i is mostly dominated by TLS-related losses, and the high-power limit ($n_p \sim 10^6$), where Q_i is dominated by power-independent losses such as vortices [30], quasiparticles [31,32], or radiation and/or package losses [4]. In order to reduce the systematic and variable losses contributed by these power-independent mechanisms and thereby determine the aggregate losses that are solely due to interface and substrate TLSs, we subtract the high-power losses from the low-power losses to determine a TLS-limited quality factor Q_{TLS}. Additional details on the measurement apparatus, techniques, and data analysis can be found in Ref. [16].

C. Dielectric-loss extraction and verification

We combine the measured Q_{TLS} values with the simulated participation matrix $\boldsymbol{P}$ to extract the loss-factor vectors $\vec{x}$ in Eq. (1), using a linear least-squares fit. To estimate the uncertainty in the resulting solutions, we use Monte Carlo error analysis. Each input trial case for the Monte Carlo analysis is selected from the estimated distribution of Q_{TLS} that we determine by measuring approximately 30 CPW resonators for each of the four geometries. The mean and standard deviation of these input distributions are determined from the mean and standard error of the measured Q_{TLS} values. A range of loss-factor vectors $\vec{x}$ is then extracted using the 4×4 participation matrix $\boldsymbol{P}$ and the matrix representation in Eq. (1) from $N = 10\,000$ repetitions of the Monte Carlo simulation.

For quantifying and predicting the losses that set Q_{TLS}, the loss factors in Eq. (1) are sufficient. However, it is often desirable to estimate the loss tangents of the dielectric regions using reasonable assumptions for the interface dielectric thickness t and permittivity ϵ. Using values similar to those typically assumed in the literature (e.g., Refs. [9], [15], [16], and [24]) for the thicknesses and dielectric values of the TLS defect regions, $t_{\mathrm{MS}} = 2$ nm, $t_{\mathrm{SA}} = 2$ nm, $t_{\mathrm{MA}} = 2$ nm, $\epsilon_{\mathrm{MS}} = 11.4\epsilon_0$, $\epsilon_{\mathrm{SA}} = 4\epsilon_0$, and $\epsilon_{\mathrm{MA}} = 10\epsilon_0$, we can ascribe loss tangents to the individual defect regions. The output histograms resulting from the Monte Carlo estimation of these loss tangents are shown in Fig. 3 and the mean values and associated 95% confidence intervals are as follows:

$$[\tan\delta] = \begin{bmatrix} \tan\delta_{\mathrm{MS}} \\ \tan\delta_{\mathrm{SA}} \\ \tan\delta_{\mathrm{MA}} \\ \tan\delta_{\mathrm{Si}} \end{bmatrix} = \begin{bmatrix} 4.8 \times 10^{-4} \pm\ 2 \times 10^{-4} \\ 1.7 \times 10^{-3} \pm\ 4 \times 10^{-4} \\ 3.3 \times 10^{-3} \pm\ 4 \times 10^{-4} \\ 2.6 \times 10^{-7} \pm\ 4 \times 10^{-8} \end{bmatrix}. \quad (4)$$

The Gaussian output distributions for each loss tangent indicate that this combination of values represents a stable unique estimation of the losses for each dielectric region in our devices.

In order to verify this participation-based loss model, we use the loss factors presented in Eq. (2) to predict the aggregate losses for nine additional distinct resonator geometries with interface participation and total Q_{TLS} that differ significantly from the device set used for loss-factor extraction. These additional devices have center trace widths w ranging from 6 μm to 28 μm, gaps to ground g ranging from 1 μm to 14 μm, and trench depths d ranging from 280 nm to 10.9 μm. The resulting Q_{TLS} ranges from approximately 1×10^6 to approximately 2.7×10^6 (for dimensions and Q_{TLS}, see the Supplemental Material [25]). A comparison between the predicted and measured Q_{TLS} for all 13 resonator geometries is shown in Fig. 4(a). The green dashed line in Fig. 4(a) represents the ideal case where the measured Q_{TLS} is equal to the predicted Q_{TLS}. The red error bars represent the 95% confidence interval for the mean measured Q_{TLS}, while the blue error bars show the 95% confidence interval of the predicted Q_{TLS} as determined by Monte Carlo simulations. The bar graph in Fig. 4(b) shows

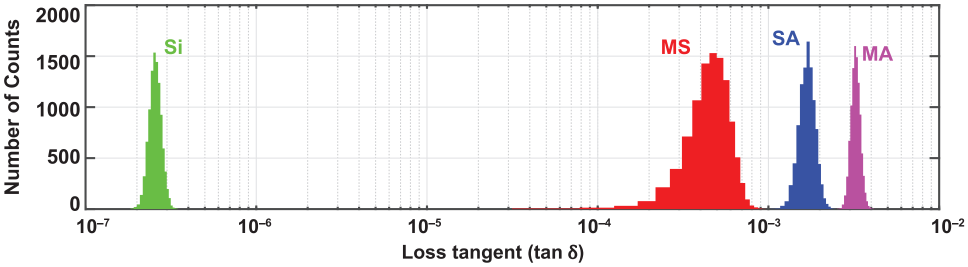


FIG. 3. The extracted loss tangents of the metal-to-substrate (MS), substrate-vacuum or substrate-air interface (SA), metal-vacuum or metal-air interface (MA), and silicon substrate (Si) dielectric regions.

the absolute contributions to losses $Q_{\mathrm{TLS}}^{-1} = \sum Q_k^{-1} = \sum P_k x_k, k \in \{\mathrm{MS, SA, MA, Si}\}$, in each of the 13 CPW resonators, the quality factors of which are shown in Fig. 4(a). This confirms that the four CPW-resonator test cases used to extract the individual region losses each emphasize a different single dielectric-region while minimizing the others; the devices labeled 1–4 (the extraction set) in Fig. 4(b) and shown in Figs. 2(a)–2(d), respectively, have the largest contribution to their aggregate losses from the MS, SA, MA, and Si dielectric layers, respectively, relative to the other devices.

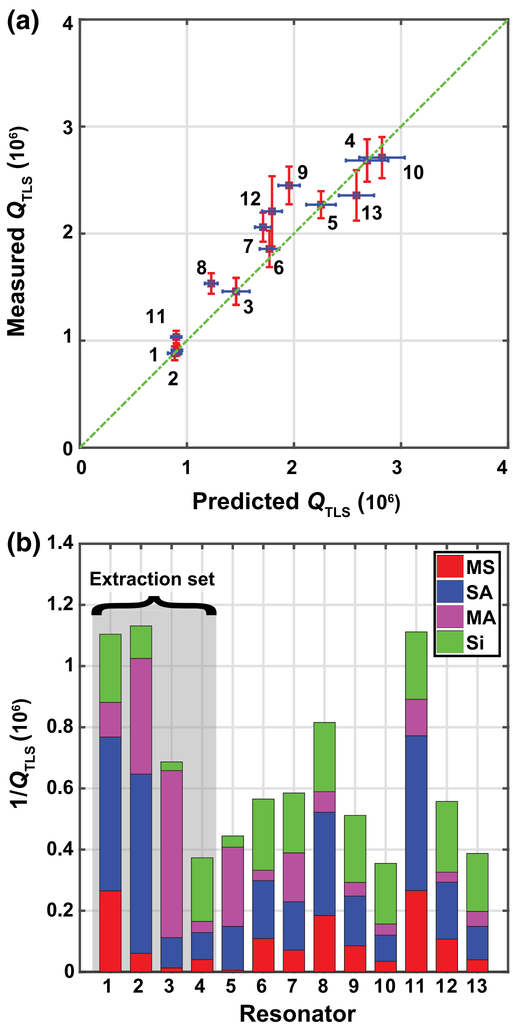


FIG. 4. (a) Measured vs predicted Q_{TLS} and (b) the corresponding loss contributions of 13 measured resonators.

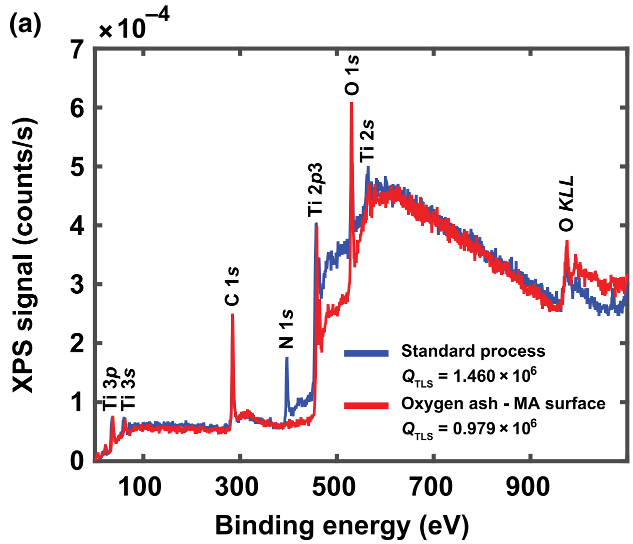
To demonstrate the effectiveness of using this technique to resolve changes in interface losses resulting from different fabrication conditions, we repeat this sample fabrication, measurement, and analysis process on a set of devices with a deliberately altered MA interface. These devices are made using the same fabrication process as the previous devices, except that the starting film is subjected to an oxygen-plasma ash prior to photolithographic patterning. As compared to the previous process, the x-ray photoelectron spectrosopy (XPS) spectrum of this film, shown in Fig. 5(a), shows that no N 1s peak associated with surface nitrogen and a corresponding increase in the intensity of the oxygen-related O 1*s* and O *KLL* peaks. As XPS is primarily sensitive to material surfaces, this data is consistent with a conversion of the titanium nitride surface to titanium oxide. Since metal oxides are a known source of TLSs [3], we see a corresponding decrease in the Q_{TLS} of this set of devices, with the MA-heavy test case decreasing from $Q_{\mathrm{TLS}} = 1.46 \times 10^6$ to $Q_{\mathrm{TLS}} = 9.79 \times 10^5$.

The loss-factor exaction results comparing the two processes are shown in Fig. 5(b). The devices subjected to the oxygen ash demonstrate a statistically significant 60% increase in the MA loss factor over the standard process. The loss factors of the other dielectric regions, however, are unchanged within the margin of their associated error bars. When combined with the simulated device participations, we can determine the magnitude of the increase in MA interface losses that contribute to the aggregate device loss Q_{TLS}^{-1} for the MA-heavy test case, as depicted in Fig. 5(c). This result is consistent with the expected decrease in device Q_{TLS} resulting from the presence of additional TLSs in the MA surface oxide and demonstrates the utility of this technique as a general tool for characterizing the dielectric losses introduced by superconducting-qubit fabrication processes.

III. DISCUSSION AND CONCLUSION

The unique estimation of the interface loss tangents shown in Fig. 3 is enabled by three aspects of this analysis. We design a set of isotropically etched CPWs to form a participation matrix $\boldsymbol{P}$ that is significantly better conditioned than is possible with planar designs or anisotropic

(a)



(b)

Process	x_{MA}(x10^{-4})	x_{SA}(x10^{-4})	x_{MS}(x10^{-4})	x_{Si}(x10^{-4})
Standard	6.5 ± 0.8	3.4 ± 0.7	0.97 ± 0.5	.0026 ± .0004
Oxygen-Ash MA surface	10.6 ± 0.3	3.0 ± 1	1.3 ± 0.7	.0025 ± .0007

(c)

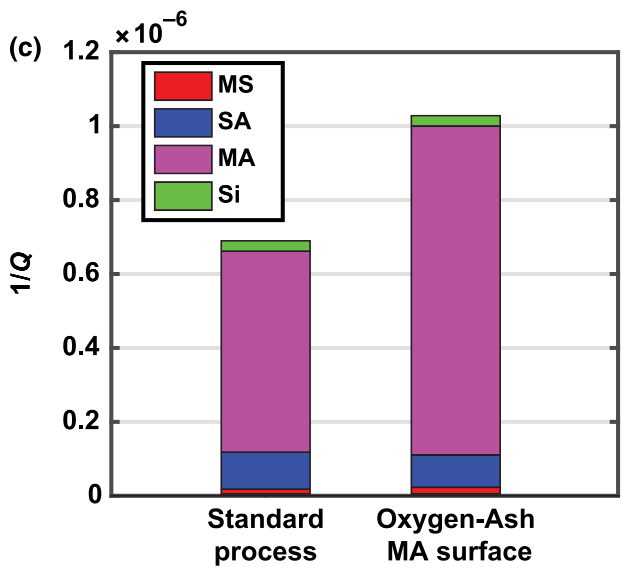


FIG. 5. (a) An XPS spectrum comparing the MA interface of the standard process with the same process subjected to an oxygen-plasma ash prior to patterning. (b) A comparison of the loss factors extracted from each set of devices. (c) The loss contributions from each individual interface for the MA-heavy devices.

trenching. Second, we measure many nominally identical copies of the same device to compensate for device-to device variation. This allows us to generate an estimate of the mean Q_{TLS} associated with each geometry and to determine the Q_{TLS} statistics required for estimation of the loss-factor uncertainty using Monte Carlo techniques. Finally, imaging of each device geometry greatly refines the accuracy of the electrostatic simulations used to determine each geometry's interface participation.

The good agreement between the measured and predicted Q_{TLS} values for devices with a wide range of total Q_{TLS} and participation ratios shown in Fig. 4(a) demonstrates the accuracy and utility of the loss-factor analysis. In addition to this predictive power, this technique can be used as a diagnostic tool for assessing the relative contributions to total losses from different interfaces for a given geometry, as shown in Fig. 4(b). Resonator 12, for example, with $(w, g, d) = (22\,\mu\mathrm{m}, 11\,\mu\mathrm{m}, 0.41\,\mu\mathrm{m})$, has a cross section that is the most similar to many untrenched resonator and qubit capacitors used in superconducting qubit circuits [28]. For this case, Fig. 4(b) demonstrates that although the SA and silicon dielectric regions have the largest contributions to the aggregate losses, all four regions have non-negligible contributions.

In order to determine the feasibility of using this technique as a general tool for superconducting-fabrication-process qualification and development, we perform simulated experiments to estimate how many devices must be measured in order to obtain a unique set of loss tangents. These simulations project the stability of the output solutions generated from inputs consisting of a variable number of measured devices with the loss tangents shown in Eq. (2) and Q_{TLS} standard deviations similar to what we observe in experiment. Furthermore, to demonstrate the utility of the isotropically etched geometry, we compare the isotropic-resonator designs labeled 1–4 in this work with the four anisotropic cases that produce the lowest-condition-number participation matrix from the device set measured in Ref. [16]. The results, shown in the Supplemental Material [25], demonstrate that while the anisotropic device simulations converge very slowly and tend to generate unstable solutions with no lower bound, the isotropically etched devices produce a bounded solution centered on the correct values within the total of approximately 120 devices that we have measured.

In summary, we combine statistical characterization of sets of specially designed isotropically etched CPW resonators with detailed EM modeling and Monte Carlo error analysis in order to uniquely determine the individual interface losses in superconducting microwave resonators. Using this technique we determined TLS-related losses of the silicon substrate and individual interface dielectrics for a superconducting quantum circuit. The determination of these values enables the construction of a predictive participation-based model for aggregate device losses that we verified using a series of superconducting CPW resonators with a range of participation ratios and total Q_{TLS}. This technique for distinguishing the relative contributions from individual material interface losses could be utilized to drive improvements in qubits and resonator design. Alternatively, the knowledge generated using this process can provide interface-specific feedback for improving fabrication processes or qualifying fabrication-process changes. In general, this technique stands to significantly enhance our ability to compare different materials and fabrication process for improving the performance of superconducting quantum circuits.

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