Nanoscale Tunnel Field-Effect Transistor Based on a Complex-Oxide Lateral Heterostructure

A. Müller,[1] C. Şahin,[2,3] M.Z. Minhas,[1] B. Fuhrmann,[4] M.E. Flatté,[2,3,5] and G. Schmidt[1,4,*]

[1] *Institut für Physik, Martin Luther University Halle-Wittenberg, 06099 Halle (Saale), Germany*

[2] *Optical Science and Technology Center, and Department of Physics and Astronomy, University of Iowa, Iowa City, Iowa 52242, USA*

[3] *Institute for Molecular Engineering, University of Chicago, Chicago, Illinois 60637, USA*

[4] *Interdisziplinäres Zentrum für Materialwissenschaften, Martin Luther University Halle-Wittenberg, 06099 Halle (Saale), Germany*

[5] *Department of Applied Physics, Eindhoven University of Technology, P.O. Box 513, 5600 MB, Eindhoven, The Netherlands*

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We demonstrate a tunnel field-effect transistor based on a lateral heterostructure patterned from an $LaAlO_3/SrTiO_3$ electron gas. Charge is injected by tunneling from the $LaAlO_3/SrTiO_3$ contacts and the current through a narrow channel of insulating $SrTiO_3$ is controlled via an electrostatic side gate. Drain-source I-V curves are measured at low and elevated temperatures. The transistor shows strong electric-field-dependent and temperature-dependent behavior, with a steep subthreshold slope as small as 10 mV/dec and a transconductance as high as approximately 22 μA/V. A fully consistent transport model for the drain-source tunneling reproduces the measured steep subthreshold slope.

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I. INTRODUCTION

Since the discovery of the electron gas between the two complex-oxide band insulators $LaAlO_3$ (LAO) and $SrTiO_3$ (STO) [1], a number of devices have been realized, including both classical field transistors [2,3] and quantum-transport devices such as the single-electron transistor [4]. Device concepts suggested for the two-dimensional electron gas (2DEG) in LAO/STO heterostructures usually use the conducting interface in a similar fashion to how a 2DEG is used in a III-V or group-IV semiconductor heterostructure. Control of the transport occurs by electric field control of the carrier concentration at the interface, as in a field-effect transistor [2,3], by side gates [5,6], or by gate control of the potential in a small LAO/STO island [4]. Less explored is charge transport in STO itself, when the material is doped, for example, with vacancies or impurities [7–9]. However, transport through insulating STO over submicron distances is also possible when a suitable band alignment is achieved by applying electric fields.

The LAO/STO system can enable new device structures because LAO/STO islands can be used as contacts for charge injection into STO with reliable performance and low threshold voltage. On the basis of such contacts we demonstrate a lateral heterostructure in which a narrow STO channel between two LAO/STO contacts conducts at bias voltages well below 100 mV, and we also demonstrate that the current can be controlled by equally small gate-source voltages applied between a side gate and the channel. The subthreshold slope under such conditions is very steep, indicating the importance of tunneling currents. Therefore, we present a steep-subthreshold-slope device that consists entirely of oxide materials and is fabricated in a single-step, industry-compatible etching process. We also demonstrate current manipulation of a wide conducting channel by a single side gate with low gate currents.

II. DEVICE DESCRIPTION

The device consists of an insulating STO channel that is laterally contacted by the 2DEG and a wedge-shaped side gate that is patterned into the 2DEG in the vicinity of the channel [Fig. 1(a)]. The channel between the source and the drain has length $L = 130 - 160$ nm and width $W = 4$ μm. The spacing between the tip of the side gate and the channel is 1 μm. For our measurements we use a standard lateral three-terminal geometry [Fig. 1(a)] consisting of two current leads (drain and source), biased by a dc-voltage source. Two additional contacts can be used as voltage probes for four-terminal measurements. The gate has only a single contact. The 2DEG arises from the deposition of

*georg.schmidt@physik.uni-halle.de

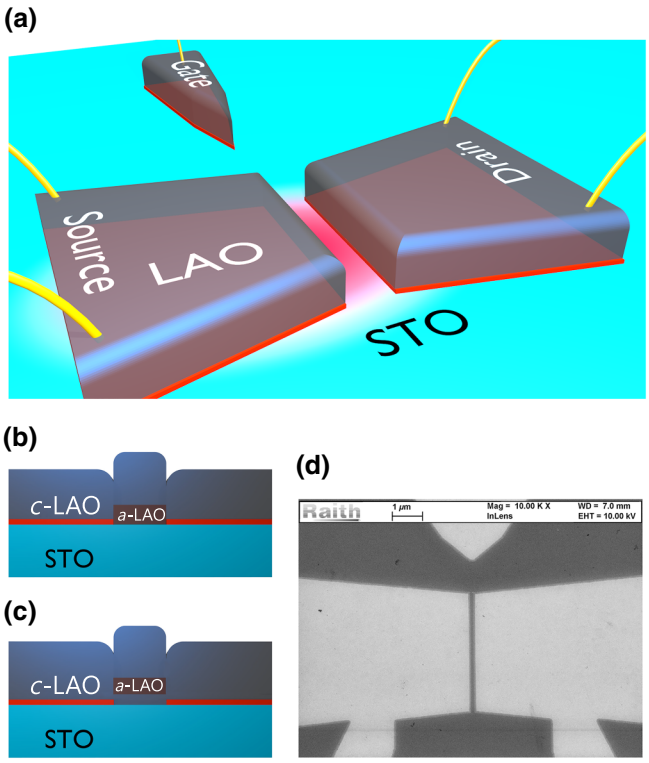

FIG. 1. (a) The sample after the structuring process. Two current pads bonded for four-probe measurements are separated electrically by a gap by removal of the LAO in that region. This creates a lateral heterostructure composed of the 2DEG underneath the LAO connected laterally by the STO channel. A gate-source voltage can be applied by a side gate. The 2DEG is directly contacted by aluminum wire bonds. Alternative patterning processes use *a*-LAO to avoid the formation of the 2DEG. The *a*-LAO is patterned by a lift-off process directly on the substrate (b) or on crystalline LAO with a subthreshold thickness of two unit cells (c) as described by Schneider *et al.* [11]. (d) A scanning-electron-microscope image of an etched structure.

six unit cells of crystalline LAO (*c*-LAO) onto the TiO_2-terminated STO surface [1]. The nonconducting areas are created either by our removing the *c*-LAO by reactive-ion etching (RIE) [Fig. 1(a)], as demonstrated by Minhas *et al.* [10], or by our locally preventing the growth of more than three unit cells of *c*-LAO [11]. The latter can be achieved by use of a patterned amorphous LAO (*a*-LAO) layer with [Fig. 1(c)] or without [Fig. 1(b)] prior deposition of a two-unit-cell subthreshold *c*-LAO layer. The second process is almost identical to the method described by Schneider *et al.* [11] and is also related to methods [5,6,12] where patterned amorphous materials different from LAO were used to prevent *c*-LAO growth. The 2DEG is electronically contacted with Al wire bonds by ultrasonic bonding directly through the top LAO layer. Figure 1(d) shows a scanning-electron-microscope image of a typical device fabricated by the RIE process.

III. RESULTS

Temperature-depended transport characteristics have been investigated in semiconducting, niobium-doped, or oxygen-deficient STO [7–9,13]. In slightly reduced STO single crystals [9] and reduced STO thin films [13] freeze-out of charge carriers was observed at low temperatures. In competition with the decrease in carrier concentration due to freeze-out, the carrier mobility increases as the temperature drops and peaks at an intermediate temperature (50 K for Ref. [9] and 100 K for Ref. [13]). Liu *et al.* [13] suggest a metal-insulator transition occurs at this temperature, with carrier trapping in an oxygen-vacancy-donor level at lower temperatures. However, they also found the carrier trapping to be partially suppressed by an electric-field-induced detrapping. In our measurements we also observe a temperature-dependent series resistance. This resistance, however, does not play a dominant role within the observed current regime for low temperatures, and therefore the metal-insulator transition and detrapping effects described above are not important for interpreting our measurements.

We determine first the drain-source I-V characteristics at 4.2 K of a RIE-etched sample with no gate connected (this structure is referred to as "structure 1" below). The results are shown in Fig. 2(a). At low bias voltages the current is below the detection limit of the current amplifier of approximately 100 fA. At a threshold bias voltage, V_{th}, the current starts to flow and we observe an increase in current of more than 7 orders of magnitude within a few tens of millivolts. This increase shows no hysteresis and is similar for positive and negative polarity (except for the current direction). The rise in current, however, is limited by an additional inherent series resistance, which in this experiment is on the order of a few kilo-ohms at 4.2 K, leading to a constant slope dI/dV at high currents. The qualitative behavior is the same for all working structures and all processes used, although the values for V_{th} and the slope differ from sample to sample and also slightly for each cool down of the same structure. V_{th} can also be shifted irreversibly to higher values by the application of a high voltage, which also results in a reduced dI/dV slope.

In Fig. 3(a) the I-V curves in the temperature range from 1.2 to 111.4 K from structure 1 are shown. The I-V curves are linear in a semilogarithmic plot and their slopes decrease with increasing temperature. When the curves are described by the simple expression $I(V) = \alpha \exp(\beta V)$, we find α increases and β decreases with rising temperature. This leads to crossing points between the curves. For $T \geq 31$ K, these crossing points are below our measurement limit since β decreases faster than $\ln \alpha$ increases. The apparent shift in V_{th} is a consequence of this behavior also because V_{th} is just the crossing point of the I-V curve with our current detection limit.

For a second structure (structure 2) with a shorter channel (approximately 130 nm) on the same sample

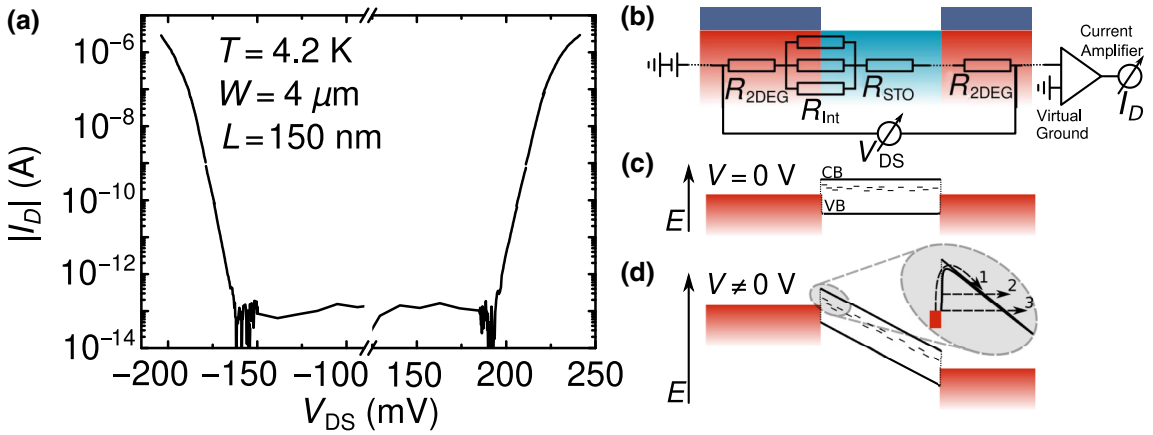

FIG. 2. (a) Typical I-V curve with a current increase of more than 7 orders of magnitude measured with different current-amplifier gains at 4.2 K. This sample is patterned by the RIE process and has a nominal width of 4 μm and a channel length of 160 nm. (b) Equivalent circuit showing the measurement geometry with the resistances of the 2DEG, the interface, and the channel in series. The parallel resistors at the interface represent different current-injection mechanisms 1,2, and 3 shown in (d). (c),(d) Band diagrams without and with applied bias. The in-gap states represent trap sites within STO. CB, conduction band; VB, valence band.

[Fig. 3(b)] the behavior is qualitatively similar but with some quantitative differences. In Figs. 3(c) and Fig. 3(d), the I-V curves are drawn as $\log I$ versus $\sqrt{V}$, as is helpful when the curves are dominated by Schottky or Poole-Frenkel emission [14–16] (see below). However, the overall resistance is smaller (which may appear as a smaller $V_{\rm th}$) and the intersections are at different currents and voltages within the measured range. In addition, for higher temperatures the I-V curves show an increasing slope at smaller voltages within the semilogarithmic plot. It is noteworthy that the linear extrapolations of the curves in Fig. 3(d) yield results very similar to the results in Fig. 3(c) and in some cases even parts of the I-V characteristics look almost geometrically identical [dashed squares in Figs. 3(a) and 3(b)] even at different temperatures. This suggests that both sets of curves reflect two different parts of the same universal I-V characteristics. Nevertheless for both structure 1 and structure 2, a slight asymmetry between positive and negative bias can be observed as the respective threshold voltages $\pm V_{\rm th}$ differ by up to 25 mV.

After connection of the side gate, I-V curves are recorded with a fixed gate-source voltage $V_{\rm GS}$ and variable drain-source voltage $V_{\rm DS}$ [Fig. 4(a)], as well as with a fixed drain-source voltage and a variable gate-source voltage [Fig. 4(b)], corresponding to transistor output and transfer characteristics, respectively. In Fig. 4(a) the I-V curves of structure 1 recorded at $T = 1.2$ K with fixed $V_{\rm GS} \in \{-50\,{\rm mV}, 0\,{\rm mV}, 50\,{\rm mV}\}$ are shown. The application of a gate-source voltage results simply in a shift of the I-V curves to higher (lower) absolute voltages for negative (positive) values of $V_{\rm GS}$. The slope of the semilogarithmic I-V curves, $d(\ln I)/dV_{\rm DS}$, remains unchanged.

A measurement with a $V_{\rm GS}$ sweep for different $V_{\rm DS}$ at $T = 1.2$ K is shown in Fig. 4(b). For currents $I \leq 10^{-8}$ A, an exponential dependence on $V_{\rm GS}$ is observed. For higher currents the slope starts to decrease, although the exponential behavior is evident only at lower temperatures. This fact, however, may also be attributed to the sharply reduced slope of the curves at higher temperatures, which makes the influence of a series resistance less prominent. The insert in Fig. 4(b) shows that the gate current is well below 200 fA during the whole measurement. The gating effect is strongly reduced with increasing temperature, as shown in Fig. 5. Figure 6 shows the reproducible operation of the device as an *on-off* switch. $V_{\rm GS}$ is switched between -100 mV and 100 mV repeatedly, each time switching $I_{\rm DS}$ from approximately 0.1 pA to approximately 0.17 μA, and back. The transconductance g_m of this measurement is $\Delta I_{\rm DS}/\Delta V_{\rm GS} \approx 0.85\,\mu$A/V but can be as high as 22 μA/V for higher $I_{\rm DS}$.

To theoretically describe the observed behavior one needs to consider the strong field and temperature dependence. The reduction of $d(\ln I)/dV$ with temperature indicates that the electric field effect scales with temperature. A higher current at low bias voltages for higher temperatures suggests a thermally activated energy expression of the form $\exp(-\Phi/k_BT)$. In Fig. 2(b) an equivalent circuit of the ungated structure is drawn. It describes the two areas of the 2DEG as metallic contacts connected by the insulating STO channel. This can be considered to be analogous to two back-to-back Schottky diodes with the two depletion regions merging into a single central one. For current to flow, the electrons need to overcome the potential barrier at the 2DEG-STO lateral interface, which occurs by different mechanisms that can be described as electrode-limited processes [17], which together determine an interface resistance as shown in Figs. 2(c) and 2(d). Each process can be described by a

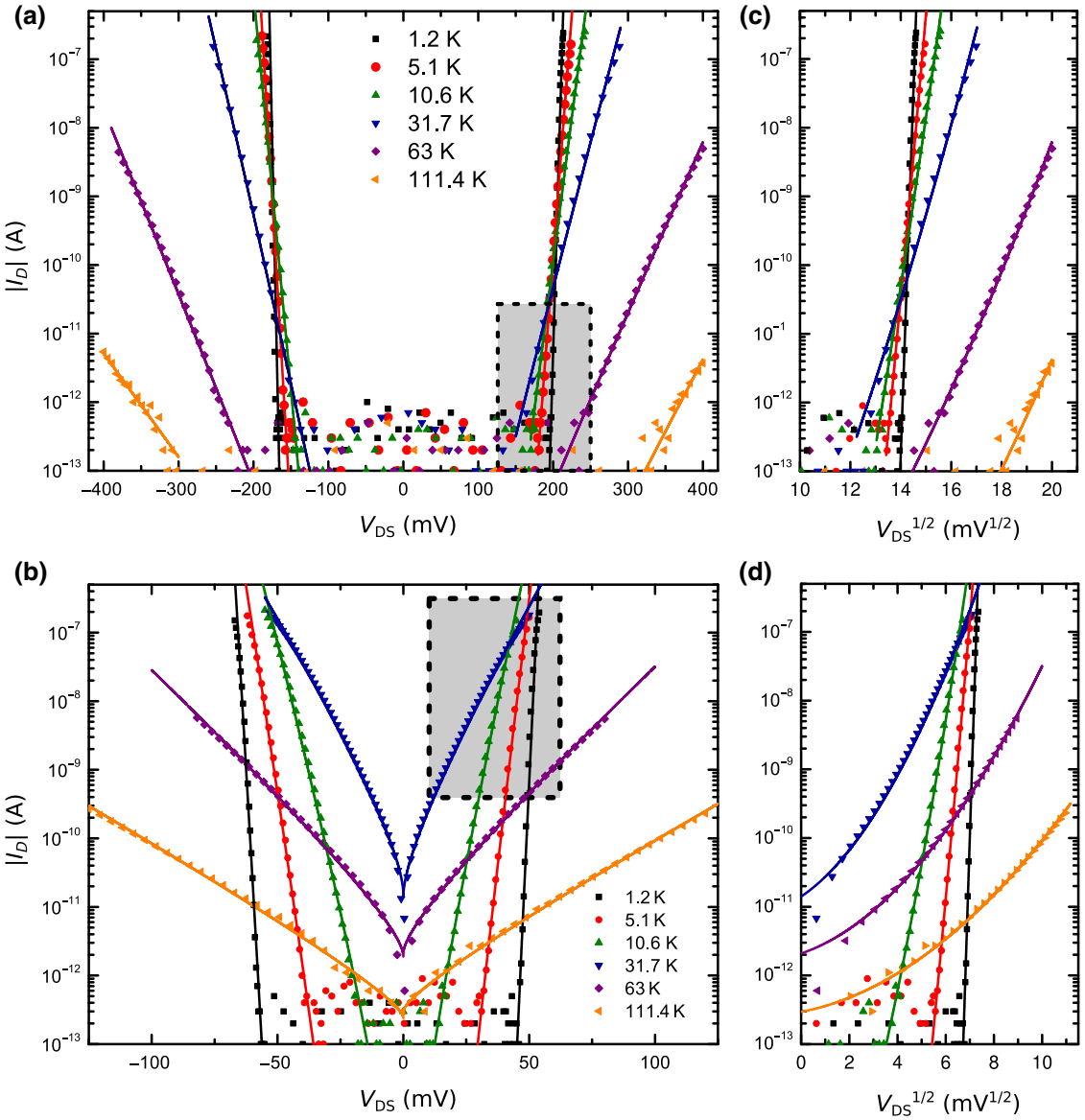

FIG. 3. (a) Temperature-dependent I-V characteristics for a device with a nominal channel length $L \approx 160$ nm. The symbols represent the measured data and the solid lines represent the calculated curves. The measurements shown are in the temperature range from 1.2 to 111.4 K. (b) I-V curves for a structure on the same sample with length $L \approx 130$ nm and otherwise the same dimensions. All measurements are taken in the same run for each temperature. The inserted dashed squares cover similarly sized current and voltage ranges for each structure. (c),(d) Current as a function of $\sqrt{V_{DS}}$.

resistor, and the rates of different processes add, which corresponds to multiple interface resistors added in parallel. Because the channel's length exceeds 100 nm, transport through the bulk of the STO, whether through the conduction band or via trap-related processes, should be treated separately.

For transport through the interface, the emission of carriers from the 2DEG into the STO's conduction band dominates the transport properties. For low temperatures and high electric fields, a triangular barrier is formed and charge carriers can tunnel directly into the insulator's conduction band as shown in process 3 in Fig. 2(d) through Fowler-Nordheim tunneling [18–20]. For higher temperatures and lower electric fields, thermally activated carriers tunnel through the thinner effective potential barrier at higher carrier energies [Fig. 2(d), process 2]. At even higher temperatures, thermionic, or Schottky, emission over the barrier occurs. The electric field added by the image-force potential lowering [Fig. 2(d), process 1] leads to thermionic emission [19,20]. The regimes of high- and low-temperature behavior always depend on the barrier height and geometry. Murphy and Good [19] and Hill [20] also derived a temperature-dependent Fowler-Nordheim equation. In a Fowler-Nordheim plot

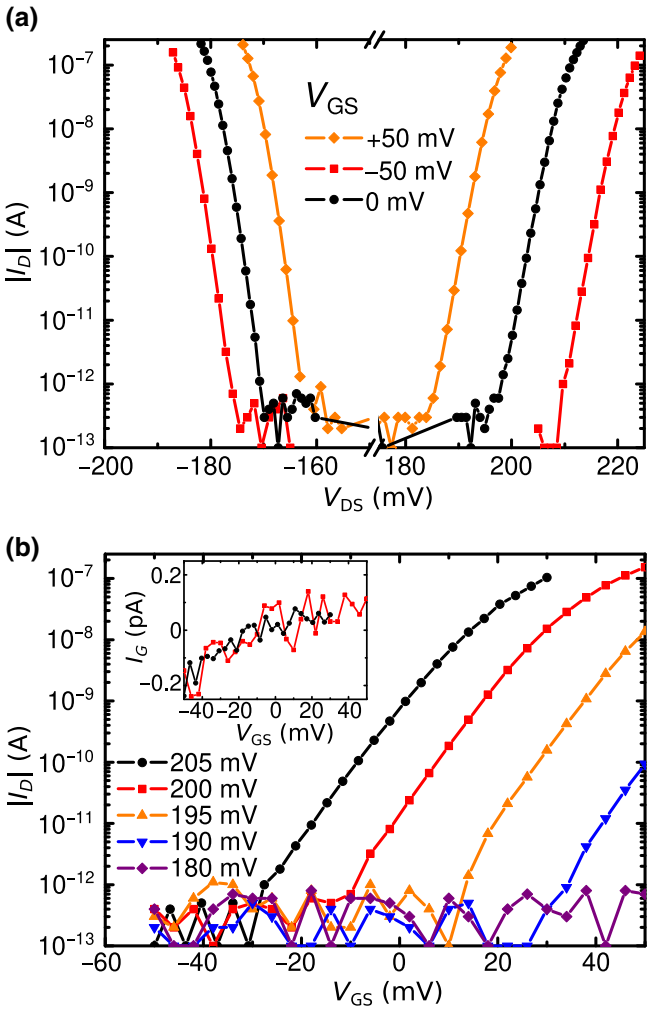

FIG. 4. (a) Drain-source-voltage sweeps for V_{GS} of 0, 50, and −50 mV at 1.2 K. (b) Gate-source-voltage sweeps for V_{DS} in the range from 180 to 205 mV. The inset shows the gate current for V_{GS} in the range from −50 to 50 mV.

$\left[\ln(I/V^2)\right.$ versus $\left.1/V\right]$ our I-V curve [Fig. 2(a)] is linear, a fact that is often claimed as evidence for Fowler-Nordheim tunneling. However, the Fowler-Nordheim equation shows only an increase in current density with increasing temperature, and the slope (in a Fowler-Nordheim plot) does not exhibit the explicit temperature dependence observed in our measurements. A change in slope would occur for a change in barrier height. This, however, would not result in the crossing of the I-V curves that we observe. Also, it should be noted that the strong dependence of the static dielectric constant $\epsilon_r(T,E)$ on the electric field [21–23] is not relevant for the tunneling process because the transit time through the thin barrier is too short for the lattice to respond (as pointed out by Scott [24]).

Thermionic emission with barrier lowering by the Schottky effect has both a strong temperature dependence and a strong field dependence and may be described by

$$J_S = \frac{4\pi mek_B^2}{h^3} T^2 \exp\left(-\frac{\Phi_{\text{eff}} - \beta_S\sqrt{\mathcal{E}}}{k_B T}\right), \qquad (1)$$

where $\beta_S = (e^3/4\pi\epsilon_0\epsilon_r)^{1/2}$, m is the effective electron mass, e is the electron charge, k_B is the Boltzmann constant, T is the absolute temperature, h is Planck's constant, $\mathcal{E}$ is the magnitude of the electric field, ϵ_r is the relative dielectric constant, and ϵ_0 is the permittivity of a vacuum. Equation (1) leads to higher currents for higher temperatures at any given electric field. It also predicts intersection points between I-V curves that move to higher current and electric field with increasing temperature. This, however, does not match our observations for all temperatures as in some cases the crossing points also move to lower current and electric field with increasing temperature, as shown in Fig. 3.

However, when fitting these I-V curves with Eq. (1) one is able to calculate an effective barrier height Φ_{eff} for each point $(I, V/\mathcal{E})$. In this way, an additional decreasing linear dependence of Φ_{eff} with respect to applied voltage emerges, which leads to $\Phi_{\text{eff}} = \Phi_0 + aV_{\text{DS}}$. This form of Φ_{eff} in Eq. (1) accurately fits both structure 1 and structure 2, as shown in Fig. 3. The fitting-parameter values are asymmetric with respect to the sign of the voltage, as discussed below. Since for usual Schottky emission no crossing between I-V curves can occur with a fixed potential barrier Φ_{eff}, the curve fits result in an increasing Φ_0 for increasing temperature. That leads, in combination with the decreasing slope of the semilogarithmic curve as temperature increases, to the creation of crossing points. Those points can be identified by the model by the formula

$$2\ln\left(\frac{T_1}{T_2}\right) = \frac{a_1 V + \Phi_{0,1} - \beta_S\sqrt{\mathcal{E}}}{k_B T_1} - \frac{a_2 V + \Phi_{0,2} - \beta_S\sqrt{\mathcal{E}}}{k_B T_2} \qquad (2)$$

with use of the condition $J_1(T_1) = J_2(T_2)$ and solving for V by taking $\mathcal{E} = \mathcal{V}/\mathcal{L}$. As a result, I-V curves recorded at different temperatures can show crossing points.

In our picture of two back-to-back Schottky diodes, one contact is always biased in the reverse direction and the other is always biased in the forward direction. Because of its higher resistance, only the reverse-biased contact needs to be considered. Within that picture small differences in the barrier height at the two different sides lead to an asymmetry of the I-V curves that must vanish at higher temperatures because of the decreasing $\Phi/(k_B T)$. The height of such a barrier may be lowered locally when O^{2+} vacancies are present at the interface [25]. In consequence, a different respective spatial distribution of vacancies at the two interfaces results in an asymmetry with respect to the sign of the bias voltage. This distribution of vacancies may be altered by the application of a

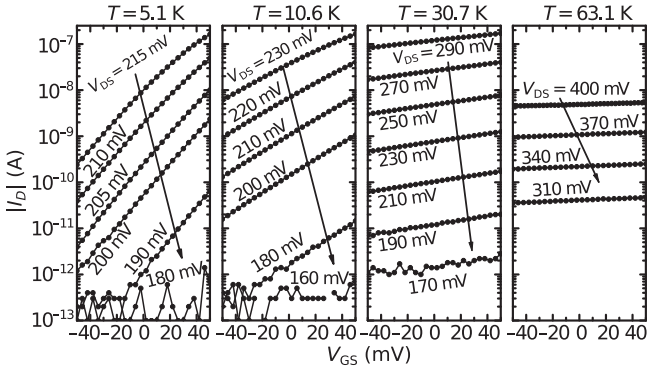

FIG. 5. Temperature-dependent V_{GS} sweeps for several V_{DS} values recorded for the same structure as shown in Fig. 4.

high bias voltage, leading to irreversible changes of the I-V curves (see Supplemental Material for shifted I-V curves after high bias voltage [26]). The irreversibility results from the fact that vacancies pushed into the 2DEG cannot travel back. These vacancies are exposed to a much smaller electric field within the 2DEG than in STO. Therefore, we observe only an increase in V_{th} and never a decrease, because the vacancy concentration inside the channel can only decrease. In addition to the O^{2+} vacancies, surface and interface states are expected to exist. Because of possible variations in the densities of the interface states, the work functions are expected to be different at the two separate junctions [27].

In addition to current flow via the conduction band, Lee *et al.* [9] suggested the existence of an impurity band in slightly-oxygen-reduced STO with strong temperature-dependent properties, due to the combination of low doping and the large temperature-dependent static dielectric constant [21–23]. Increasing the electric field

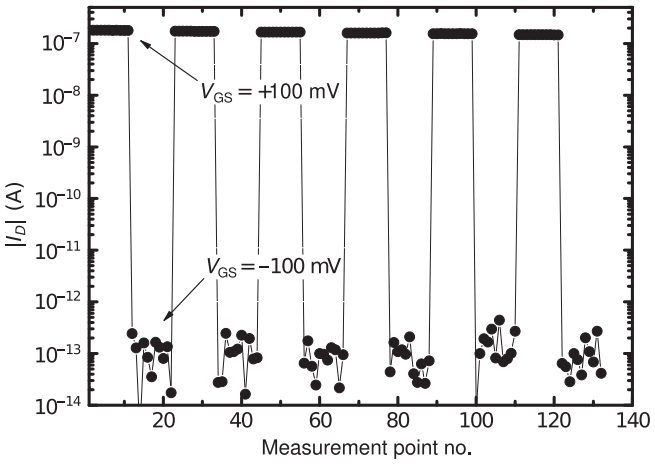

FIG. 6. Demonstration of an *on-off* switch at 1.2 K for an applied drain-source voltage of 57 mV and $V_{GS} = \pm 100$ mV. The *off* current is at the detection limit and the *on-off* ratio is at least 10^6.

and temperature reduces the static dielectric constant and thus increases the potential between the vacancies. Carriers trapped at the vacancies can surpass this potential more easily at elevated temperatures. This behavior would also indicate that the potential barrier in such an impurity band should be highly dependent on temperature and increase with increasing temperature.

By the application of a gate-source voltage, the bands within STO are shifted up or down depending on the sign of the gate-source voltage. This shift is expressed in a rise or reduction in Φ_0 through $\Phi_0 \pm \alpha_{GS} V_{GS}$, which results in an exponential change in current when one is sweeping the gate-source voltage. Since $\pm\alpha_{GS} V_{GS}$ is also divided by $k_B T$, a strong decrease in the gating effect is observed with increasing temperature. It is unlikely that the gate influences only the adjacent side of the channel because of the symmetric nature of the observed gate action. An asymmetric gate influence would change the conductance of the nearer side of the channel, while the other side would remain mainly unaffected. In this scenario it would be possible to open this side of the channel and increase the current accordingly by applying a certain gate-source voltage. However, a gate-source voltage of opposite sign would close only this side of the channel, while the remaining conductance of the other side would prevent an efficient current reduction. Because in our experiments we do not observe this asymmetry but rather observe a fully symmetric effect of the gate-source voltage, we can assume that the gate acts on the channel as a whole.

As Fig. 3 shows, the model fits the measurements almost perfectly; the lines indicate the fitted curves and the symbols represent the measurements. The crossing points are now linked to a change in effective barrier height Φ_0 and the parameter a. The parameters given by the fitting procedure are shown in Table I. For the calculation of I_D, an effective mass of $3m_e$, a high-frequency dielectric constant of $\epsilon_r = 5$ [22], and an emitter area $A = 5$ nm $\times$ 4 μm are used. For reduced STO thin films, Liu *et al.* [13] determined an activation energy of the oxygen vacancies of 25 meV between 200 and 300 K. In the case of unannealed c-LAO/STO samples, Liu *et al.* [28] reported an oxygen-vacancy activation energy of 4.2 meV below 100 K. Both were determined by Hall measurements. This gives an additional hint that the injection mechanism is electrode limited and not bulk limited due, for example, to Poole-Frenkel emission via oxygen vacancies. The increase in Φ_0 is noticeable from the data, because at low fields one would always expect an increase in current if the potential barrier is the same for all temperatures. Because of the different voltage regimes for the I-V curves for the different structures in Fig. 3, the fitting parameters necessarily have different values. However, when looking at the qualitative dependence of $\Phi_0(T)/a(T)$ on temperature, one can observe a very similar behavior for both structures. That mathematically supports our earlier statement that

TABLE I. Parameters used for the plotting in Fig. 3.

Structure 1	T (K)	Φ_0 (meV)	a (e)	Structure 2	T (K)	Φ_0 (meV)	a (e)
$+V/-V$	1.2	28.19/30.12	−0.041/0.067	$+V/-V$	1.2	15.1/15.7	−0.082/0.056
$+V/-V$	5.1	42.58/44.72	−0.097/0.135	$+V/-V$	5.1	21.4/21.4	−0.202/0.145
$+V/-V$	10.6	55.6/59.4	−0.132/0.192	$+V/-V$	10.6	25.2/25.2	−0.265/0.207
$+V/-V$	31.7	102.3/103	−0.222/0.259	$+V/-V$	31.7	42.2/42	−0.322/0.296
$+V/-V$	63	195/199.5	−0.275/0.301	$+V/-V$	63	101.6/102.1	−0.374/0.373
$+V/-V$	111	382.3/327.6	−0.429/0.297	$+V/-V$	111	209.4/211.4	−0.403/0.414

both structures show similar features in their I-V curves (indicated by the shaded areas in Fig. 3) but at different voltages. Also, the irreversible modification of the I-V characteristics can now be linked to motion of oxygen vacancies as observed in a recent study [29]. The presence of oxygen vacancies and their role in defining the threshold voltage are further confirmed by annealing experiments. Two samples are investigated for which an annealing step was part of the fabrication process. For one sample the patterning is done by dry etching and annealing is performed directly after the etching. The other sample is fabricated by the process described by Schneider *et al.* [11], which includes an *in situ* annealing step [26]. Both samples show an increased threshold voltage from the first measurement, in agreement with the increased threshold voltage with decreasing vacancy concentration described above.

Cen *et al.* [30] reported results for smaller three-terminal structures with gating; the three terminals were conducting lines induced in an insulating LAO/STO bilayer by a conducting AFM, and the spacings between the source, drain, and gate were up to 1 order of magnitude smaller than our channel. At high temperatures they observed an increase in conductance caused by thermal activation, and they suggested quantum field emission as a dominant transport mechanism at low temperatures, supported by the signature of STO phase transitions related to changes in ϵ_r. We suggest that the process suggested in Ref. [30] is not suitable for huge throughput and long device stability, in contrast to the RIE process used in our case. Because of smaller dimensions and higher applied voltages, the electric field in the experiment of Cen *et al.* [30] is much higher than that described here, leading to a different transport mechanism with a different temperature dependence. The larger dimensions of our device simply exclude any direct tunneling process between the contacts. The difference in functionality is also visible from the fact that we observe no influence of the structural phase transitions as described in Ref. [30].

IV. CONCLUSION

We show that it is possible to create a field-effect transistor based on transport through more than 100 nm of STO in an LAO/STO heterostructure. The transport is dominated by the Schottky barriers between the electron gas on both sides of the gap and the STO inside the gap, resulting in strong temperature-dependent and nonlinear I-V characteristics. Because of the large dielectric constant of STO, the barrier height can be controlled by a side gate-source voltage, resulting in full transistor functionality. The device is fabricated by state-of-the-art lithography and dry-etching processes. The results based on two different patterning processes (see Supplemental Material for transport characteristics in the a-LAO/c-LAO structure [26]) exclude transport through defects induced by dry etching. Our results show that due to the special properties of STO nanostructures in LAO/STO, there may still be an unrecognized potential for applications beyond classical device concepts. Even though the fabricated transistor shows little effect at elevated temperatures, the design concept demonstrates a natural way to include high-k dielectric materials into a transistor by using them for the gate and the channel as well, which is an advantage over commonly used silicon technology. Steep drain–source I-V curves enable gating with very low voltages and lead to a very low power switching. On the other hand, the experiments show the limitations of nanopatterning of LAO/STO devices. No matter whether the gap is fabricated by etching or by the method of Schneider *et al.* [11], a gap of less than 200-nm width between two regions of LAO/STO becomes conducting at relatively low bias voltages, greatly limiting the density of integrated nanodevices. For integration purposes, it may be necessary to add additional, "dummy" gates between different devices to efficiently insulate them from each other.

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A.M. did part of the processing, analyzed the data, performed all the transport measurements, and fit them to the model equations. C.Ş. and M.E.F. suggested the electric-field-dependent tunneling rate and derived the

resulting equations. M.Z.M. deposited the LAO layers by pulsed-laser deposition. B.F. did the reactive-ion etching. G.S. planned and supervised the experiment. All authors contributed to the manuscript and reviewed it before submission.

APPENDIX A: SAMPLE PREPARATION

The devices are fabricated from large-area LAO/STO heterostructures. These heterostructures are fabricated by pulsed-laser deposition of six-unit-cell LAO on (001)-oriented STO substrates. The substrates are prepared as described in previous studies [31,32]. For the deposition (fluency of 2 J/cm^2 at $f = 2$Hz) an O_2 pressure of 0.001 mbar at a temperature of 850 °C is used.

The layers are patterned by electron-beam lithography and dry etching. PMMA is used as an electron-beam resist and subsequent etch mask. The exposure is done at an acceleration voltage of 30 kV with use of a RAITH PIONEER exposure tool. After development, the LAO is patterned by dry etching down to the STO substrate by the etching process described in Ref. [10]. The *a*-LAO layer is patterned by a standard PMMA lift-off process. For the process described in Fig. 1, the *a*-LAO layer is annealed for 1 h at 650 °C in an O_2 atmosphere to make the interface insulating [28]. No contact metallization is used but the electron gas is contacted electrically by direct ultrasonic bonding through the LAO.

APPENDIX B: MEASUREMENT

The samples are characterized in a ^{4}He-bath cryostat with a variable-temperature insert that allows measurements down to 1.2 K. Voltages are applied using high-precision homebuilt 20-bit digital-to-analog converters. The source current is measured by either a multiple-range current amplifier with a noise floor of approximately 200 fA or a homebuilt current amplifier with fixed gain. The gate current is measured via the voltage drop over a 10-MΩ series resistor. All voltages are measured with high-precision, high-impedance difference amplifiers connected to an Agilent 34420A nanovoltmeter.

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