Modeling Computer Memory Based on Ferromagnetic/Superconductor Multilayers

S.E. Shafraniuk,[1,*] I.P. Nevirkovets,[2] and O.A. Mukhanov[2]

[1] *Tegri LLC, 558 Michigan Avenue, Evanston, Illinois 60208, USA*

[2] *Hypres Inc., 175 Clearbrook Road, Elmsford, New York 10523, USA*

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A model of superconducting computer memory exploiting the orthogonal spin transfer (OST) in a pseudo-spin-valve (PSV) that is controlled by a three-terminal Josephson superconducting-ferromagnetic transistor (SFT) is developed. The building blocks of the memory are hybrid PSV and SFT structures. The memory model is formulated in terms of the equation-defined PSV and SFT devices integrated into the PSV-SFT-memory-cell (MC) circuit. Logical units "0" and "1" are associated with the two PSV states characterized by two different resistance values. Elementary logical operations comprising the read-write processes occur when a word pulse applied to the SFT's injector coincides with the respective bit pulse acting on the MC. Physically, a word pulse switches the SFT to a resistive state, causing PSV switching between the logical "0" and "1" states. Thus, the whole switching dynamics of the MC depends on the nonequilibrium and nonstationary properties of the PSV and SFT. Modeling of the single MC as well as larger MC-based circuits comprising 12 and 30 elements, respectively, suggests that such memory cells can undergo ultrafast switching (subnanosecond) and have low energy consumption per operation (sub-100 fJ). The model suggested allows the study of the influence of noise, the punch-through effect, cross talk, parasitic effects, etc. The results obtained suggest that the hybrid PSV-SFT structures are well suited to superconducting computing circuits as they are built from magnetic and nonmagnetic transition metals and therefore have low impedances (1–30 Ω).

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I. INTRODUCTION

Issues of local overheating and thermal management in contemporary digital semiconducting circuits, serving as an element base for current computers, are the major impediments to progress in this area [1]. Presently, computing information is processed by transmitting the electric pulses that trigger logic elements in a circuit involving semiconducting diodes and transistors. Such elements release Joule heat when subjected to electric signals. In large circuits, comprising approximately 10^6–10^8 elements per chip, the total amount of released heat is great, hampering the whole computer's performance [2]. Today, as a power supply for a supercomputer, typically a small power plant is needed. The overheating issue becomes greater when the clock frequency and the element density in the circuits increase. One promising solution to this long-standing problem affecting computing efficiency and speed is the development of Josephson-based electronics [1,3–6], whose basic physical principles and functionality are quite different from those of their semiconducting transistor counterparts. Although in both semiconductors and superconductors there is an energy gap in the quasiparticle excitation spectrum, the quantum coherence of the superfluid condensate of the latter suggests remarkable properties. The benefit is that the finite voltage state of the Josephson junction (JJ) is not related to energy dissipation, and thus no Joule heat is released. The finite voltage across the JJ results from the time-dependent change of the condensate's phase difference occurring without energy dissipation. For such a reason, the energy dissipation does not impact the clock speed of superconducting electronic circuits as happens in their semiconducting counterparts. Since the superconducting wires and logic elements release much less heat than their normal and semiconducting counterparts, the energy efficiency of the computing process is increased by several orders of magnitude. Furthermore, the switching speed of the Josephson-based logic elements is much greater than that of semiconducting devices [1,3–6]. Besides, recent progress in increasing the cooling efficiency and improving the thermal management [7] based on newly discovered two-dimensional materials makes superconducting computing even more promising.

Superconducting and semiconducting electronics [1,3–6] are based on distinct physical principles. In particular, present superconducting circuits are typically

*serhii.sh@hotmail.com

designed with Josephson junctions with only two terminals, and the absence of a superconducting-transistor element imposes restrictions on the overall circuit's performance and also limits its capabilities. Therefore, on the path to creating a fully functional and efficient superconducting computer, there remain important technical issues that require further elaboration. One of the key problems is the development of a three-terminal Josephson transistor [8–11] that would essentially simplify the design of the whole superconducting electronics. In particular, the Josephson transistor, when available, would essentially diversify the schematics and improve the overall performance, since the digital logic based on three-terminal Josephson transistors [8–11] would benefit from reduction of the fan-out effect, noise, and errors, which hamper the performance of currently available Josephson digital circuits [1,6,12,13].

Another emerging problem is the development of high-density, fast, energy-efficient nonvolatile, and nondestructive superconducting computer memory. Presently known solutions either fail to function as nonvolatile, nondestructive memory or lack satisfactory energy efficiency, speed, and stability. Existing computer memory is based on semiconducting transistors consuming a considerable amount of energy and switching at limited speed, which impairs its overall performance. Furthermore, when coupled with superconducting circuits, semiconductors become a source of noise and errors.

In this paper we consider a circuit model of computer memory (see Fig. 1), whose elements are built with a pseudo-spin-valve (PSV) coupled to a three-terminal Josephson superconducting-ferromagnetic transistor (SFT), based on a hybrid superconductor/ferromagnetic multilayer [8–10,14]. The model is elaborated on the basis of our previous experimental measurements and theoretical study of PSV [15–18] and SFT [8–10,14] structures. The experimental and theoretical data [8–10,14–18] are reformulated here in terms of equation-defined devices (EDDs) comprising a PSV-SFT-memory-cell (MC) circuit. We describe the physics of the devices, the SFT and the pseudo-spin-valve, in terms of small phenomenological models, as explained in Secs. II–IV. We see that such models (see Secs. II–IV) are more suitable for studying practical applications in large circuits as the previous microscopic models [14,19,20] are too cumbersome and are good only for single devices. The aims of this work are as follows: (i) to introduce compact models of the SFT and the pseudo-spin-valve to improve the design capabilities for large superconducting circuits; (ii) to tailor the smaller phenomenological models to match the complex microscopic theory and the experimental data [14,19,20] that are impractical in large-circuit simulations; (iii) to simplify the phenomenological models as much as possible to increase the speed and quality of large-circuit simulations. The PSV functionality exploits the

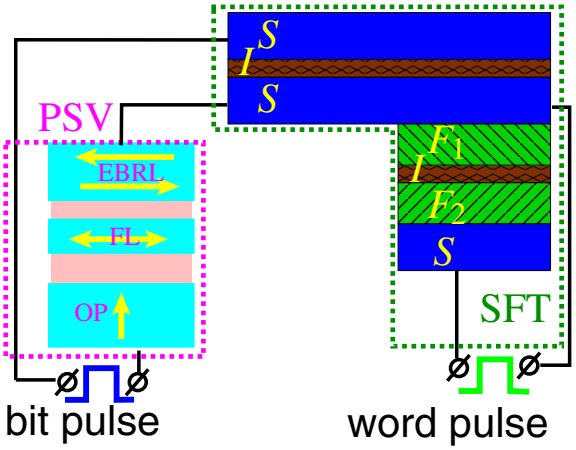

FIG. 1. Computer MC based on a PSV controlled by a SFT. EBRL is the exchange-biased synthetic antiferromagnet reference layer and FL is the in-plane-magnetized soft free layer controlled by the out-of-plane polarizer (OP), I is the dielectric barrier, S is the superconductor, F_1 and F_2 are two different ferromagnets

phenomenon of orthogonal spin transfer (OST) [15–18], initialized by the subnanosecond pulses of the bias electric current altering the magnitude of pseudo-spin-valve resistance $R_{\rm PSV}$ between the minimum R_L and the maximum R_H. Such PSV switching is controlled by use of nonequilibrium-quasiparticle injection to suppress the critical Josephson supercurrent in the SFT. Thus, the STF injector acts as the base electrode of the transistor, while the two superconducting layers of the superconductor-insulator-superconductor (*S*-*I*-*S*) subjunction correspond to the emitter and the collector.

Circuit simulations allow the optimal parameters of the hybrid memory cell that ensure the best memory performance to be found. The two PSV states characterized by R_L and R_H, respectively, are associated with the logical units "0" and "1." Reading-writing the logical information is performed by applying a word pulse to the SFT's injector. On the one hand, the nonequilibrium-quasiparticle injection suppresses the superconductivity in the acceptor *S*-*I*-*S* junction, thereby reducing the magnitude $I_{\rm ca}$ of its critical supercurrent. Thus, by applying a word pulse to the SFT's injector, one switches the *S*-*I*-*S* acceptor to the resistive state. On the other hand, the *S*-*I*-*S* acceptor is coupled to the PSV, which is subjected to bit pulses. When the word and bit pulses act simultaneously, the cumulative transport current becomes sufficiently strong to alter the PSV state, forcing the free layer to change its polarization with respect to the in-plane-polarized reference layer from parallel to antiparallel, or vice versa. Below we see that *S*-*I*-*S* switching from a superconducting state to a resistive state (or vice versa) can be exploited to control the PSV resistance.

Thus, a necessary condition for the reading-writing process to occur is that the word pulse coincides with the

respective bit pulse acting on the MC. Physically, a word pulse switches the Josephson *S-I-S* subjunction part of the SFT to a finite-voltage (resistive) state, causing PSV switching between the logical "0" and "1" states, manifesting itself as the elementary read-write process. The whole switching dynamics of the PSV-SFT memory cell depends on the nonequilibrium and nonstationary properties of the structural components. Other important factors determining the switching dynamics are the geometry and the design of the memory circuit, which must be elaborated and optimized to reduce parasitic effects, cross talk, and noise as well as to improve the overall thermal management. The goal of this work is to study the nonstationary dynamics of PSV-SFT memory using SPICE and QUCS simulators complemented by the MATHEMATICA and MATLAB toolboxes. We perform numerical simulations of the single PSV-SFT memory cell and larger computer memory circuits comprising 12 and 30 elements.

II. MODELING THE PSV AND SFT DEVICES

Design, validation, and optimization of electronic circuits is accomplished by computer-aided design (CAD) and circuit simulations. CAD tools are used to develop semiconducting integrated circuits; However, they are not mature enough for superconducting digital electronics [21]. When new devices are invented, one should make significant efforts to properly define them and integrate into electronic circuits. Fabricating the devices and even explaining their physics with complex microscopic models does not guarantee they will properly function in the circuits. This motivates verification of whether such devices can function as elements of large superconducting circuits. Nonetheless, circuit simulations cannot run without simple but adequate phenomenological models describing the basic physical properties of the SFT and pseudo-spin-valve devices. Since the working principles of the devices are very different from the physics of traditional electronic elements, the answer is far from trivial. This work aims to show that devices such as the SFT and pseudo-spin-valve are able to work as elements of a superconducting electronic circuit. In the following sections we build the required phenomenological models matching the microscopic theories [14,19,20] and fulfilling the requirements of circuit simulators. The agility and simplicity of the phenomenological models allows the simulation of quite complex superconducting memory circuits, which would be impossible with use of the former microscopic models. The compact models of the three-terminal SFT and the two-terminal pseudo-spin-valve thus allow the demonstration that such the devices are suitable for practical applications as they can function as key elements of large superconducting circuits: the SFT governs the switching of the pseudo-spin-valve posing as a memory cell of a superconducting computer.

A variety of superconducting digital logic devices are based on rapid-single-flux-quantum technology [1,12,13], which has existed for almost three decades. But progress in rapid-single-flux-quantum technology was slowed by a shortage of necessary circuit elements. One example was the absence of a three-terminal superconducting transistor, which complicated the design of electric pulse generators, triggers, and switches. This motivated efforts toward the development of efficient simulation methods that would facilitate successful progress in this field. There were numerous attempts to elaborate the superconducting electronics by adopting simulators traditionally used for development of semiconducting circuits. The most-popular and most-available CAD tools [21] for superconducting electronics include the SPICE simulator [22,23], which serves as a platform to design and implement models for Josephson-based superconducting electronic circuits.

Here we implement a similar approach to elaborate models of the SFT [8–11] of the MC made of the hybrid PSV-SFT device depicted in Fig. 1 and of larger superconducting memory circuits. The PSV and SFT devices, representing the key parts of the MC, behave as highly nonlinear elements with essential reactive impedance components (i.e., either as capacitive or as inductive). Orthogonal-spin-transfer pseudo-spin-valve nanopillar devices [16,24–30] containing an out-of-plane-magnetized polarizing layer and an in-plane-magnetized spin-valve structure show promise as cryogenic magnetic memory elements [19,20,32,33]. PSVs exhibit ultrafast switching (subnanosecond) and low energy consumption per operation (sub-100 fJ) owing to large initial spin-transfer torque from the perpendicular polarizer. Furthermore, these devices are well suited to integration with Josephson-junction circuits as they comprise magnetic and nonmagnetic transition metals and therefore have low impedances (1–30 Ω). However, because a PSV has only two terminals, it cannot be suitably controlled, which limits its functionality as a memory-circuit element. In this work, we extend the capabilities of a PSV by integrating it with a SFT, which results in a fully functional memory cell. First, we formulate and study the models of single PSV and SFT elements as shown in Figs. 12 and 13 (see the Appendix). In the next step, we integrate the two models to derive a model of the MC. The functional model of the MC is then used in the subsequent development of larger MC-based memory circuits comprising 12 and 30 elements, which are well suited for studying the basic functionality of the PSV-SFT computer memory. Schematics of the PSV and SFT blocks developed in either graphical form or text form in the SPICE [23,34] and QUCS [35–37] simulation environments [38,39] are converted to a system of linear or nonlinear differential equations that effectively are the result of all the individual components in the circuit. In this way, every circuit component in the simulator is regarded as the compact model of the circuit. The simulation parameters are

the coefficients of these sets of equations. Mathematically, the equations are deduced from nodal analysis and the software uses numerical models of the equation systems to solve them, focusing on the specified circuit analysis. Respective compact models are derived for analysis of every kind of component—transient, dc, ac and temperature—aiming to represent them in a suitable form. Such a form is then used for circuit solutions in SPICE and QUCS [38,39]. Below we describe how to formulate the model for SPICE and QUCS by including the defined nonlinear devices in the circuit and solving the system of equations in the circuit setup. We conduct the numerical analyses and find circuit solutions the allow understanding of and implementation of the device along with the other circuit components under arbitrary conditions that are discussed, without considering particular details of the simulation tools or coding methods.

III. SFT JOSEPHSON TRANSISTOR

To accomplish the switching between logical states of the two-terminal PSV, we combine it with a three-terminal SFT, whose electrical circuit diagram is shown in Fig. 12. Namely, the two devices, PSV and SFT, are combined in a hybrid electronic circuit comprising the computer memory cell, whose logical states are triggered by the SFT introduced and studied in Refs. [8–11]. The SFT device [8–11] is modeled as an electronic circuit with nonlinear elements in the form of analytical expressions for the electric current $I = I_R + I_C + I_J$, which consists of the active quasiparticle $I_R = V_R/R$ and reactive capacitive $I_C = C(dV_C/dt)$ components complemented by the Josephson supercurrent,

$$I_J = J_c \sin\varphi = J_c \sin\left[\frac{2\pi}{\Phi_0}\int V_J(t)dt\right], \qquad (1)$$

where φ and V_J are the superfluid condensate phase difference and the voltage across the junction, respectively, Φ_0 is the quantum flux, and we have used the Josephson relationship

$$\frac{d\varphi}{dt} = \frac{2\pi}{\Phi_0}V_J(t). \qquad (2)$$

It is instructive to represent the Josephson supercurrent in another form as

$$I_J = \frac{\int V_J(t)dt}{L_J(V_J, I_J)}, \qquad (3)$$

where we have introduced the effective nonlinear inductance

$$L_J = \frac{\Phi_0}{2\pi I_J}\arcsin\left(\frac{I_J}{J_c}\right). \qquad (4)$$

In the above formulas, the resistance R, the capacitance C, and the inductance L_J of the S-I-S subjunction (see Fig. 1), which represent the components of the SFT, are nonlinear functions of the electric currents I_i and bias voltages V_i (where $i = R, C, J$) related to the respective branches the SFT circuit.

The electric current through the S-I-S subjunction of the SFT is described by the resistively and capacitively shunted junction (RCSJ) model in terms of the second-order differential equations for φ. In the S-I-S, the system oscillates in a potential well, giving rise to the sinusoidal current description given by Eq. (1). The phase-dependent Josephson-junction energy $U(\varphi)$ takes the form of the washboard potential, whose slope increases with the bias current I as shown in Fig. 2(a). Flexibility of control in

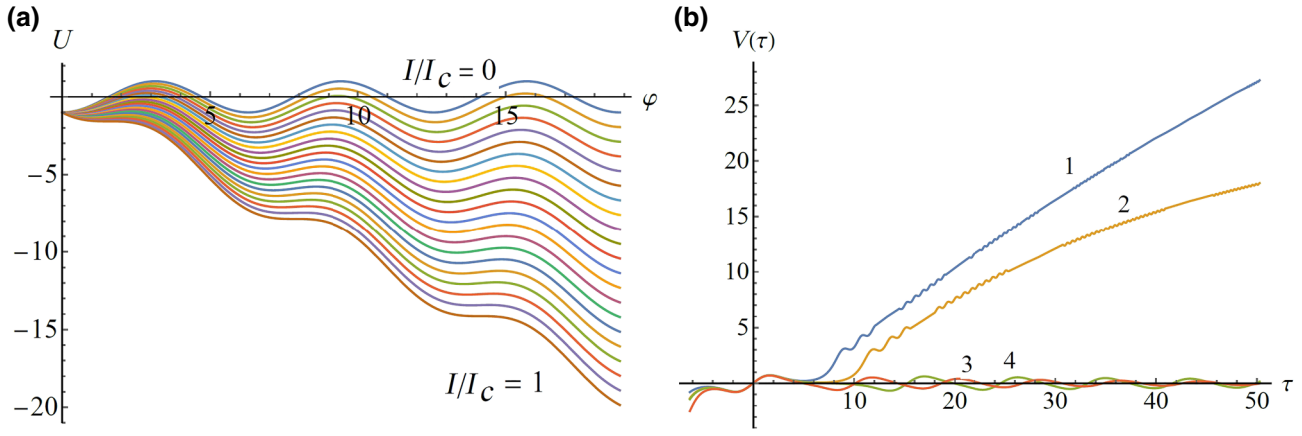

FIG. 2. Nonstationary properties of the SFT. (a) The washboard potential $U(\varphi)$ tilts more strongly as the bias current increases from $I/J_c = 0$ to $I/J_c = 1$. In the SFT, the tilt is changed by adjustment of either I or J_c, achieving much better flexibility of control as compared with a conventional Josephson junction, where the tilt is controlled only by I. (b) Time dependence of the JJ voltage $V(\tau)$, where $\tau = \omega_J t$ is the dimensionless time and ω_J is the Josephson plasma frequency. Curves 1, 2, 3, and 4 are related to $\beta_J = 0.01,\ 0.03,\ 0.033$, and 0.065, respectively. In the SFT one can readily alter both ω_J and β_J by changing merely the injector current.

the SFT is accomplished by changing the tilt by adjusting either I or J_c, which is impossible in a conventional Josephson junction, where the tilt is controlled only by I. Furthermore, in the SFT one can readily alter both ω_J and β_J by merely changing the injector current. When enough bias current is applied, the height of the potential well decreases and the system rolls off to lower potential wells, losing energy due to dissipation. When I is small, the system can get into the next potential well because of phase diffusion, meaning that thermal activation is responsible for particles crossing the energy barrier [6]. The total electric current through the S-I-S is

$$I = I_J + I_R + I_C, \tag{5}$$

which gives the differential equation in the form

$$J_c \sin\varphi + \frac{V}{R_N} + C\frac{dV}{dt} = 1. \tag{6}$$

To compute the dc current-voltage characteristic, we need to know the time-averaged voltage:

$$\langle V\rangle = \frac{\hbar}{2e}\left\langle\frac{d\varphi}{dt}\right\rangle = J_c R_N \beta_J \left\langle\frac{d\varphi}{d\tau}\right\rangle, \tag{7}$$

where J_c is the critical current, $\tau = \omega_J t$ is the dimensionless time, R_N is the normal state resistance,

$$\beta_J = \frac{1}{\omega_J R_N C}, \tag{8}$$

and the ω_J is the Josephson plasma frequency

$$\omega_J = \sqrt{\frac{2eI_c}{\hbar C}}. \tag{9}$$

The McCumber parameter β_c is given by

$$\beta_c = \frac{1}{\beta_J^2} = \frac{2e}{\hbar} I_c R_N^2 C. \tag{10}$$

A simple analytical expression is obtained when the S-I-S subjunction capacitance is small. In this limit, $\beta_J \gg 1$ and the Eq. (6) is reduced to

$$\beta_J \frac{d\varphi}{d\tau} + \sin\varphi = \kappa, \tag{11}$$

where $\kappa = I/J_c$ and

$$\langle V\rangle = J_c R_N \beta_J \left\langle\frac{d\varphi}{d\tau}\right\rangle = J_c R_N \beta_J \frac{1}{T}\int_0^T \frac{d\varphi}{d\tau} d\tau = 2\pi J_c R_N \frac{\beta_J}{T}, \tag{12}$$

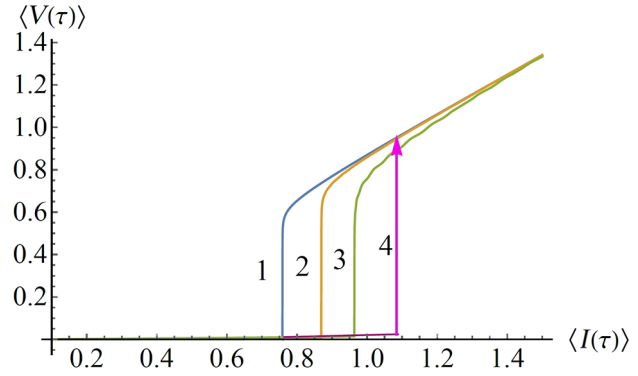

FIG. 3. Time-averaged curves of the SFT acceptor dc return current $\langle V(\tau)\rangle$ versus $\langle I(\tau)\rangle$ for $\beta_J = 0.05$ (curve 1), $\beta_J = 0.3$ (curve 2), and $\beta_J = 0.6$ (curve 3). One can see the hysteresis (curve 4) is larger for smaller β_J.

where the period T is defined by

$$T = \frac{2\pi}{\sqrt{\kappa^2 - 1}}\beta_J. \tag{13}$$

Using

$$T = \int_0^T \frac{d\varphi}{\left(\frac{d\varphi}{d\tau}\right)} = \beta_J \int_0^{2\pi} \frac{d\varphi}{\kappa - \sin\varphi}, \tag{14}$$

we find

$$\frac{T}{\beta_J} = \frac{2\pi}{\sqrt{\kappa^2 - 1}}\theta(\kappa - 1), \tag{15}$$

which gives

$$\langle V\rangle = 2\pi I_c R_N \frac{\beta_J}{T} = I_c R_N \sqrt{\kappa^2 - 1}. \tag{16}$$

For a JJ with an arbitrary capacitance C, we solve Eq. (6) numerically. Respective results are given in Figs. 2 and 3: in Fig. 2(a), we show the Josephson energy $U(\varphi)$, and in Fig. 2(b) we show the time-dependent voltage $V(\tau)$; in Fig. 3 we present the I-V curve of the JJ computed by solving Eq. (6) and finding the time-average $\langle V(\tau)\rangle$ versus $\langle I(\tau)\rangle$.

In low-transparency superconducting tunneling junctions, I_R is a nonlinear function of V_R, with threshold $V_R = 2\Delta/e$, where Δ is the superconducting energy gap in the banks of the S-I-S junction [40]. Furthermore, if there are also resistive and capacitance branches of the three-branch

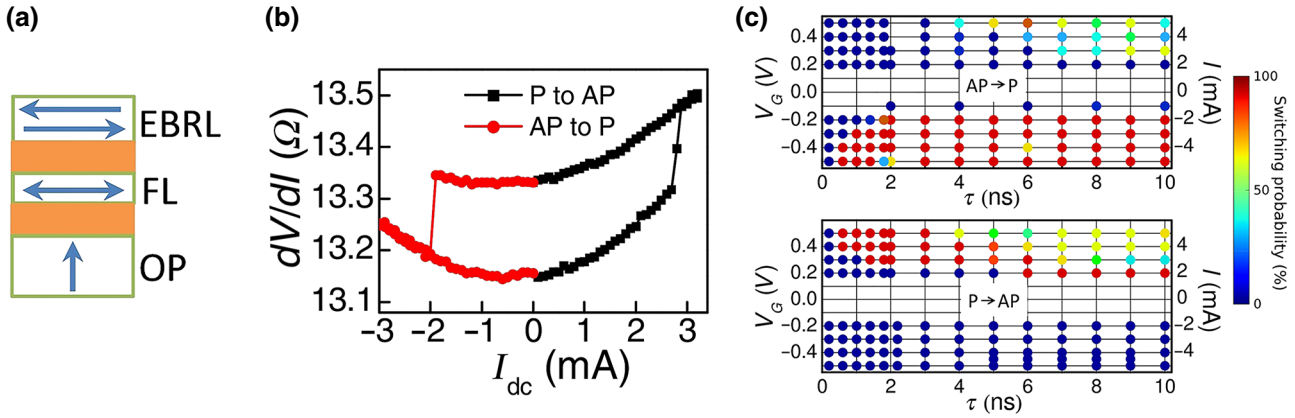

FIG. 4. Experimental data used to build simplified phenomenological models of the PSV [15]. (a) The PSV where the out-of-plane polarizer (OP) controls magnetization of the free layer (FL) coupled to the in-plane-magnetized exchange-biased reference layer (EBRL). (b) The OST switching diagram [15–18] modeled by the EDD, according to Eqs. (18)–(21). (c) Switching probability diagram [15] expressed as voltage V_G (y axis) versus duration τ (x axis) mimicked by Eq. (25). The estimated pulsed current (I) at the device is shown on the second y axis. Red marks the maximal (100%) switching probability, whereas dark blue means the absence of switching events. AP, antiparallel, P, parallel. Reproduced with permissions from AIP, Ref. [15].

EDD, then

$$I_J = I - I_R - I_s, \tag{17}$$

which gives the nonlinear inductance of the Josephson junction in the form

$$L_J = \frac{\Phi_0}{2\pi}\frac{1}{I - I_R - I_s}\arcsin\left(\frac{I - I_R - I_s}{I_c}\right), \tag{18}$$

where I_s is the Josephson supercurrent. In the three-terminal SFT, where the *S-I-S* Josephson subjunction is integrated with the nonequilibrium-quasiparticle *S-F-I-F-S* injector, as sketched in Fig. 1, the magnitude of the *S-I-S* critical current I_c is suppressed owing to the quasiparticle injection [8–11]. The electrical circuit diagram of the SFT is shown in Fig. 12, and the respective SFT-EDD subcircuit is depicted in Fig. 13. Thus, when applying Eq. (1) to the SFT, we assume that I_c depends on the *S-F-I-F-S*-injector bias current I_i as shown in Fig. 13 (Right). In our SFT circuits shown in Figs. 12 and 13, the suppression of I_{ca} by the *S-F-I-F-S* injector in Eq. (1) is modeled by an approximate analytical function with a bell shape:

$$I_{ca} = \frac{I_{c0}}{1 + \sinh^2\left(\frac{V_{inj}}{V_{wd}}\right)}, \tag{19}$$

where V_{inj} is the injector bias voltage and V_{wd} is the bell width, which are obtained from experiments [8–11] or numerical simulations [41,42]. Equation (19) mimics the experimentally obtained curve $\delta I_{ca}/\delta I_i$ shown on the right in Fig. 13, as we set $I_i = V_{inj}/R_i$, where R_i is the injector resistance. For the SFT modeling we use typical values $V_{wd} = 2$ mV and $V_{inj} = 0 - 20$ mV. The circuit parameters in Fig. 12 are selected to maximize the transistor effect when the electric pulses on the source V1 with amplitude $V_1 = 50\ \mu$V to 1 mV and duration $\tau_p = 0.13$ ps applied to the SFT base cause substantial change of the electric potential $V_{node\,1}(t)$ at node 1, as is evident from the respective transient-analysis diagrams shown in Fig. 5. The respective electric current pulses are measured by probe Pr1. A strong transistor effect is observed for $R_1 = R_2 = 1\ \Omega$, $R_3 = 13\ \Omega$, and electric potential $V_2 = 60$ mV at source V2. The respective subcircuit parameters in Figs. 12 and 13 (see equation-defined device D1 on the left in Fig. 13) are $R_9 = 1$ MΩ, $R_6 = R_7 = 0.1\ \Omega$, $R_3 = R_8 = 0.8\ \Omega$, and $C_2 = 0.001$ fF.

In the following sections, using the EDD model of the SFT formulated above, we elaborate electronic circuits exploiting the Josephson-transistor effect. Adding the SFT elements to the superconducting electronic circuits gives considerable benefits. First, the circuitry is greatly simplified; while many unwanted side effects are excluded. Second, a strong advantage of the SFT-based circuits is that they consume much less energy and can function at much higher clock speed than their semiconducting counterparts. Other alternatives to a SFT were considered in Refs. [43–45]. According to our estimations [14], the SFT design has better capabilities to control the other elements in the circuits when working to switch pseudo-spin-valves in computer memory as discussed below.

IV. HYSTERESIS IN JOSEPHSON JUNCTIONS

The electric current I between two superconductors separated by a weak link forming a Josephson junction

flows without dissipation until I reaches a critical current I_c, at which a finite bias voltage appears. The I-V curve is described by the RCSJ model [13]. In conventional S-I-S Josephson junctions, the hysteresis in the current-voltage characteristic is determined by the junction capacitance C when it is relatively large. Another hysteresis mechanism occurs in lateral superconductor–normal-metal–superconductor (S-N-S) junctions, where the distance between the two superconducting electrodes results in a small capacitance, much lower than in a typical S-I-S junction. Then, an observable hysteresis occurs in lateral junctions owing to local heating in the normal-metal spacer when their critical current is large: once the junction has switched to the resistive branch, it does not recover the superconducting state until the bias current is decreased to a significantly smaller retrapping current I_r. Such hysteresis was observed in superconducting constrictions and microbridges (see respective references in Ref. [46]), superconducting nanowires, normal metals, two-dimensional electron gases, semiconductor nanowires, carbon nanotubes, and graphene. Thus, there are two known mechanisms explaining the hysteresis: (i) excessive Joule heat in the weak link induces there an increase of the local temperature; (ii) the effective capacitance is larger than the geometric capacitance.

Before conducting transient simulations, we briefly discuss the time-averaged properties of the SFT. In Figs. 2 and 3 we present numerical solutions for the current-biased SFT illustrating its nonstationary properties. From Fig. 2(a), one can see that the washboard potential $U(\varphi)$ tilts more strongly as the bias current increases from $I/I_c = 0$ to $I/I_c = 1$. The $U(\varphi)$ slope changes by adjustment of either I or I_c, which provides much better flexibility of control in the SFT, as compared with a conventional Josephson junction, where the slope is controlled only by I. In Fig. 2(b), we show the time dependence of the SFT voltage $V(\tau)$, where $\tau = \omega_J t$ is the dimensionless time, ω_J is the Josephson plasma frequency, and curves 1, 2, 3, and 4 are related, respectively, to $\beta_J = 0.01,\ 0.03,\ 0.033$, and 0.065. In Fig. 3, we show the time-averaged SFT dc return-current curves $\langle V(\tau)\rangle$ versus $\langle I(\tau)\rangle$ for $\beta_J = 0.05$ (curve 1), $\beta_J = 0.3$ (curve 2), and $\beta_J = 0.6$ (curve 3). Remarkably, in the SFT one can readily alter both ω_J and β_J by merely changing the injector current. From Fig. 3 one can conclude that the I-V curves of such junctions show hysteresis, which becomes larger for smaller β_J. In this work we include the I-V-curve hysteresis in the circuit model regardless of its microscopic mechanism by approximating the quasiparticle branch of the I-V curve by a simple analytical expression, while the Josephson supercurrent is found by our solving the RCSJ equations in the course of the circuit simulations. Coefficients of the RCSJ equations that correspond to certain magnitudes of the normal-state resistance, capacitance, and critical supercurrent are

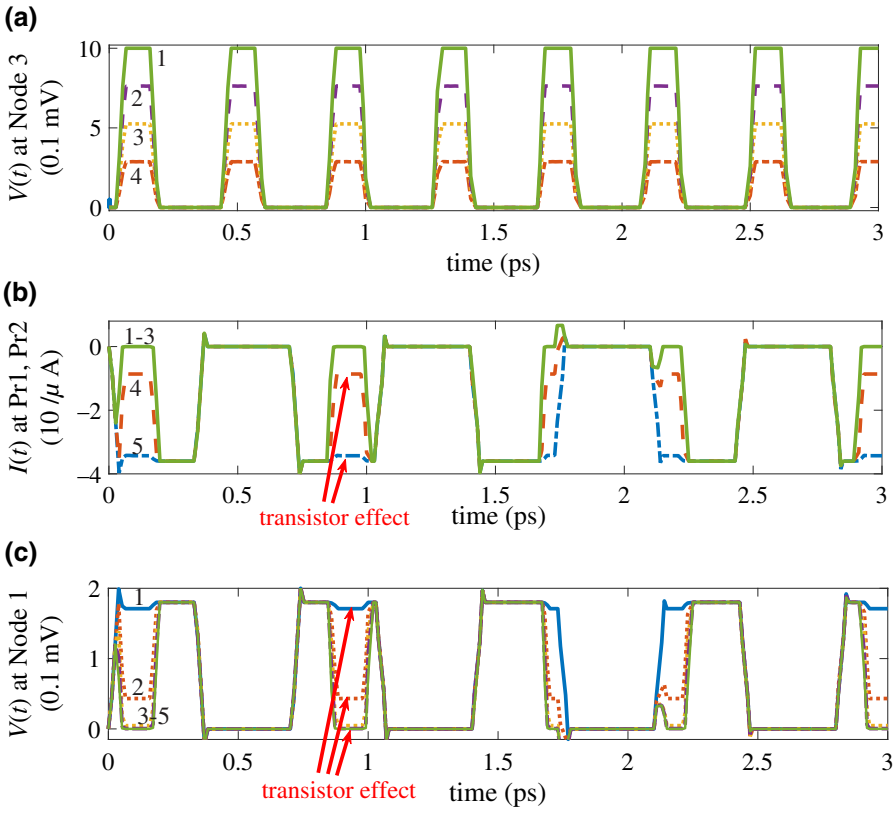

FIG. 5. Transition-analysis diagrams of the test circuit (see Figs. 12 and 13) of a SFT serving as a Josephson transistor. One can notice a strong transistor effect detected by the electric current probes Pr1 and Pr2 and the time-dependent voltage $V(t)$ at Node 1. Curves 1–5 correspond to voltage-pulse amplitudes $U_{\rm in} = 5\ \mu$V, 287 μV, 1 mV, 5 mV, and 10 mV, respectively, at the source V1.

selected by our optimizing the circuit performance in the course of simulations.

V. PSEUDO-SPIN-VALVE

The PSV, whose switching is induced by OST [5–9], controlled by the SFT, serves as an elementary cell of the memory circuit. The PSV nanopillar devices contain an out-of-plane-magnetized polarizing layer and an in-plane-magnetized spin-valve structure. These devices are compatible with Josephson-junction circuits.

We describe the logical states of superconducting digital circuits in terms of the state variable *St*. For a particular PSV element, the initial *state parameter* is defined as

$$S_{\rm st} = \begin{cases} 0 \text{ for } \uparrow\uparrow, \\ 1 \text{ for } \uparrow\downarrow, \end{cases} \tag{20}$$

where $\uparrow\uparrow$ and $\uparrow\downarrow$ stand for the parallel and antiparallel magnetization, respectively. As a departure point, we use the experimentally measured switching diagram of the OST-PSV resistance $R_{\rm PSV}(I) = dV(I)/dI$, where I and V are the bias current and voltage, respectively, depicted in Fig. 4. The hysteresis in $R_{\rm PSV}(I)$ is described in terms of an EED. The state variable *St*, related to the lower R_L and higher R_H values of $R_{\rm PSV}(I)$ is set by the magnitude of the magnetic field H (or by the bias current). Typically, the PSV switching characteristics show strong hysteresis that must be properly accounted for in the circuit simulations. Specifically, the PSV-state switching forth $0 \to 1$ and back $1 \to 0$ occurs at different magnitudes of the bias voltage. Therefore, we introduce the two lower $V_{\rm Ll}$, $V_{\rm Lr}$ and two higher $V_{\rm Hl}$, $V_{\rm Hr}$ switching voltages that are established by particular PSV geometry and material parameters. The simplest analytical form of $R_{\rm PSV}$ is written using the stepwise function $\theta(x)$:

$$\begin{aligned} R_{\rm PSV}(V) = {} & \theta(V_{\rm Lr} - V)\delta_{S,0}R_L \\ & + \theta(V - V_{\rm Lr})\theta(V_{\rm Hr} - V)\delta_{S,0}[R_L + S_{\rm sl}(V_{\rm Hr} - V)] \\ & + \theta(V - V_{\rm Hl})\delta_{S,1}R_H \\ & + \theta(V_{\rm Hl} - V)\theta(V - V_{\rm Ll})\delta_{S,1}[R_L + S_{\rm sl}(V_{\rm Hl} - V)], \end{aligned} \tag{21}$$

where $S_{\rm sl}$ is a finite slope, extracted from experiments. The respective electric current $I(V)$ through the PSV is then

$$I(V) = \frac{V}{R_{\rm PSV}(V)}. \tag{22}$$

Equation (21) illustrates how to include the actual experimental data. The resistance $R_{L(H)}$ in the bias voltage intervals $V_{\rm Ll} < V < V_{\rm Lr}$ and $V_{\rm Hl} < V < V_{\rm Hr}$ is approximated by tailoring the respective piecewise cubical parabolas describing the bias-voltage dependence:

$$R_{L(H)}(V) = R^{(0)}_{L(H)} + \alpha_{L(H)}V + \beta_{L(H)}V^2 + \gamma_{L(H)}V^3. \tag{23}$$

The coefficients $\alpha_{L(H)}$, $\beta_{L(H)}$, and $\gamma_{L(H)}$ are obtained by fitting the experimental curve shown in Fig. 4(b). The respective model form of $R_{\rm PSV}(V)$ is shown in Fig. 6. Along with $R_{\rm PSV}$, whose time response to the applied electric bit pulse is stepwise and whose Fourier transform takes the form $R_{\rm PSV}(\omega) \propto (1/2)[\delta(\omega) - i/(\pi\omega)]$, one also introduces an effective nonlinear inductance $L_{\rm PSV}$ by

$$L_{\rm PSV}(V, I)I_{\rm PSV} = \int V_{\rm PSV}(t)dt. \tag{24}$$

The respective "reactive resistance" $R_{\rm PSV}$ for a harmonic signal takes the form $R^{(L)}_{\rm PSV} = i\omega L_{\rm PSV}$. One estimates that $L_{\rm PSV} = 1.6 \times 10^{-3}$ μH for $\omega = 2\pi f = 2\pi \times 0.5$ GHz. The time dependence of the PSV switching probability is mimicked by introducing a nonlinear inductance connected in series with the PSV. At relatively low $\omega < 10$ GHz, $I_{\rm PSV}$ is large enough to ensure reliable PSV switching. In contrast, as ω increases above approximately 10 GHz, the electric current $I_{\rm PSV}$ through the PSV is diminished due to the $i\omega L_{\rm PSV}$ increase, and hence the switching is suppressed. If there are also resistive and capacitance branches of the three-branch EDD, then $I_{\rm PSV} = I - I_R - I_C$. The simplest EDD in this model is introduced with use of

$$I_i = \frac{1}{L_{\rm PSV}(V_i, I)} \int V_i(t)dt, \tag{25}$$

where $L_{\rm PSV}(V_i, I)$ depends on the ith branch voltage V_i and the total current I.

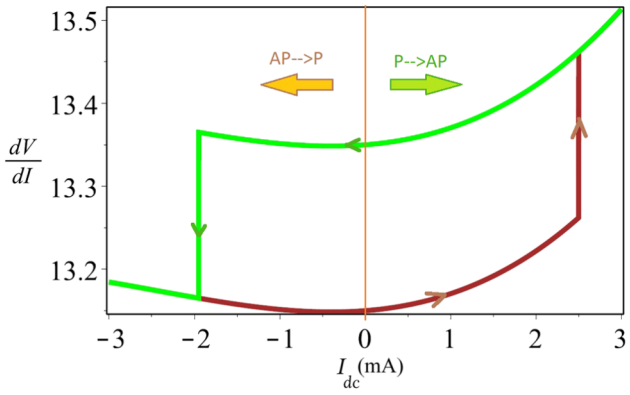

FIG. 6. Model form of the OST switching diagram used in the EDD. The PSV differential resistance $dV/dI_{\rm dc}$ (Ω) switches stepwise at $I_{\rm dc} = -2$ mA and $I_{\rm dc} = 2.4$ mA. The area of the switching loop depends on the pulse duration, whose optimal value is approximately 5 ns. AP, antiparallel; P, parallel.

The simplest EDD form of the PSV nonlinear differential resistance $R_{\rm PSV}$ versus the switching current $I_{\rm dc}$ and the pulse duration $\tau_{\rm sw}$ is analytically approximated by

$$R_{\rm OST} = R_P + \frac{1}{2}R_{\rm sw}\tanh\left(\frac{I_{\rm dc}-I_h}{I_{\rm wd}}\right) \times\left[1+\tanh\left(\frac{\tau-\tau_{\rm sw}}{T_{\rm wd}}\right)\right], \quad (26)$$

where I_h, R_P, $R_{\rm sw}$, $I_{\rm wd}$, $\tau_{\rm sw}$, and $T_{\rm wd}$ are the PSV switching parameters, which are obtained either from the experimental data [15–18] or from the results of the PSV microscopic modeling [41,42]. The PSV switching event ($0 \rightarrow 1$) happens when the energy supplied by the external power source exceeds a certain threshold. In particular, such a threshold is evident from the experimental data [15–18]. In the external field $H = 49$ mT, for the parallel-to-antiparallel transition (i.e., $0 \rightarrow 1$), the switching event occurs when the switching time exceeds 0.6 ns and the bias current exceeds $I_{\rm dc} \geq 2.7$ mA. The antiparallel-to-parallel transition (i.e., $1 \rightarrow 0$) occurs at $I_{\rm dc} \leq -1.9$ mA. The PSV EDD is represented by respective subcircuit elements defined by Eqs. (20)–(26).

VI. THE PSV-SFT MEMORY CELL

In this work we elaborate the forth $0 \rightarrow 1$ and back $1 \rightarrow 0$ switching processes of the two-terminal PSV characterized by two distinct magnitudes R_L and R_H of their resistance [15–18], comprising the two logical states "0" and "1," respectively. We developed a model describing the switching dynamics of the PSV, shown in Fig. 4. The PSV switching probability is characterized by a certain critical magnitude of the spin-polarized electron energy W_c transported across the device in the course of the orthogonal-spin-transfer process. Typical characteristic energies of the two devices, the PSV and the SFT, differ by a few orders of magnitude: for the PSV, the switching energy is $W_{\rm cr}^{\rm PSV} \sim 10^{-14}$–$10^{-16}$ J, while for the SFT, the respective Josephson energy is $W_{\rm cr}^{\rm SFT} \sim 10^{-19}$ J. The polarization degree of the electron subsystem in the PSV determines the magnitudes of the minimum R_L and maximum R_H resistance of the OST valve. The model depends on the basic physical characteristics of the orthogonal spin transfer and geometry of the PSV. The OST model circuit is complemented by the SFT circuit shown in Figs. 12 and 13, whose switching dynamics is illustrated in Fig. 5 by the respective transient-simulation diagrams. To induce PSV switching between the two logical states [Eq. (20)], we exploit suppression of the critical supercurrent $I_c(I_i)$ due to the quasiparticle injection determined by the injector current I_i, as illustrated by Fig. 13 (Right), where we show the critical supercurrent $I_{\rm ca}$ and gain $\delta I_c/\delta I_i$ of the *S*-*I*-*S* acceptor versus the *S*-F_1-*I*-F_2-*S*-injector current I_i. The physical mechanism of the switching event is that the word pulses applied to the SF_1IF_2S subjunction cause injection of nonequilibrium quasiparticles into the *S*-*I*-*S* acceptor, thereby changing its critical supercurrent $I_{\rm ca}$, as determined by the $I_c(I_i)$ plot in Fig. 13 (right). This brings the *S*-*I*-*S* into the finite-voltage state, which also initializes change of the PSV resistance $R_{\rm PSV}$, provided that simultaneously a bit pulse is applied to the PSV. Otherwise, when the word and bit pulses do not coincide with each other, the state of the PSV remains unchanged.

The information obtained was used to develop the schematics of the PSV-SFT MC shown in Fig. 1, whose electronic circuit is shown in Fig. 14. The test circuit, involving dc simulation, parameter sweep, ac simulation, and transient simulation, allows detailed study of the switching dynamics of the single PSV-SFT memory cell. The PSV is inserted into the Wheatstone bridge, allowing determination of the current logical state, which is either "0" or "1." The basic functionality of the PSV-SFT memory cell depends on a variety of factors involving not only the fundamental physical processes occurring in the OST and SFT subsystems but also the design and geometry of the electronic circuit. The transient-simulation results are given in Fig. 7. One can analyze the dynamics of the PSV switching, reflecting the process of writing and reading the logical information in the PSV-SFT memory cell. In the circuit in Fig. 14, the word pulse is applied to the SFT base, while the bit pulse biases the emitter-collector line, both governing the read-write logical operations. Such operations involve a writing process by applying positive pulses for the writing and reading "0" $\rightarrow$ "1" and negative pulses are used for the writing and reading "1" $\rightarrow$ "0." From the test results one can infer that the read-write process in the computer memory circuit shown in Fig. 14 is nondestructive and nonvolatile. An important issue is that there is a mismatch between the Josephson and PSV switching energies, which requires the use of high magnitudes of $I_{\rm ca}$, a low shunting capacitance, and a low shunting resistance. A straightforward resolution of this issue is accomplished with use of *S*-*N*-*S* junctions instead of *S*-*I*-*S* junctions. Further increase of the SFT switching power in the SFT geometry is achieved by use of stacks of *S*-*N*-*S* junctions instead of a single *S*-*I*-*S* subjunction.

The efficient performance the single PSV-SFT memory cell shown in Fig. 14 is accomplished with the following parameters: the bit-line and word-line impedances are both $Z = 50\ \Omega$, $R_1 = 1\ \Omega$, $R_2 = 35\ \Omega$, the Wheatstone bridge resistances are $R_3, R_4, R_5 = 5.15\ \Omega$, and the lower and upper resistances of the PSV are $R_L = 5\ \Omega$ and $R_H = 5.3\ \Omega$, respectively. Flawless operation of the PSV-SFT memory cell requires the use of superconducting junctions with a high Josephson energy and low resistance, assuming that *S*-*N*-*S* junctions must be used. This implies a high magnitude of the acceptor's critical current $I_{\rm ca} = 0.32$ A. Figure 7 shows the transient-simulation results for the PSV-SFT cell depicted in Fig. 14. The switching process

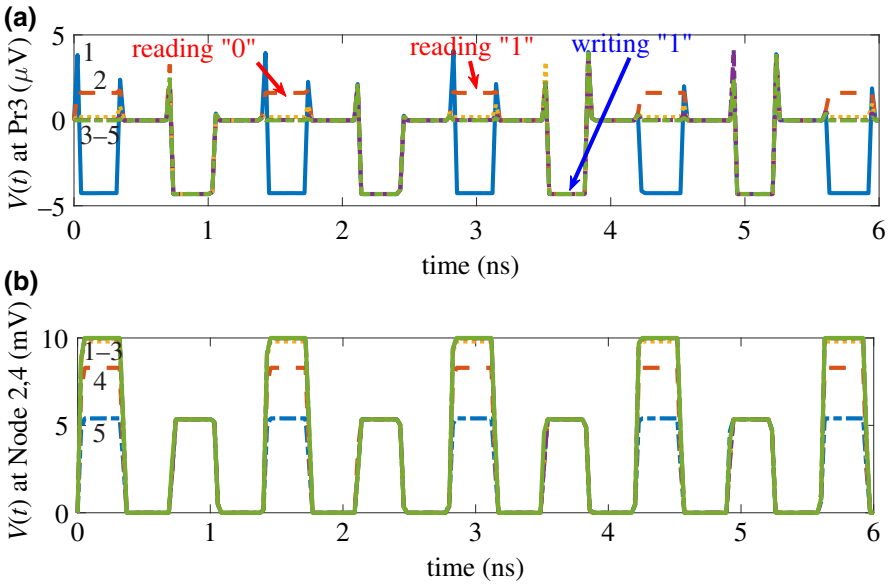

FIG. 7. Transient-simulation results for the PSV-SFT cell shown in Fig. 14. (a) Diagram for *V(t)* at Pr3 showing switching between the positive and negative signals during the read and write "0" → "1" processes. (b) The bit-line-pulse magnitudes [*V(t)* at node 2 and *V(t)* at node 4] are positive. A positive-negative signal of the odd pulses corresponds to reading "0-1," while a positive-negative signal of the even pulses corresponds to writing "0-1," provided the preceding state of the PSV is "0." To write "0-1" provided the preceding state of the PSV is "1," one uses negative bit-line pulses [not shown in (b)]. Curves 1–5 correspond to voltage-pulse amplitudes $U_{in} = 30\ \mu$V, 273 μV, 515 μV, 5 mV, and 10 mV, respectively, at the source V1.

between the positive and negative signals during the read and write "0" → "1" processes is presented in Fig. 7(a) for *V(t)* at probe Pr3, provided that the bit line pulse magnitudes [*V(t)* measured at Node 2 and Node 4] are positive. A positive-negative signals of the odd pulses is related to reading "0-1," while a positive-negative signal of the even pulses corresponds to writing "0-1," provided the preceding state of the PSV is "0." To exercise the process of writing "0-1" provided the preceding state of the PSV is "1," one should apply negative bit-line pulses [Fig. 7(b)].

To characterize the memory cell further, we compute the *S*-parameter diagram used to define the signal-wave response of a multiport electrical element at a given frequency. Here, the *S*-parameter simulation acts as a small-signal ac simulation. It is used to characterize the passive rf component and find the small-signal characteristics of the memory cell at a specific bias. All nonlinear components are linearized and the linear circuit that results is analyzed as a multiport device. Each port is excited in sequence, a linear small-signal simulation is performed, and the response is measured at all ports in the circuit. That response is then converted into *S*-parameter data, which are in turn sent to the dataset. Respective *S*-parameter-simulation diagrams for the circuit in Fig. 14 are shown in Fig. 8.

VII. COMPUTER MEMORY CIRCUIT

In the next step, the elaborated models of the PSV, SFT, and MC are integrated into larger and more-complex superconducting computer memory circuits. In particular, we model the switching dynamics of the computer memory on the basis of OST involving PSVs and multilayered SFTs comprising 12 (see the computer memory circuit in Fig. 15) and 30 memory-cell elements (not shown). The aim is to understand the basic criterion and establish requirements determining the stability of work and optimal switching parameters of the PSV-SFT-based computer memory. Simulation results for the memory comprising 12 elements are presented in Fig. 8 as switching diagrams $V(t)$. The readout–writing voltage signals $V_{Pr1}(t)$–$V_{Pr9}(t)$ are measured by probes Pr1–Pr9 attached to the individual PSV-SFT cells as shown in Fig. 15. The schematic of a single PSV-SFT memory cell (indicated by the purple ellipses in Fig. 15) is explained in Fig. 14. Furthermore, such a schematic is also evident from Fig. 9, where we show the respective *S*-parameter-simulation circuit and the respective simulation results. Details of the switching dynamics, in the course of writing and reading the logical information in the MC-based computer memory, critically depend on the circuit parameters that are established on the basis of the present simulations. In the circuit shown in Fig. 15 (see also Fig. 14), the word-line electric signal pulses are applied to the SFT base of the cell, while the bit-line pulses are applied to the emitter-collector line, both governing the read-write operations in the PSV-SFT computer memory circuit.

The memory-circuit operations involve a reading-writing process by applying positive pulses for the writing and reading "0" → "1" and negative pulses for the writing and reading "1"→"0." From the simulation results shown in Fig. 7 it is evident that the read-write process in the memory circuit is nondestructive and nonvolatile. The transient-analysis description of the PSV-SFT computer-memory switching dynamics, although cumbersome, allows the basic properties the PSV-SFT memory circuit to be determined.

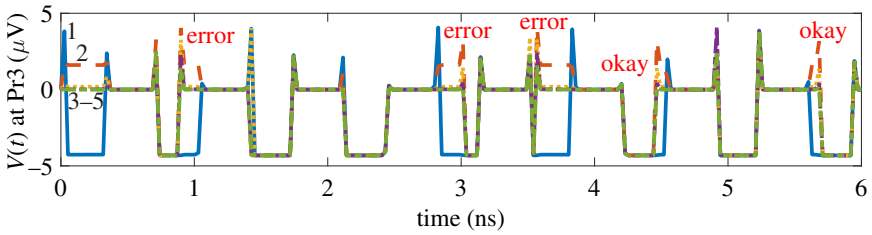

FIG. 8. Example of the transient simulation the OST-SFT memory circuit, showing errors in the readout–writing time-dependent voltage signal *V(t)* at Pr from the memory cell Pr3 presented in Fig. 15. Curves 1–5 correspond to voltage-pulse amplitudes $U_{in} = 15\ \mu$V, 260 μV, 715 μV, 5 mV, and 10 mV, respectively, which are the same for the word lines V1 and V3–V13. The signals from other cells Pr1, Pr2, Pr4-Pr13 show similar behavior.

VIII. READ-WRITE ERRORS

The origin of errors in the PSV-SFT computer memory in the course of reading-writing the logical information is examined as follows. We use CAD of the experimental PSV and SFT elements to study the mechanisms of reading-writing errors in the PSV-SFT memory. The errors are intentionally generated by our introducing additional elements and/or by altering parameters of the circuit. Particular model parameters depend on the MC geometry and are devised with use of basic physical principles of SFT Josephson transistors and orthogonal-spin-transfer pseudo-spin-valves. The MC memory model is built by our integrating the previously elaborated models of the pseudo-spin-valves and the multilayered SFTs, as reported earlier. In this work, the sources of errors ate studied in

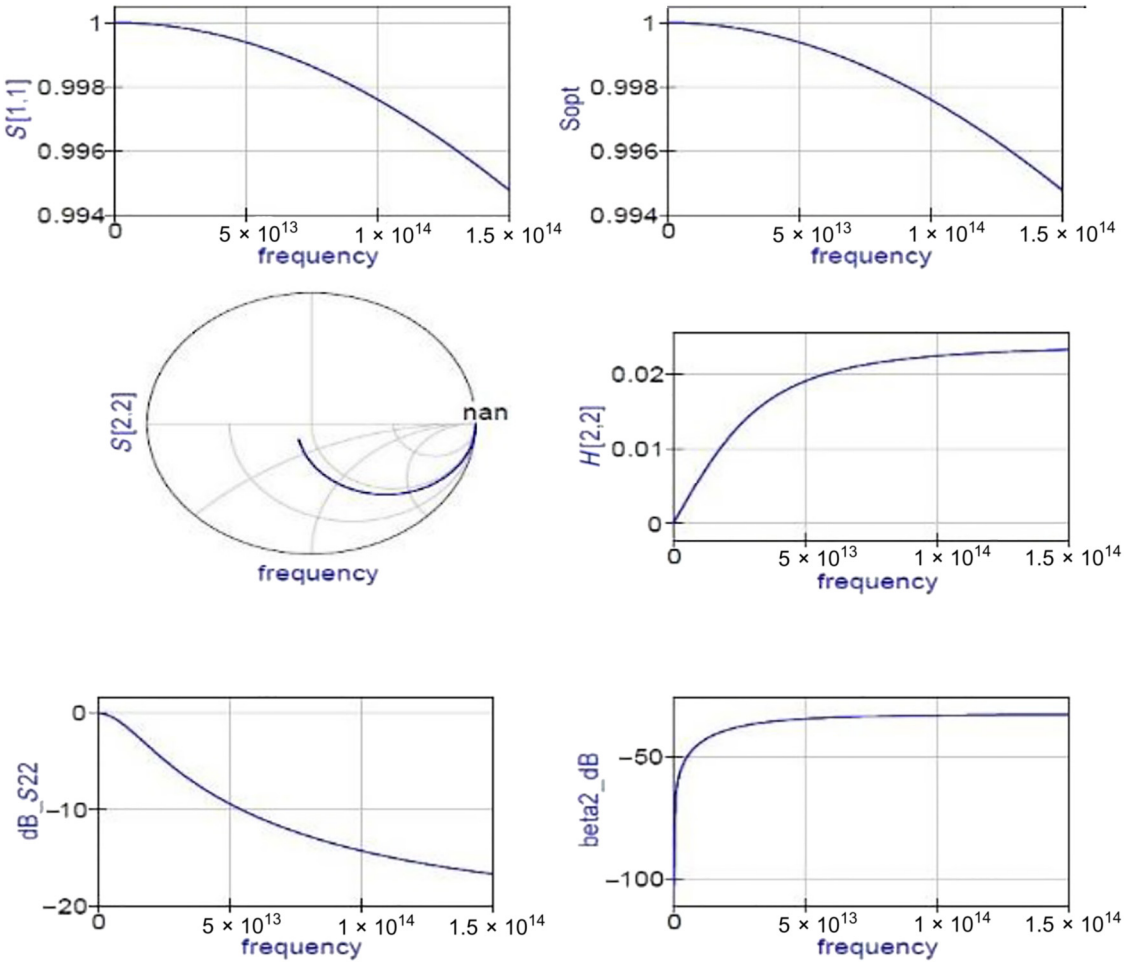

FIG. 9. *S*-parameter-simulation results for the memory cell shown in Fig. 15.

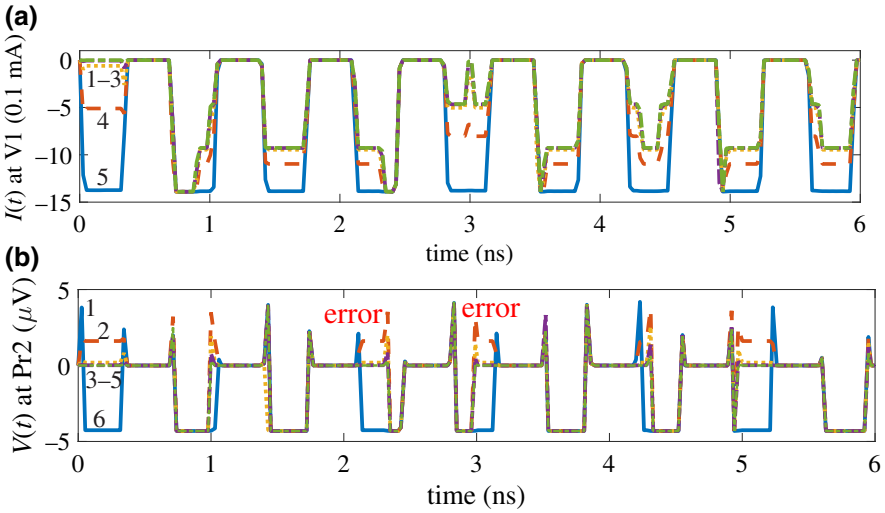

FIG. 10. Transient-analysis diagrams reflecting the time-dependent electric signals. V2 is the electric current at the MC2 emitter (a), while *V(t)* at Pr2 is the voltage measured by probe Pr2 (b). To initialize errors, we set the word-pulse period as distinct for different memory cells in the same circuit. Curves 1–6 correspond to voltage pulse amplitudes $U_{\rm in} = 20$ μV, 252 μV, 415 μV, 5 mV, 10 mV and 12 mV respectively which are the same for word lines V1, V3, and V4.

MC-based circuits made of 12 MC elements (Fig. 15) and 30 MC elements (not shown). The goal is to find criteria and requirements to prevent errors in the course of MC-based memory operation. This would increase the stability of work and facilitate setting the optimal switching parameters of the hybrid computer memory.

The quantitative measure of performance and functionality of the memory circuit is the bit-error rate (BER). Several factors determine the BER. Besides noise, the errors also arise from the punch-through effect, cross talk, parasitic effects, and Josephson plasma oscillations, especially at higher frequencies. A schematic of the PSV-SFT memory, whose individual MC elements are indicated by the purple ellipses in Fig. 15 (for simplicity we show just three MC elements), is given in Fig. 14. To mimic the parasitic effects affecting the performance of the memory circuit, we add capacitances C1 and C2 and inductances L1–L3, whose values are changed for different simulation runs. In Fig. 10 we present the simulation results for the computer memory in the form of transient-analysis switching diagrams $V_{\rm Pr2}(t)$. The readout–writing voltage signal $V_{\rm Pr2}(t)$ shown in Fig. 10 is measured by probe Pr2 attached to the individual MC element as shown in Fig. 15.

The dynamics of the reading-writing errors occurring during the OST-SFT-cell switching depends on the circuit parameters that are obtained from the present simulations. The word pulses are applied to the SFT injector serving as the base of the Josephson transistor. For proper MC switching, they must coincide with the bit pulses acting in the emitter-collector lines; thereby both type of pulses, when acting simultaneously, govern the read-write operations in the OST-SFT computer memory circuit. With the intent to initialize errors, we set the word-pulse period as being distinct for different memory cells in the same circuit. The reading-writing operations are performed with positive pulses for writing-reading "0" → "1" and negative electric pulses are used for writing-reading "1" → "0." One can see that the read-write process in the memory circuit is nondestructive and nonvolatile, as confirmed by the simulation results shown in Fig. 10.

The available experimental data in conjunction with the theoretical modeling suggest that the readout–writing processes depend on the value of the spin-polarized electron energy W_c transferred through the OST pseudo-spin-valve when the bit pulse is applied. The magnitude of the BER also depends on the relationship between the critical energies for the OST device $W_{\rm cr}^{\rm OST}$ and the respective energies of the SFT device $W_{\rm cr}^{\rm SFT}$. Thus, to reduce the BER, the ratio $W_{\rm cr}^{\rm SFT}/W_{\rm cr}^{\rm OST} \sim 10^{-5}$–$10^{-3}$ must be chosen appropriately. Along with the MC configuration, the BER of the PSV-SFT computer memory depends on the circuit's impedance, which also affects its switching rate. In turn, the magnitude of the impedance depends on the geometry and physical parameters of the SFT Josephson transistors

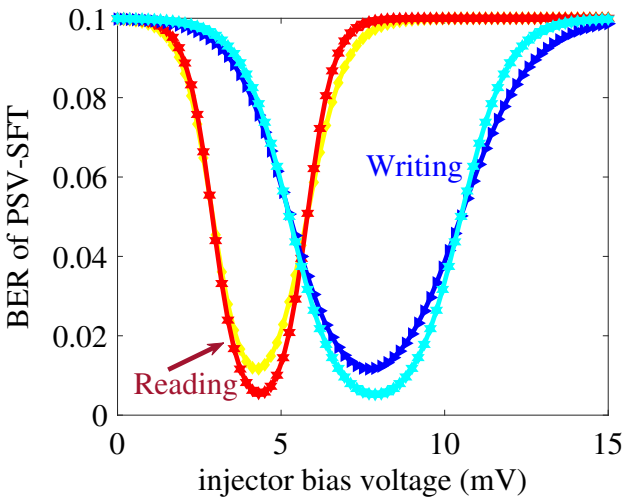

FIG. 11. The BER of the memory circuit for reading-writing at $\nu = 1$ GHz (blue, red) and $\nu = 1.5$ GHz (cyan, yellow) obtained in the course of the multiple simulation cycles with different initial conditions, which resulted in a variety of error events.

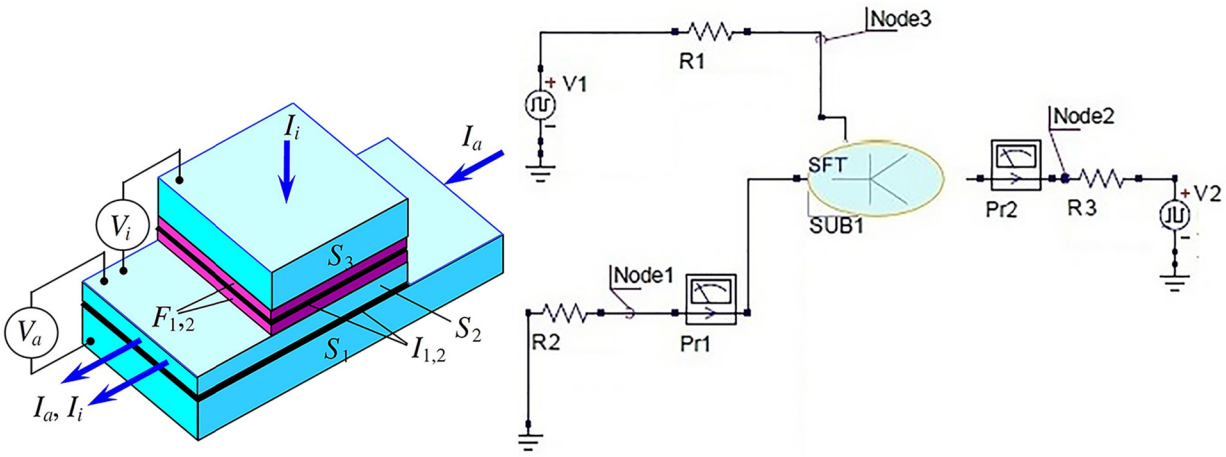

FIG. 12. Test circuit of the SFT serving as a Josephson transistor [8–11], whose geometry is shown on the left (reproduced from Ref. [14] with permission from the American Physical Society). We perform dc simulations, Harmonic balance simulations, ac simulations, and transient simulations for the parameters given in text. Here SUB1 denotes the subcircuit describing the superconducting-ferromagnet transistor (SFT).

and how they couples with the multilayered ferromagnetic PSV. In the memory circuit shown in Fig. 15, the bit errors originate from the circuit dynamics and noise. The OST-SFT memory circuits are affected by two different noise sources, the JJ noise of the SFT and the noise generated in the normal-state elements. The latter noise is the so-called Johnson noise (JN), whose JN-current rms value is $i_{\rm rms} = \sqrt{4k_BTv/R}$, where k_B is the Boltzmann constant and v is the bandwidth. The JN current consists of the noise current generated inside the MC memory circuit at 4.2 K and the room-temperature noise penetrating from the outside environment along the cables. The noise in a single JJ was examined in Ref. [47], where the authors found that the JJ emits shot noise when the bias voltage V exceeds 1 mV, while Johnson noise is generated when $V < 1$ mV. We calculated the BER of the MC memory circuit in the course of the mixed-signal simulations. The noise is included by our adding the respective random sources of current. Furthermore, we consider that the critical current is spread as $I_c = I_c^{(0)} + \delta I_c^{(n)}$, where the randomness $\delta I_c^{(n)}$ depends on the MC index n and is relatively small, $\max|\delta I_c^{(n)}/I_c^{(0)}| < 0.1$. In the simulations, we also include the randomness of the OSR resistivity difference $\delta R_{\rm PS}^{(n)} = R_{\rm max}^{(n)} - R_{\rm min}^{(n)}$, assuming that $\max|\delta R_{\rm PS}^{(n)}/R_{\rm max}^{(0)}| < 0.1$. Multiple simulation cycles with different initial conditions resulted in a variety of error events. This allowed us to find the dependence of

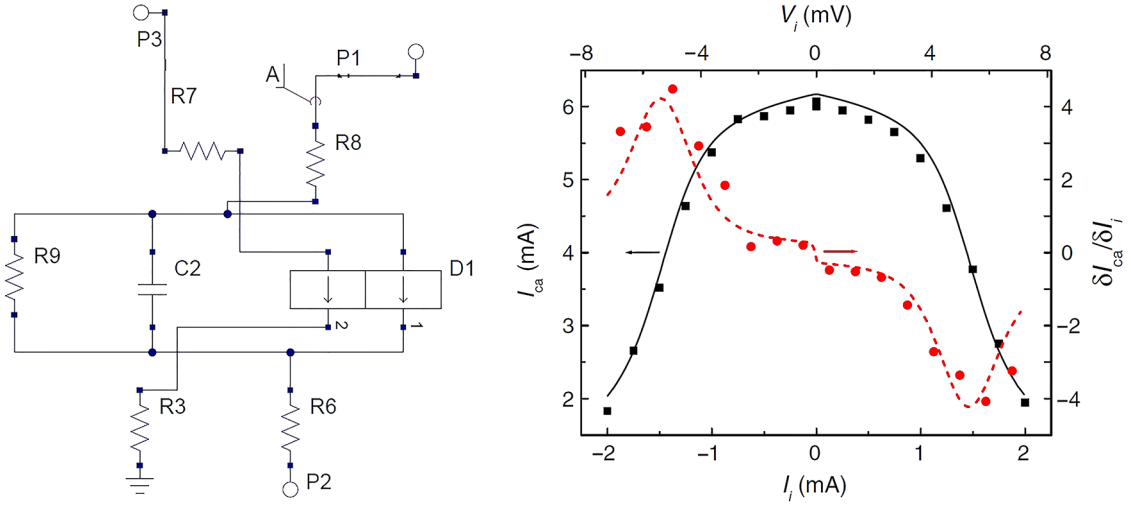

FIG. 13. The left panel shows the subcircuit of SFT-EDD D1, where R9 and C2 are shunting resistance and capacitance, respectively. The SFT switching dynamics critically depends on the shunting resistance R9 and capacitance C2. The right panel shows experimental data (points) and theoretical results (solid and dashed curves) used to formulate the EDD; see Eqs. (1) and (25). Critical supercurrent $I_{\rm ca}$ (black) and gain $\delta I_{\rm ca}/\delta I_i$ (red) of the *S-I-S* acceptor [14] versus the SF_1IF_2S-injector current I_i. The right panel is reproduced from Ref. [14] with permission from the American Physical Society.

the BER on the injector bias voltage, corresponding to the magnitude of word pulses on the SFT base as presented in Fig. 11. The results obtained suggest that the BER is optimized at a certain injector bias voltage V_i. This is evident from Fig. 11, where we show the BER as function of as a function of the injector bias voltage. One can see that the BER is sharply reduced from 0.1 to 0.01 for reading at $V_i \sim 4$ mV and for writing at $V_i \sim 8$ mV. If the injector bias voltage is insufficient, omission errors arise, while insertion errors arise if the injector bias voltage is excessive. Since Johnson noise prevails, the BER dependence resembles the classical error function, which agrees with the conventional BER theory.

IX. CONCLUSIONS

The simulation results suggest that the hybrid computer memory is characterized by ultrafast switching (subnanosecond) and low energy consumption per operation (sub-100 fJ) due to large initial spin-transfer torque from the perpendicular polarizer. Our model, describing superconducting computer memory circuits, also allows the study of the effects of noise, the punch-through effect, cross talk, parasitic effects, etc. An advantage of hybrid PSV-SFT devices, serving as elements of superconducting computing circuits, is that they are built from magnetic and nonmagnetic transition metals and therefore have low impedances (1–30 Ω). Therefore, PSV-SFT-based computer memory shows promise for future superconducting computers.

The main results of this work are summarized as follows: (i) We create small agile phenomenological models that adequately capture the physics of a SFT and a pseudo-spin-valve making the design of large superconducting circuits possible. In particular we develop the circuit model of the Josephson transistor. (ii) We prove that use of SFT and pseudo-spin-valve devices adds many remarkable capabilities to superconducting-electronics design. In particular, we prove that the three-terminal Josephson transistor can function as a key element of large circuits and can control other devices in the circuit. This ensures functionality and flawless performance of computer memory based on the two-terminal pseudo-spin-valve. As an example, we design the circuit model demonstrating the writing-reading operations in the hybrid PSV-SFT computer MC and in larger memory circuits. The model helps optimize the performance and functionality of the memory circuit characterized by the BER. (iii) We examine the criteria and requirements determining the stability of work and switching parameters of PSV-SFT-based computer memory. The circuits show a remarkably low error rate and good tolerance in large-circuit simulations.

APPENDIX

1. The test circuit of the SFT

Figure 12 shows the geometry (left) and the electrical circuit diagram (right) of the three-terminal SFT. Mathematical details of the model are given in Sec. III.

2. Respective SFT-EDD subcircuit

The respective SFT-EDD subcircuit is depicted in Fig. 13. In the model by applying the simplified Eq. (1)

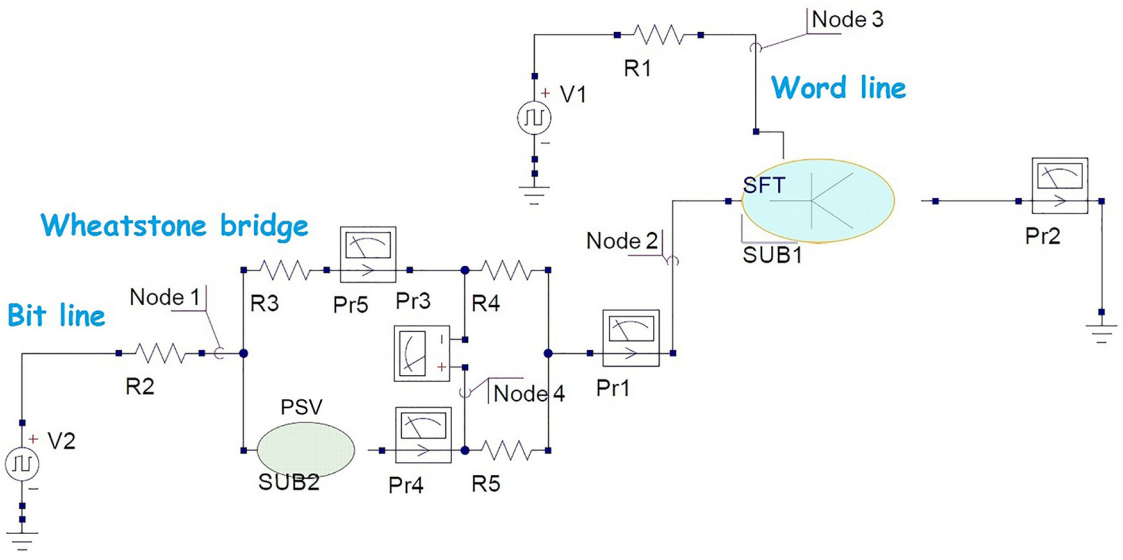

FIG. 14. The PSV-SFT computer memory cell devised to study the switching dynamics. Relevant parameters are indicated near the respective circuit element. The PSV is inserted into the Wheatstone bridge, allowing determination of its current logical state. Here SUB2 denotes the subcircuit describing the pseudospin valve (PSV).

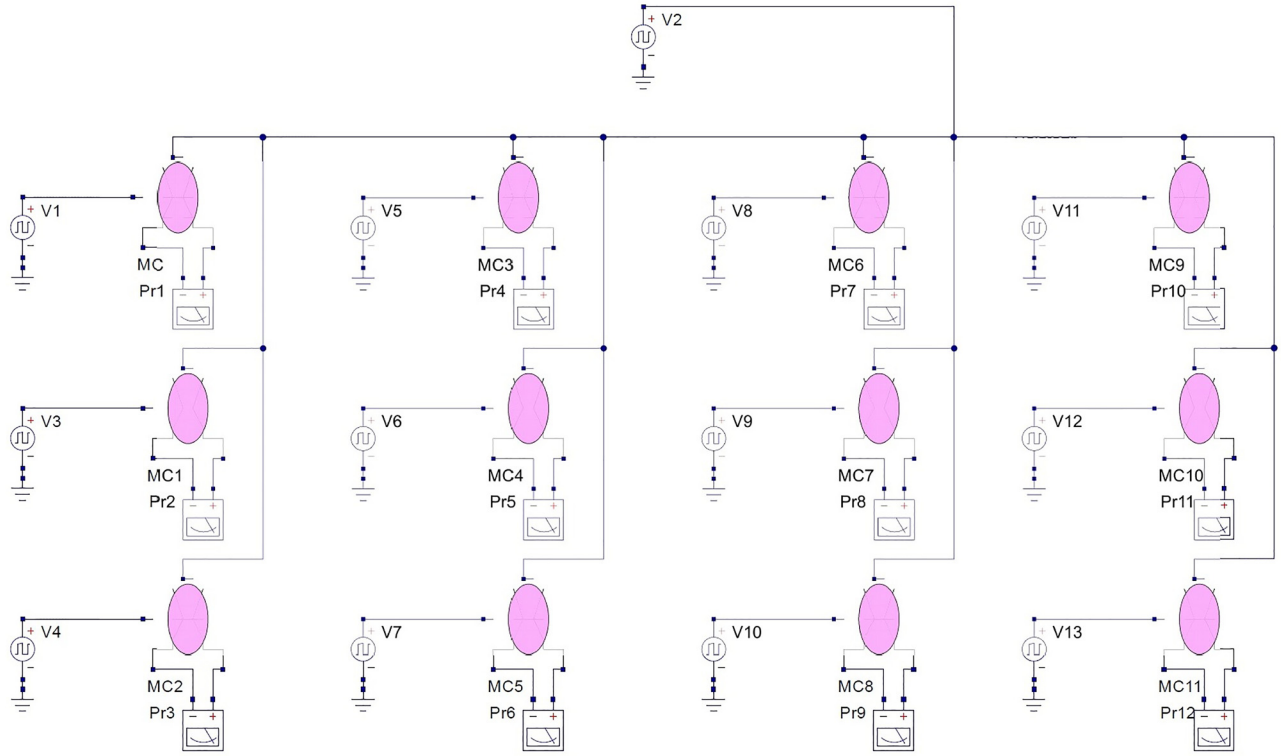

FIG. 15. The PSV-SFT computer memory circuit comprising 12 cells. The reading-writing operations are conducted using the multilayered SFTs. To simulate errors, the bit line is common for all 12 cells, while the word lines are individual for each of the cells. The ellipses (SUB) denote the subcircuits describing the respective memory cells.

to the SFT, we assume that I_c depends on the *S-F-I-F-S*-injector bias current I_i as shown on the right in Fig. 13. Detailed circuit parameters are given at the end of Sec. III.

3. Electronic circuit of the PSV-SFT memory cell

We develop a schematic of the PSV-SFT MC (Fig. 14). Here the SFT serves to accomplish switching between the logical states of the two-terminal PSV. The two devices, the PSV and the SFT, are combined to form a hybrid electronic circuit comprising the computer memory cell, whose logical states are triggered by SFT introduced and studied in Refs. [8–11].

Detailed circuit parameters for modeling the single PSV-SFT memory cell shown in Fig. 14 are given at the end of Sec. VI.

4. The PSV-SFT computer memory circuit comprising 12 cells

The functional performance of the large computer memory circuit shown in Fig. 15 based on SFT-controlled pseudo-spin-valves is studied by the simulations described

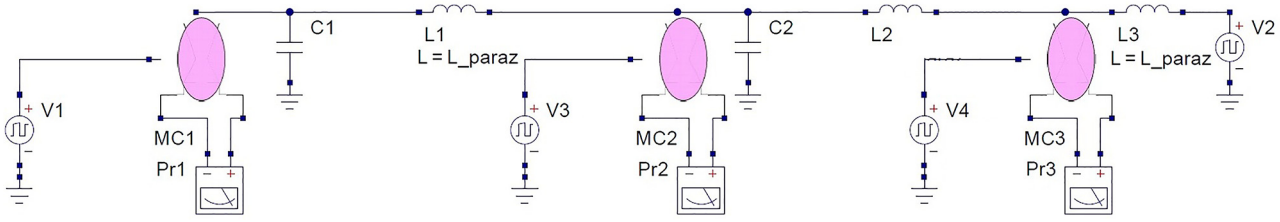

FIG. 16. The PSV-SFT computer memory circuit comprising three memory-cell elements (MC1–MC3) based on OST controlled by the three-terminal Josephson SFT transistor. The structure of the memory cells and the respective subcircuit schematics are shown in Fig. 14 and explained in main text. The capacitances C1, C2 and inductances L1–L3, whose values are changed for different simulation runs, mimic the parasitic effects, L_paraz denotes the parasitic inductance. Reading-writing the logical information is performed by applying word pulses to the SFT base and bit pulses to the emitter-collector.

in Sec. VII, where details of the circuit design are also given. The individual memory-circuit elements are indicated by the purple ellipses.

Using the approach developed, we integrate the elaborated models of the PSV, SFT, and MC into larger and more-complex circuits comprising SFT and PSV elements.

5. PSV-SFT memory circuit comprising three memory-cell elements

Important insight into the stability and tolerance of computer memory circuits is obtained by our mimicking the parasitic effects affecting the performance of the memory circuit. An example of such a test circuit comprising PSV-SFT memory is given in Fig. 16, where for simplicity we show just three MC elements. Detailed circuit parameters and simulation details are given in the main text.

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