Radio-Frequency Methods for Majorana-Based Quantum Devices: Fast Charge Sensing and Phase-Diagram Mapping

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Radio-frequency (rf) reflectometry is implemented in hybrid semiconductor-superconductor nanowire systems designed to probe Majorana zero modes. Two approaches are presented. In the first, hybrid nanowire-based devices are part of a resonant circuit, allowing conductance to be measured as a function of several gate voltages approximately 40 times faster than using conventional low-frequency lock-in methods. In the second, nanowire devices are capacitively coupled to a nearby rf single-electron transistor made from a separate nanowire, allowing rf detection of charge, including charge-only measurement of the crossover from $2e$ interisland charge transitions at zero magnetic field to $1e$ transitions at axial magnetic fields above 0.6 T, where a topological state is expected. Single-electron sensing yields a signal-to-noise ratio exceeding 3 and a visibility of 99.8% for a measurement time of 1 μs.

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I. INTRODUCTION

Solid-state quantum computation schemes that involve repeated measurement and feedback, including topological schemes [1–4] with potentially long coherence times [5,6], nonetheless require fast read-out of charge or current in order to operate on reasonable time scales [7]. For topological qubits based on Majorana modes in nanowires (NWs) with proximity-induced superconductivity, quasiparticle poisoning of Majorana modes constrains read-out times to microseconds or faster [12], as has already been demonstrated for superconducting [13–16] and spin qubits [17–20].

Here, we report the realization of radio-frequency (rf) reflectometry in various configurations of InAs nanowires (NWs) with epitaxial Al, fabricated to form single or coupled Majorana islands, with and without proximal NW charge sensors. The device geometries are inspired by recent theoretical proposals for demonstrating elementary topological qubit operations in these systems [1–4]. Two approaches to fast measurements are investigated in detail. In the first, a resonator made from a cryogenic inductor and capacitor is coupled directly to the leads of the device [21–23], providing a conductance measurement similar to what is obtained with a low-frequency (LF) lock-in amplifier, though considerably faster. In the second, a similar resonator is capacitively coupled to a proximal NW charge sensor configured for both LF and rf charge read-out. The overall charge sensitivity is investigated as a function of the measurement time and is found to yield a signal-to-noise ratio (SNR) for single-charge detection exceeding 3 and a visibility of 99.8% for an integration time of 1 μs, with correspondingly higher values for longer integration times. Proximal NW charge sensors are found to be compatible with magnetic fields exceeding 1 T, the range needed to reach the topological regime [8–11]. All measurements are carried out in a dilution refrigerator (Oxford Instruments Triton 400) with a base temperature of approximately 20 mK, equipped with a 6-1-1 T vector magnet.

II. EXPERIMENTAL SETUP

The reflectometry signal is optimized by matching the circuit impedance Z, including the device resistance R_{dev}, to the characteristic impedance of the transmission line, $Z_0 = 50\ \Omega$. Near matching, the reflection coefficient of the

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resonant circuit, $(Z - Z_0)/(Z + Z_0)$, is sensitive to small changes in $R_{\rm dev}$ [24,25]. To enable multiple simultaneous measurements, four rf resonant circuits with different discrete inductances in the range $L = 1.2$–$4.7\ \mu$H are coupled to a single-directional coupler via a coupling capacitor, C. One such resonant circuit is depicted in Fig. 1(a). It consists of a ceramic-core chip inductor [26], a parasitic capacitance, C_P, from bond wires and on-chip metal electrodes, and the device, with $R_{\rm dev}$ tuned by the gate voltages. The parasitic capacitance is found to be unchanged over several cool-downs.

LF lock-in measurements of differential conductance $g = dI/dV|_{V_{\rm bias}}$ of either the device or the sensor are carried out in a two-wire voltage-bias configuration using a transimpedance (current-to-voltage) amplifier [27] connected to the drain of the device, providing voltage input to a lock-in amplifier (Stanford Research SR830). The voltage bias consists of a dc component, $V_{\rm bias}$, and a LF component in the range of 4–10 μV at frequencies below 200 Hz.

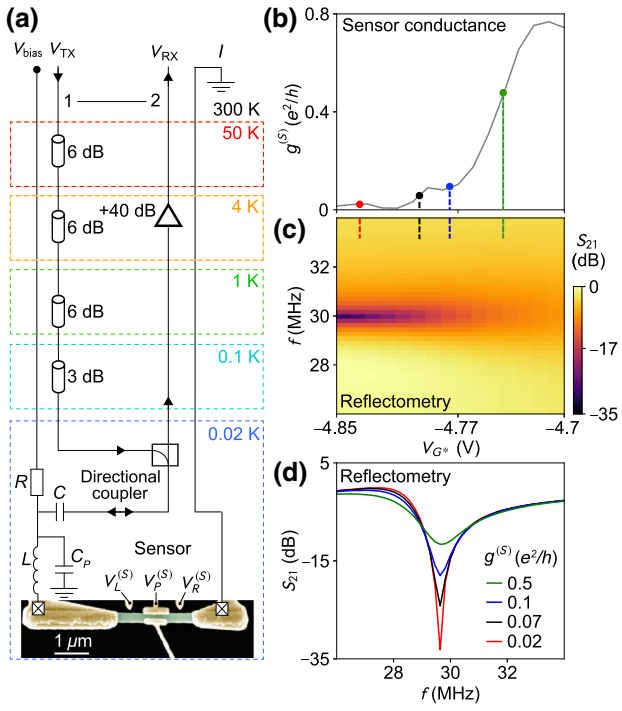

FIG. 1. The rf charge-sensing setup. (a) A circuit diagram of a nanowire (sensor) embedded in a resonant circuit allowing conductance [by measuring current $I(V_{\rm bias})$] or reflectometry measurement (by measuring reflected signal $V_{\rm RX}$), respectively (see the main text). (b) The sensor conductance, $g^{(S)}$, as a function of the sensor gate voltage, $V_{G^*} = V_L^{(S)} = V_P^{(S)} = V_R^{(S)}$. (c) The scattering parameter, S_{21}, as a function of the carrier frequency f, and V_{G^*} acquired simultaneously with (b). $S_{21}(f)$ develops a dip at $f_{\rm res} \sim 30$ MHz, indicating that the matching condition of the resonator is approached toward low sensor conductance. (d) Vertical cuts of (c) for the gate voltages indicated in (b). The on-resonance reflectometry signal acts as an alternative measure of $g^{(S)}$.

Reflectometry measurements of either the device or the sensor are performed as follows. A rf carrier at frequency f with amplitude $V_{\rm TX}$ is applied to the source lead following a series of attenuators at various temperature stages [Fig. 1(a)], giving a total of 21 dB of attenuation, with an additional 15 dB of attenuation from the directional coupler, mounted below the mixing chamber plate. After reflection from the device, the signal passes back through the directional coupler into a cryogenic amplifier (Caltech CITLF3; noise temperature $T_n = 4$ K from 10 MHz to 2 GHz) with +40 dB of gain. The output signal, $V_{\rm RX}$, is then detected using one of three methods: (1) using a network analyzer to measure $S_{21} \equiv 20\log(V_{\rm RX}/V_{\rm TX})$ [Fig. 1(c)]; (2) using discrete analog components to demodulate by standard homodyne detection, followed by a fast-sampling oscilloscope (for details, see Appendix B); (3) using a rf lock-in amplifier (Zurich Instruments UHFLI [28]). Each method has its advantages. Method (1) is convenient for quickly determining if a change in device resistance has an effect on the circuit impedance, which shows up as a change in the magnitude of S_{21}. Method (2) provides fast acquisition of phase maps at different gate configurations, particularly if the device is tuned into the regime of small charging energies. For these applications, methods (2) and (3) are comparable. Method (3) has advantages in simultaneously measuring the phase and magnitude of the reflected signal and is used to quantify SNR of the proximal NW sensors and to detect charge occupancy of Majorana islands tuned to low barrier transmission.

Figures 1(b)–1(d) show a comparison of the LF lock-in measurement and the reflectometry measurement, $S_{21}(f)$, of conductance $g^{(S)}$ of a charge sensor as it is pinched off using electrostatic gates. In the reflectometry measurement, V_{RX} varies rapidly near the resonance frequency $f_{\rm res} \sim 30$ MHz, yielding a dip in $S_{21}(f)$ that depends on the common gate voltage. Line cuts of S_{21} at different values of V_{G^*} are shown in Fig. 1(d). The depth of the resonance changes by approximately 21 dB as the sensor conductance, $g^{(S)}$, is decreased from 0.5 e^2/h to 0.02 e^2/h. In this case, an increasing $R_{\rm dev}$ moves the resonator impedance toward matching.

III. CONDUCTANCE: LF LOCK-IN VERSUS RF REFLECTOMETRY

Figure 2(a)shows a hybrid InAs/Al island (device A) defined by Ti/Au gates that wrap around the NW, isolated by HfO_2 dielectric. Al is removed from the NW ends with wet etch, leaving a continuous Al segment, where gates L and R set the boundaries of the island. Gate voltages V_L and V_R control coupling of the island to the leads, while three additional gates tune the chemical potential and density on different parts of the island (see Appendix D). Only

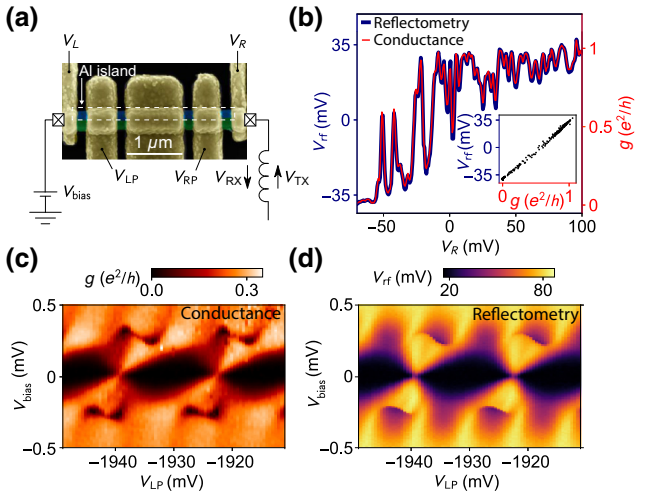

FIG. 2. Conductance via lock-in versus lead reflectometry: device A. (a) A scanning electron micrograph of a top-gated InAs/Al nanowire device with the relevant gates labeled. The dashed white box indicates the Al island. (b) The zero-bias pinch-off characteristic of the right barrier gate, V_R, as measured by conductance (red) and reflectometry (blue). The inset shows a parametric plot of the two traces. The Coulomb-blockade diamonds are measured by conductance (c) and reflectometry (d). In both cases, the dependence on the plunger voltage V_{LP} is $1e$ periodic at high bias and $2e$ periodic at zero bias.

the gate marked V_{LP} in Fig. 2(a) is used, with the others fixed at zero volts. A dc voltage V_{bias} is applied to the left lead, while the right lead is connected to the rf circuit ($L = 2.7\ \mu$H, $f_{\mathrm{res}} \sim 52$ MHz) using method (2), described above. Simultaneous LF and rf measurements of the pinch-off characteristic of the right barrier with the left barrier fixed at $V_L \sim 1$ V are shown in Fig. 2(b). At positive V_R, the right-hand side of the island is open and shows a positive demodulated voltage V_{rf}, while at negative V_R, the right junction is closed and no current can flow through the island. Overall, V_{rf} is found to be proportional to g measured with an LF lock-in, as shown in the inset of Fig. 2(b).

Setting both barriers into the tunneling regime using V_L and V_R creates a Coulomb-blockaded island. A two-dimensional (2D) map of Coulomb diamonds as a function of V_{bias} and the left plunger gate, V_{LP}, is shown in Figs. 2(c) and 2(d). At finite bias, $V_{\mathrm{bias}} \geq 0.2$ mV, above the superconducting gap of Al, conductance oscillations with a period of half the zero-bias period are found, characteristic of a superconducting island. At low bias, transport is via Cooper pairs, yielding $2e$ periodicity; at biases above the superconducting gap, $1e$ transport is available, halving the period.

The similarity of the LF lock-in and rf reflectometry data exhibited in Figs. 2(c) and 2(d) indicates that rf reflectometry yields essentially equivalent results to LF conductance, although with a dramatic reduction of data-acquisition time. For instance, a 2D map of V_L versus V_{LP} consisting of 3000×1500 points (Appendix A) requires roughly 1 h of acquisition time, including data processing. The acquisition of comparable data using LF lock-in methods with a 30 ms integration time would require $1500 \times 3000 \times 30$ ms ~ 38 h to achieve a comparable SNR and resolution.

IV. CHARGE SENSING

The charge sensing of a Majorana island is accomplished by placing a second NW (sensor wire), without a superconducting layer, next to the hybrid-NW Majorana device and capacitively coupling the two NWs with a floating metallic gate [29]. Charge sensing complements conductance and is the basis of parity read-out in several theoretical proposals (e.g., Ref. [1]). The approach is similar to schemes used for spin qubit read-out [30–32]. In the context of topological qubits, one can generalize the idea used in spin qubits known as "spin-to-charge conversion," where a well-isolated quantum variable (spin) is read out projectively by mapping the relevant qubit state onto charge and then detecting charge [19,20]. In a similar way, the parity of a Majorana island grounded via a trivial superconductor, a well-isolated quantum state, can be read out projectively as a charge state if the island is gated into isolation, forming a topological Coulomb island [1], a process that we denote "parity-to-charge conversion."

A. LF charge sensing

A Majorana island formed from a gated segment of InAs/Al that gates L and R encapsulate, with extended leads made from the same wire (device B), is shown in Fig. 3(b).Regions with tunable carrier density and conductance, made by removing the Al shell, are aligned with electrostatic gates deposited in a subsequent lithography step. Local depletion of the charge carriers in these regions (tuned by gates L and R) creates two superconductor-insulator-superconductor tunnel junctions with a semiconductor-superconductor island in between. A T-shaped floating gate couples the superconducting island to the charge sensor NW, which is operated in the Coulomb-blockade regime by depleting its barriers with gate voltages $V_L^{(S)}$ and $V_R^{(S)}$ (for details, see Appendix D).

LF lock-in measurement of conductance through the InAs/Al NW island as a function of V_{bias} and the compensated gate voltage V_P^* is shown in Fig. 3(a). Compensation means that whenever the device plunger voltage V_P is swept, the sensor plunger $V_P^{(S)}$ is also varied to prevent V_P from affecting the sensor charge state via capacitive coupling, allowing the sensor to remain on a single Coulomb peak as V_P^* is swept. Compensation is illustrated in Fig. 3(c), where the green dashed line shows a compensated trajectory through the space of the two plunger voltages.

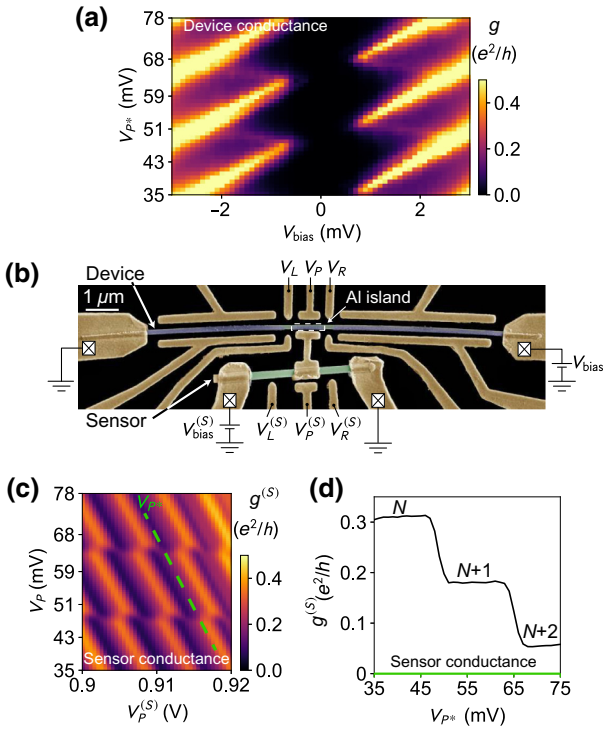

FIG. 3. The charge sensing of a superconducting island using lock-in measurement of a remote charge sensor: device B. (a) Conductance through the InAs/Al nanowire device [blue in (b)] as a function of the bias voltage, $V_{\rm bias}$, and the compensated plunger voltage, V_P^* (for an explanation of compensation, see the main text). (b) A false-color scanning electron micrograph of a device with the relevant gates labeled. A T-shaped Ti/Au floating gate couples the superconducting island (white dashed box) ("Device") to a bare InAs nanowire ("Sensor"). (c) The sensor conductance $g^{(S)}$ at $V_{\rm bias} = 0$, as a function of $V_P^{(S)}$ and V_P. (d) A cut along the green dashed line in (c). Distinct constant-conductance-value plateaus are indicated by the associated electron occupation of the Majorana island.

Coulomb-blockade diamonds are visible in Fig. 3(a). The suppression of conductance for $|V_{\rm bias}| < 0.4$ mV, independent of V_P^*, reflects the presence of a superconducting gap in both leads and is consistent with the gap of Al, assuming that the induced gap $\Delta_I \sim 0.2$ meV is roughly equal in the three NW segments. The charging energy $E_C \sim 0.7$ meV is extracted from the Coulomb diamonds of Fig. 3(a). The large charging energy, $E_C/\Delta_I > 1$, is consistent with suppressed conductance of Cooper pairs at $V_{\rm bias} = 0$ [33–35]. The large E_C results from the small capacitance between the device island and the metal back gate due to thick (500 nm) SiO_2. By comparison, device A has 200 nm of SiO_2, reducing the charging energy to below the induced gap, leading to $2e$ Cooper-pair transport between Coulomb valleys.

The sensor conductance, $g^{(S)}$, at zero dc bias, $V_{\rm bias}^{(S)} = 0$, as a function of the plunger gate voltages $V_P^{(S)}$ and V_P, is shown in Fig. 3(c). Conductance oscillations along the $V_P^{(S)}$ axis indicate that the sensor island is tuned into the Coulomb-blockade regime, whereas discontinuities along V_P reflect charge transitions in the main hybrid device. We emphasize that charge transitions are *not visible* in zero-bias conductance of the device [Fig. 3(a)] but *are visible* as plateaus in sensor conductance $g^{(S)}$ as the device charge changes by 2 between adjacent Coulomb valleys [Figs. 3(c) and 3(d)].

B. RF charge sensing

A double-Majorana-island device (the white dashed boxes indicate the Al islands) motivated by Ref. [1] (device C) is shown in Fig. 4(a).Near the main device, two bare InAs NWs, capacitively coupled to each of the islands via floating gates, serve as independent charge sensors for the two islands. Each sensor is part of an independent rf circuit, with $L_1 = 3.3$ μH ($f_{\rm res} \sim 60$ MHz) and $L_2 = 4.7$ μH ($f_{\rm res} \sim 40$ MHz). The data acquisition uses method (3), described above. Gates V_L, V_M, and V_R are each set to the tunneling regime. Voltages applied to plunger gates LP and RP affect both the carrier density in the semiconductor and the charge offset of each island (see Appendix D). Figure 4(b) shows the charge-sensing signal of a $2e$-$2e$ periodic superconducting double island at $B = 0$, measured using the right charge sensor (S2), with a plane subtracted to remove cross-coupling of the plungers to the three barrier gates, V_L, V_M, and V_R. Periodic $1e$-$1e$ double-island plane-fitted data, measured using the left charge sensor (S1) at finite magnetic field ($B = 0.8$ T) parallel to NW axis, are shown in Fig. 4(c). A hexagonal pattern, characteristic of a double-island device, is readily seen at both zero field and $B = 0.8$ T [Figs. 4(b) and 4(c)]. The magnetic field B evolution of the right $2e$ periodic island into the $1e$ periodic island regime, with the left island tuned into a Coulomb valley, is shown in Fig. 4(d). The data are differentiated along $V_{\rm RP}$ to improve the visibility of the charge transitions.

Previous works [11,36] have investigated nearly $1e$ periodic island charge occupancy, consistent with an emerging topological phase, using conductance. The use of reflectometry and charge instead has the advantage of not requiring electron transport through the device itself. As seen from Fig. 4(d), sensing is consistent with these previous transport studies [11]. We will not focus on peak spacing and motion here, to keep the focus on measurement methods.

C. Fast charge measurement and signal-to-noise ratios in the $1e$ regime

The SNR for detecting the transfer of a single electron between islands of the double-island device in Fig. 4(a) is investigated as a function of the measurement time using the pulsed gate sequence shown in Fig. 5(a).Measurements

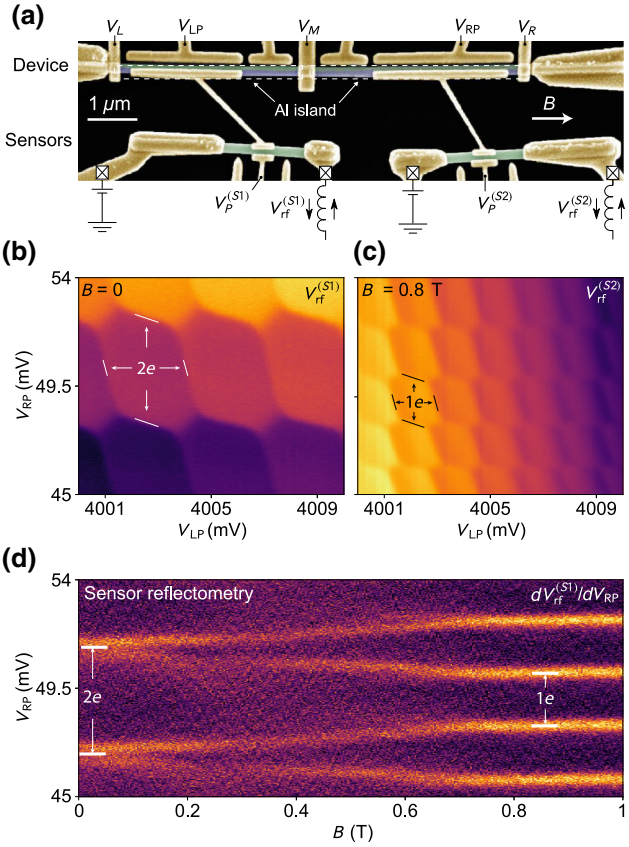

FIG. 4. The rf charge sensing of a double Majorana island: device C. (a) A scanning electron micrograph of the device measured (the white dashed boxes indicate the Al islands). The voltage-tunable tunnel barriers are labeled as V_L, V_M, and V_R. The island plunger gates are labeled as V_{LP} and V_{RP} for the left and right island, respectively. (b) The $2e$-$2e$ periodic superconducting double-island charge-stability diagram measured at $B = 0$ by rf charge sensing with a right sensor. (c) The $1e$-$1e$ periodic double-island charge-stability diagram measured at $B = 0.8$ T with a left sensor. (d) The evolution of the charge occupancy of the right island (controlled by V_{RP}) as a function of B. The color map shows the measured rf demodulated signal from the right sensor ($V_{rf}^{(S2)}$) and is differentiated along the V_{RP} axis. A periodicity change from $2e$ to $1e$ in the V_{RP} direction is observed as B is increased.

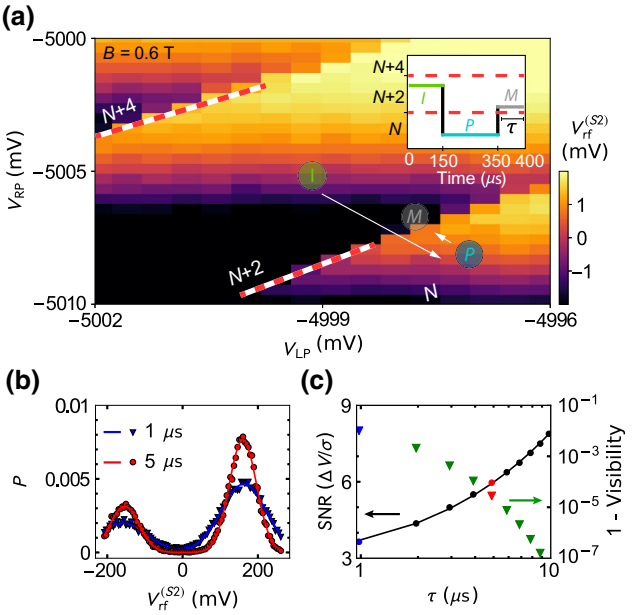

FIG. 5. The charge sensitivity and the SNR: device C. (a) The $1e$-$1e$ periodic double-island charge-stability diagram at $B = 0.6$ T, measured using the right-proximal charge sensor. The main device is configured such that tunneling to the left or right lead reservoirs is negligible. Only the interisland transitions are visible (red and white dashed lines). The relative charge occupancy of the islands is marked as N, $N+2$, and $N+4$. To characterise the SNR, a pulse sequence was used on gates LP and RP to move the system to different positions (I, M, and P) on the charge-stability diagram (for a description, see the main text and Appendix C), while the inset shows the sequence and duration of each pulse. (b) The probability of single-shot read-out outcomes (P) of demodulated voltage signal $V_{rf}^{(S2)}$ for two different measurement times: $\tau = 1$ μs (blue) and $\tau = 5$ μs (red), at the measurement point (M) showing a bimodal relative-charge-state distribution. (c) The SNR (left-hand axis) at the measurement point (M) together with theoretical fit. The extracted visibility (right-hand axis) from the double Gaussian fits (see the main text) is given as a function of the measurement time.

are done in an applied axial magnetic field $B = 0.6$ T, where the charge-stability diagram shows $1e$-$1e$ hexagons. However, in contrast to the tuning in Fig. 4(c), V_L and V_R are set to isolate the double island, with negligible coupling to the source and drain. Only interisland transitions [white and red dashed lines in Fig. 5(a)] are measurable in this configuration.

A cyclic pulse sequence is applied to gates LP and RP using an arbitrary waveform generator (Tektronix 5014c), placing the system in three configurations, initialization (I) for 150 μs, preparation (P) for 200 μs, and measurement (M) for a range of times from 1 μs to 50 μs [for details, see Fig. 5(a) inset and Appendix C]. The preparation position and duration are chosen to yield roughly equal populations of relaxed and exited populations, which also depend sensitively on the interisland-barrier gate voltage, V_M. The results of the measurement, integrated over the measurement time, are then binned to form histograms showing the distinguishability of the N and $N+2$ charge-difference states ($N = N_L - N_R$ is the charge difference, where N_L and N_R are the occupancies of the left and right islands). Note that the number of cycles used to gather the histogram statistics does not affect the distinguishability of the two states. More cycles yield a convergence of the histogram to a stable smooth bimodal distribution. On the other hand, the distinguishability of the two populations is affected by the duration at the measurement point (M). We note that read-out is carried out at the measurement point

(M) by triggering the waveform digitizer card (for details, see Appendix C).

The resulting histogram after 10^8 cycles is fitted with a sum of two Gaussians, as follows:

$$A_N e^{-(V_{\rm rf}^{(S2)}-\mu_N)^2/2\sigma_N^2} + A_{N+2} e^{-(V_{\rm rf}^{(S2)}-\mu_{N+2})^2/2\sigma_{N+2}^2}, \quad (1)$$

where A, μ, and σ are the amplitudes, means, and standard deviations of the N and $N+2$ charge differences. Measured distributions and best fits to Eq. (1) for measurement times $\tau = 1$ μs and $\tau = 5$ μs are shown in Fig. 5(b). The separation of the two peaks, ΔV, reflects the sensitivity of the charge sensor, while the peak widths σ_N and σ_{N+2} result from measurement noise. We define SNR $= \Delta V/\sigma$, where $\sigma^2 = \sigma_N^2 + \sigma_{N+2}^2$. Note that Eq. (1) does not include relaxation from N to $N+2$ during the measurement. A more complicated form that includes relaxation during measurement has been investigated in Ref. [37]. In the present case, where τ is much shorter than the charge relaxation time, as set by V_M, Eq. (1) is valid. The measured SNR as a function of the measurement time τ is shown in Fig. 5(c) (left-hand axis). A SNR > 3 with an integration time of 1 μs is achieved.

Figure 5(c) shows that the SNR increases with the measurement time, τ, as expected. The simplest model of this dependence, assuming uncorrelated noise [18], is $\mathrm{SNR}(\tau) = [\Delta V/\sigma(1\ \mu\mathrm{s})][(\tau+\tau_0)/1\ \mu\mathrm{s}]^{1/2}$. By using the fit parameters $\Delta V = 175.3$ mV, $\tau_0 = 1.5$ μs, and $\sigma(1\ \mu\mathrm{s}) = 74.8$ mV, the model yields the curve shown in Fig. 5(c), which compares well with the experimentally measured SNR(τ) in the range 1–10 μs. Another quantity that characterizes the quality of detection is the visibility, V, defined as the probability of correctly identifying excited and ground states (N and $N+2$) and expressed as $V = F_N + F_{N+2} - 1$, where F_N and F_{N+2} are the fidelities calculated following [37] (for details, see Appendix C). The resulting dependence of the visibility on the measurement time, $V(\tau)$, is shown in Fig. 5(c), where again the effects of relaxation during measurement are neglected. We find that $V(1\ \mu\mathrm{s}) = 0.998$. These results are comparable to previously reported charge-detection studies [38–42].

V. CONCLUSIONS

In summary, we investigate rf charge sensing and read-out of various InAs/Al nanowire devices relevant for Majorana qubits. Two read-out types are studied. First, resonant circuits are directly coupled to the device lead, yielding an improvement in measurement time by a factor of 40 compared to conventional lock-in measurements. Second, charge sensing via a second nanowire capacitively coupled to the device via a floating gate allows the charge occupancy in the device to read out noninvasively, even when visible transport is suppressed through the device. As an application, we follow the evolution of Coulomb charging from $2e$ periodicity to $1e$ periodicity as an axial magnetic field is increased from 0 to 0.6 T, complementing previous conductance measurements of Majorana signatures, without needing to run current through the device. The sensor quality as a function of the measurement time is investigated using a pulse sequence that cycles the charge occupancies of the islands. A SNR exceeding 3 can be achieved for integration times of 1 μs, with visibility $V =$ 99.8%. The presented results show that rf resonant circuits, coupled both directly to the device or to proximal capacitive sensors, can be used for fast and detailed characterization that conventional low-frequency techniques are unable to provide.

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D. Razmadze and D. Sabonis contributed equally to this work.

APPENDIX A: LEAD REFLECTOMETRY

Figure 6(a) shows a 2D map of $V_{\rm rf}$ as a function of V_L and V_P with $3000 \times 1500 = 4.5$ million points. The effective time constant per point $\tau = 200$ μs. The data are acquired over approximately 1 h using rf lead reflectometry. The estimated time of completion is about 40 h using lock-in techniques with a 30-ms integration time. At the moment, such gate maps are necessary for locating the topological regime in NW devices and as a result any technique that can speed up the acquisition of such data sets can give a big advantage in experimental research.

APPENDIX B: INSTRUMENTS

The reflectometry measurements presented in Figs. 2 and 6 are performed with the customized demodulation circuit presented in Fig. 7. Below, we list other electronic equipment used in the experiments.

(1) Demodulation unit, used for reflectometry measurements in Figs. 4 and 5: Zurich Instruments, Ultrafast Lock-in Amplifier (600 MHz) [28]

(2) Current-to-voltage converter: University of Basel, Electronics Laboratory, low-noise–high-stability I-V converter, SP 983 with IF3602

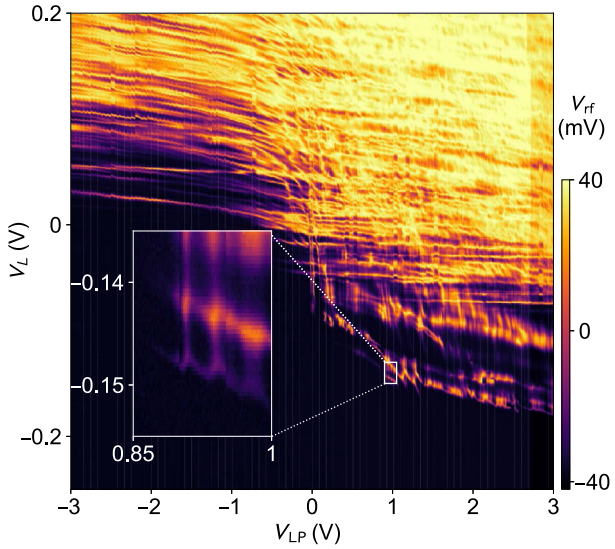

FIG. 6. A fast high-resolution charge-sensing measurement using lead reflectometry. The gate-voltage map of the left cutter, V_L, versus the plunger gate, V_P, acquired with the lead-sensing method in 1 h. The estimated time to complete a 2D gate-gate measurement with comparable resolution using a conventional lock-in with a 30 ms time constant would be approximately 40 h.

(3) Voltage sources: 48-channel QDAC, custom digital-to-analog converters, QDevil ApS [43]

(4) Lock-in: Stanford Research SR830 DSP lock-in amplifier

(5) Waveform generator: Keysight 33500B

(6) Arbitrary-waveform generator: Tektronix 5014 C, 1.2 GS/s

(7) Vector-network analyser: Rohde & Schwarz ZVB8

(8) Directional coupler: Minicircuits ZEDC-15-2B (1 MHz to 1 GHz)

(9) Microwave switch: Minicircuits ZASWA-2-50DR+ (dc, 5 GHz)

(10) Cryogenic 4 K amplifier: Caltech Weinreb CITLF3

(11) Digitizer: AlazarTech ATS9360 12-bit, 1.8 GS/s

APPENDIX C: SIGNAL-TO-NOISE RATIO AND VISIBILITY

The extraction of the SNR and the visibility is accomplished with the following pulse-sequence cycle [Fig. 5(a) inset]. The pulse sequence starts with a fixed-amplitude voltage pulse on gates RP (positive voltage pulse) and LP (negative voltage pulse), bringing the system to a point I for a duration of $\tau_I = 150\ \mu$s for initialization into a relative charge state $N+2$. Then, the gates LP (positive voltage pulse) and RP (negative voltage pulse) bring the system into a relative charge N state (point P) for a time $\tau_P = 200\ \mu$s. Finally, gates LP (negative voltage) and RP (positive voltage) bring the system close to intraisland degeneracy point M (between the N and $N+2$ relative

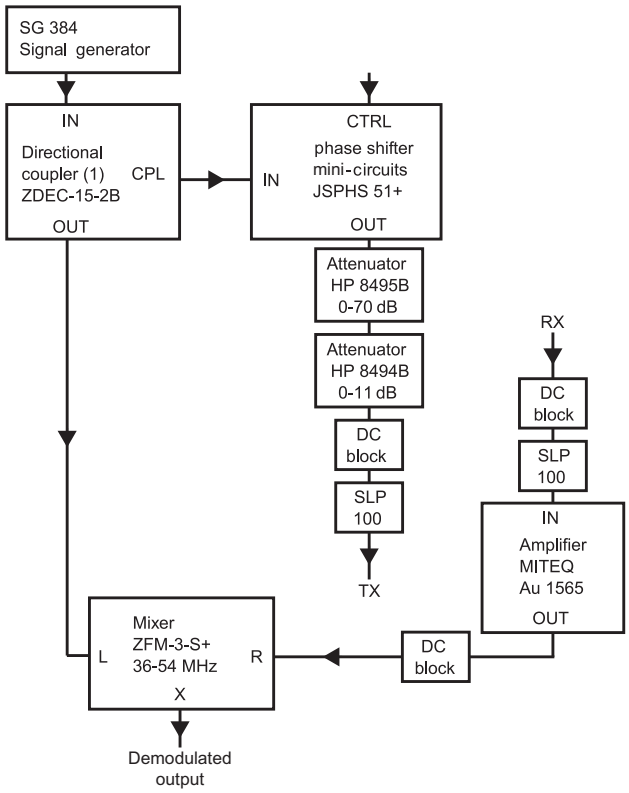

FIG. 7. A block diagram of the demodulation circuit.

charge states), which we denote as the measurement position. V_{TX} excitation is controlled by the microwave switch (ZASWA-2-50DR+), in order to avoid disturbances in the system during the manipulation phase (I and P). The readout is performed only at the measurement point (M) by triggering the ATS9360 12-bit waveform digitizer card for a total time duration of $\tau = 50\ \mu$s. To build the statistics, $N_{\text{cycles}} = 10^8$ experimental runs of the pulse sequence are performed. From histograms of $V_{rf}^{(S2)}$ measurements (with 2 mV bin size), the probability, $P_{V_{rf}^{(S2)}}$ of singe-shot outcomes can be estimated for each value of the measurement time τ.

For the sake of simplicity, all denoted V_{rf} here will refer to demodulated voltage with the right charge sensor ($V_{\text{rf}}^{(S2)}$). The visibility is defined as $V = F_N + F_{N+2} - 1$ [37], where F_N and F_{N+2} are the fidelities of the relative charge states N and $N+2$, respectively. The fidelity of a charge state, N, is defined by $F_N = 1 - \text{erf}(N)$, where $\text{erf}(N)$ is an error of having a pure N charge state. $N+2$ state fidelity is similarly expressed, as $F_{N+2} = 1 - \text{erf}(N+2)$. This error is calculated using a cumulative-normal-distribution function, which for the $N+2$ state is $\int_{-\infty}^{V_T} n_{N+2} dV_{rf}$, where V_T is the threshold voltage calculated by the two-mean-Gaussian-fit peak position $[(\mu_N + \mu_{N+2})/2]$ and n_{N+2} is the probability density for relative charge state $N+2$, which is expressed as

$e^{(V_{\rm rf}-\mu_{N+2})^2/2\sigma_{N+2}^2}/\sqrt{2\pi}\sigma_{N+2}$. The error of having a pure N state can be expressed as $\int_{V_T}^{\infty} n_N dV_{rf}$, with probability density $e^{(V_{\rm rf}-\mu_N)^2/2\sigma_N^2}/\sqrt{2\pi}\sigma_N$. Minimizing the function of two errors (erf(N) and erf($N+2$)) and then inserting the found fidelities, we calculate the visibility $V = 1 - \text{erf}(N) + 1 - \text{erf}(N+2) - 1$. This yields a visibility $V = 99.8\%$ for an integration time of 1 μs.

APPENDIX D: FABRICATION

All of the devices presented have a nanowire (NW) diameter of approximately 100 nm. The NWs are grown using the vapor-liquid-solid technique in a molecular-beam-epitaxy system with the InAs [111] substrate crystal orientation [44]. Following the NW growth, Al is deposited epitaxially *in situ* on several facets of the NW, with an average thickness of 10 nm [10,44]. The NW is then positioned on a chip with a homebuilt micromanipulator tool [a Zaber XYZ-Theta stage with an Eppendorf micromanipulator (model 4r) and a large-working-distance Leica microscope], which allows micrometer precision in placement. The Al is selectively etched using wet etchant Transene D. All patterning is performed using an Elionix ELS-7000 EBL. Next, we present the details specific to fabrication of all three devices:

(1) Device A: The InAs/Al NW has Al shell on two of its facets and is fabricated on a Si chip covered with 200 nm of SiO_2. The Ti-Au contacts (5 nm + 150 nm) are evaporated after performing rf milling to remove the oxide from the NW. Then, 7 nm of HfO_2 is deposited by atomic-layer deposition. Finally, the last set of Ti-Au gates (5 nm + 150 nm) is evaporated.

(2) Device B: The InAs/Al NW has Al shell on two of its facets and is fabricated on a Si chip covered with 500 nm of SiO_2. Then, the first set of Ti-Au contacts (5 nm + 100 nm) is evaporated after performing rf milling to remove the oxide from the NW. Finally, the last set of Ti-Au gates (5 nm + 100 nm) is evaporated.

(3) Device C: The InAs/Al NW has Al shell on two of its facets and is fabricated on a Si chip covered with 200 nm of SiO_2. The Ti-Au contacts (5 nm + 150 nm) are evaporated after performing rf milling to remove the oxide from the NW. Then, 5 nm of HfO_2 is deposited by atomic-layer deposition. Finally, the last set of Ti-Au gates (5 nm + 150 nm) is evaporated.

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