Voltage-Controlled Topological Spin Switch for Ultralow-Energy Computing: Performance Modeling and Benchmarking

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A voltage-controlled topological spin switch (VTOPSS) that uses a hybrid topological insulator–magnetic insulator multiferroic material is presented that can implement Boolean logic operations with sub-10-aJ energy per bit and an energy-delay product on the order of 10^{-26} J s. The device uses a topological insulator, which has the highest efficiency of conversion of the electric field to spin torque yet observed at room temperature, and a low-moment magnetic insulator that can respond rapidly to a given spin torque. We present the theory of operation of the VTOPSS, develop analytic models of its performance metrics, elucidate performance scaling with dimensions and voltage, and benchmark the VTOPSS against existing spin-based and CMOS devices. Compared with existing spin-based devices, such as all-spin logic and charge-spin logic devices, the VTOPSS offers 10–70 times lower energy dissipation and 70–1700 times lower energy-delay product. With experimental advances and improved material properties, we show that the energy and energy-delay product of the VTOPSS can be lowered to a few attojoules per bit and 10^{-28} J s, respectively. As such, the VTOPSS technology offers competitive metrics compared with existing CMOS technology. Finally, we establish that interconnect issues that dominate the performance in CMOS logic are relatively less significant for the VTOPSS, implying that highly resistive materials can indeed be used to interconnect VTOPSS devices.

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I. INTRODUCTION

Spin-based logic and memory devices use nanomagnets as digital spin capacitors to store and manipulate information [1]. Typically, spin-polarized electric currents or magnetic fields are used to control the magnetization vector of nanomagnets while reading and writing information [2]. Compared with their charge-based counterparts, spin-based devices offer nonvolatility of information and superior logical efficiency (i.e., fewer devices to implement a given Boolean function [3]). However, most spin-based devices suffer from high energy dissipation resulting from a large electric current density on the order of 10^6 A/cm^2 required to reorient the magnetization vector [4,5]. Such large current densities not only lead to excessive Joule heating in the device but could cause electromigration issues in metallic interconnects [6]. At the same time, reversal of metallic ferromagnetic bodies using antidamping spin-transfer torque (STT) proceeds on a timescale on the order of hundreds of picoseconds to a few nanoseconds [7]. As such, existing spin-based devices have an energy-delay product (EDP) that is 1000 to 10 000 times larger than that of their CMOS counterparts [8].

To harness the full potential of spintronics technology, it is imperative to develop methods for energy-efficient and fast manipulation of the magnetic order parameter. Actuation methods, such as voltage control of magnetic anisotropy and coercivity, use of magnetoelectric and exchange coupling in multiferroic-ferromagnetic heterostructures, and charge-carrier-density-mediated ferromagnetism control, have been investigated [9,10]. Yet, these effects are generally weak at room temperature, which limits their practical use. For example, full 180° reversal of a ferromagnet via the magnetoelectric effect requires the assistance of electric currents or magnetic fields or can be accomplished with the resonant pulsed switching mode, which requires precise pulse timing [11–14]. Magnetoelastic effects that are used to tune the magnetic properties of thin films via epitaxial strain or piezoelectric substrates are generally observed in low-aspect-ratio nanomagnets [15,16]. However, in high-aspect-ratio nanomagnets it is difficult to use strain effects to tune the magnetic properties.

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A promising research direction is "topological spintronics," which has been driven by the demonstration of efficient room-temperature spin-charge conversion in heterostructures with a topological insulator (TI) interfacing with a ferromagnetic metal [17]. The key property responsible for this advance is the combination of large spin-orbit-coupling (SOC) strength and time-reversal symmetry that leads to the formation of helical Dirac surface states possessing an inherent spin-momentum locking [18–21]. The distinctive feature of TIs is that even without carriers near the chemical potential in the bulk, the spin Hall conductivity can be finite and significantly larger than that of heavy metals such as Pd, Pt, and W [22–24].

Here we use electric fields across a TI, resulting in coherent transport of spins across the material, to generate a spin torque on the magnetization of an adjacent magnetic insulator (MI) layer [25]. Unlike for a ferromagnetic metal, there is no shunting of electric current in the MI layer and current is restricted to flow on the surface of the TI layer. Furthermore, the MI can induce a gap in the TI surface states, rendering the TI surface state insulating, which is (counterintuitively) beneficial for the device operation. The spin-based device, a voltage-controlled topological spin switch (VTOPSS), decouples the elements of a magnetoelectric material [26], allowing us to simultaneously optimize the choice of both TI and MI materials, thereby enabling ultralow-energy computing. One of the most important properties of the MI layer is its low damping [27,28], which is highly desirable in device applications where switching is realized through magnetization precession, as in a VTOPSS.

The transduction principle of charge current to magnetization to charge current is an old one, used prominently by Datta and Das [29] in their first spin-FET proposal, and also in later spin FETs, such as the device proposed by Hall and Flatté [30] in 2006. A similar transduction principle is also used in the charge-spin logic (CSL) device proposed by Datta *et al.* [31,32] in 2012. Unlike prior device proposals, the VTOPSS is purely electric field driven such that charge-to-magnetization transduction is accomplished without the flow of electric current. The magnetoelectric effect in the VTOPSS allows efficient charge-spin conversion at the TI-MI interface solely by application of an electric field across the TI. Given that a TI possesses a large spin Hall conductivity even without carriers near the chemical potential in its bulk, it avoids the dissipative charge currents present in heavy-metal layers [33] used as spin generators in the CSL device. Although both devices use a magnetic tunnel junction (MTJ) to read the magnetization information, in the VTOPSS the free layer of the MTJ is exchange-coupled to the MI layer, making the read process more robust against the effects of thermal noise.

The remainder of this paper is organized as follows. In Sec. II, the physics of operation of the VTOPSS is presented. In Sec. III, analytic models of performance metrics of the VTOPSS are presented, followed by benchmarking results against existing spin- and charge-based devices in Sec. IV. In Sec. V, implementation of universal Boolean logic gates and the logical efficiency of the VTOPSS resulting from its innate polymorphism are highlighted. Section V summarizes the key findings of this work while also offering an outlook on future research directions.

II. PHYSICS OF OPERATION

The evolution of the wave functions of the full bands of the TI, under the influence of an electric field, produces coherent transport of spins across the material [34], which can be used to efficiently manipulate the magnetization state of an adjacent magnetic layer [35]. The charge Hall conductivity and bulk dissipative charge currents vanish or are small in the TI, but the spin Hall conductivity is finite and can be much larger than that of a large-SOC metal [36]. A TI has the highest efficiency of conversion of the electric field to spin torque yet observed at room temperature [37,38]. Hybrid TI-MI structures decouple the constituent features of a multiferroic material, allowing independent optimization of both components of the response of magnetization to an electric field (i.e., generation of spin torque from the electric field and response of the magnetic moments to the spin torque).

The total Berry curvature of a full band measures the integrated correlation between spin and orbital degrees of freedom. For a so-called trivial insulator this correlation integrates to zero across the entire full band. Thus, if at one region of the Brillouin zone the wave functions of the band have spin and orbit correlated preferentially parallel, there will be another region of the zone in which the wave functions are correlated preferentially antiparallel. An example is the valence band in a trivial direct-gap semiconductor, such as GaAs, which is of p-orbital character, for which the wave functions near the valence maximum are heavy-hole states, with spin and orbit degrees of freedom parallel, whereas at energies below the split-off energy, the spin and orbit degrees of freedom are preferentially oriented antiparallel.

TIs differ from these trivial insulators in that this spin-orbit correlation does not integrate to zero. The spin-orbit correlation is described quantitatively by the Berry curvature of the band, and thus the electronic ground state in a TI possesses a nonzero integrated Berry curvature. The spin Hall conductivity in the clean static limit, evaluated as the linear response of the spin current to an electric field by the Kubo approach, depends directly on the Berry curvature:

$$\sigma_{yx} = \frac{e\hbar}{V} \sum_{n} \sum_{k} f_{n\mathbf{k}} \Omega^{z}_{n\mathbf{k}}, \tag{1}$$

where e is the elementary charge, $\hbar$ is the reduced Planck constant, V is the volume of the system, $\mathbf{k}$ is the crystal momentum, n is a band index, and is $\Omega^z_{n\mathbf{k}}$ is the Berry curvature,

$$\Omega^z_{n\mathbf{k}} = 2\sum_{n\neq n'} \mathrm{Im}\frac{\langle u_{n\mathbf{k}}|j^z_y|u_{n'\mathbf{k}}\rangle\langle u_{n'\mathbf{k}}|v_x|u_{n\mathbf{k}}\rangle}{(E_{n\mathbf{k}}-E_{n'\mathbf{k}})^2}. \quad (2)$$

Here the Fermi-Dirac function $f_{n\mathbf{k}}$ ensures that the sum is over filled states, corresponding to all the filled bands at zero temperature. The spin-current and velocity operators, $\hat{j}^j_i$ and $\hat{v}_i$, are

$$\hat{j}^j_i = \frac{\hbar}{4}(\hat{v}_i\sigma_j + \sigma_j\hat{v}_i), \quad \hbar\hat{v}_i = \nabla_{k_i}\hat{H}, \quad (3)$$

where σ_j is the spin operator along direction j and $\hat{H}$ is the Hamiltonian of the material. The current and velocity operators are evaluated between the states with Bloch functions $u_{n\mathbf{k}}$ and $u_{n'\mathbf{k}}$ with energies $E_{n\mathbf{k}}$ and $E_{n'\mathbf{k}}$, respectively.

As the integrated Berry curvature of the full band does not vanish for a TI, and the spin Hall conductivity is directly related to the total Berry curvature of the filled states of the TI, even without any carriers near the chemical potential in the bulk, the spin Hall conductivity does not vanish. This characteristic clearly identifies the spin current involved as nondissipative until it encounters other regions, such as an interface. Here we take advantage of this localized effect to drive the VTOPSS shown in Fig. 1. The device relies on the accumulation of spins at an interface, originating from the voltage (V_{in}) applied to the TI. The spin Hall conductivity for a TI can be as large as (or larger than) that of a large-SOC metal, but the dissipative longitudinal charge current will vanish for the TI. Thus, a TI provides the advantages of a large spin Hall conductivity, but without the intrinsic dissipation of a metallic material. The resulting spin current produced by the electric field on the TI generates a torque on the spin in the magnetic material through exchange coupling or antidamping torque. In the case of effective exchange coupling, the torque forces the magnetization to precess and eventually reverse.

The spin current density created by application of an electric field E_{TI} is

$$J_s = \sigma_{yx}E_{\mathrm{TI}}. \quad (4)$$

The resulting magnetization dynamics of the ferromagnetic insulator can be described by the Landau-Lifshitz-Gilbert-Sloncewski equation in a macrospin limit [39]:

$$\frac{1}{\gamma'}\frac{d\hat{\mathbf{m}}}{dt} = -\mu_0\hat{\mathbf{m}}\times\mathbf{H}_{\mathrm{eff}} - \alpha\mu_0\hat{\mathbf{m}}\times\left(\hat{\mathbf{m}}\times\mathbf{H}_{\mathrm{eff}}\right) - \underbrace{c_{\mathrm{ex}}j_s\hat{\mathbf{m}}\times\hat{\mathbf{p}}}_{\text{Field like torque}} + \underbrace{j_s\hat{\mathbf{m}}\times\left(\hat{\mathbf{m}}\times\hat{\mathbf{p}}\right)}_{\text{Slonczewski torque}}, \quad (5)$$

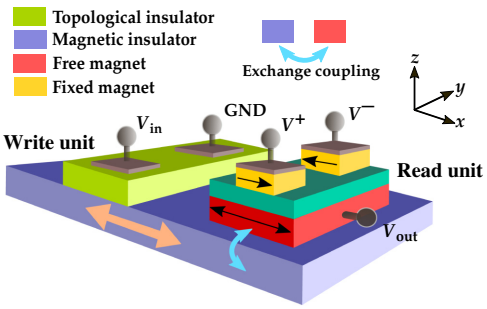

FIG. 1. Copy and invert functions implemented with the VTOPSS. In the write unit, an input voltage signal applied across the TI layer causes spin accumulation at the interface of the TI and MI layers, which exerts a spin torque on the magnetization of the MI layer to reverse it. The read unit has a MTJ exchange-coupled to the MI layer that allows reading of the information in the MI layer. The polarity of the output voltage can be changed on the fly by change of the polarity of the voltages V^+ and V^- on the MTJ stack, allowing both inverting and noninverting logic to be realized with the same primitive/layout. Typical system materials include $Bi_2Se_3/(Bi_xSb_{1-x})_2Te_3$ as the TI, $Y_3Fe_5O_{12}$, $(Ni_{0.65}Zn_{0.35})(Al_{0.2}Fe_{0.8})O_4$, $BaFe_{12}O_{19}$, or $Tm_3Fe_5O_{12}$ as the MI, (Co,Fe)B-MgO-(Co,Fe)B/Ru/CoFe/IrMn (synthetic antiferromagnet) as the MTJ, and metallic or semiconducting nanointerconnects with effective resistivity less than 100 $\mu\Omega$ cm as wires. GND, ground.

where $\hat{\mathbf{m}}$ is a unit vector in the magnetization direction, $\gamma' = \gamma/(1+\alpha^2)$, where γ is the gyromagnetic ratio, μ_0 is the vacuum permeability, and α is the Gilbert damping coefficient. The last two terms describe a spin torque from a spin current polarized in a direction $\hat{\mathbf{p}}$, generally perpendicular to the electric field and in the plane of the TI-MI interface. $J_s = 2M_s t_{\mathrm{MI}} j_s$, where M_s is the magnetization of the MI layer and t_{MI} is its thickness. (We assume a thin ferromagnetic insulator with area in contact with the topological insulator A_{int} and thickness t_{MI}.) The first spin-torque term describes the precession of the magnetization about the spin-polarization direction, with an exchange-coupling parameter c_{ex}. (For an estimate of this parameter, see Ref. [35].) This term is often referred to as a fieldlike interaction. The second spin-torque term characterizes the Slonczewski "antidamping" torque, a torque that can oppose the dissipative term (the second term on the right-hand side of the equation), leading to precessional magnetization dynamics and switching.

The effective field $\mathbf{H}_{\mathrm{eff}}$ characterizes the magnetic anisotropy of the free layer. For a uniaxial magnet with easy-magnetization direction in the y direction

$$\mathbf{H}_{\mathrm{eff}} = 2E_b m_y/(\mu_0 M_s V_{\mathrm{MI}}), \quad (6)$$

where E_b is the energy barrier to magnetization reversal and V_{MI} is the volume of the MI layer. The magnetization-switching mechanism depends on the orientation of the

magnetic easy axis relative to the direction of spin polarization $\hat{\mathbf{p}}$. When the two are orthogonal, the switching can occur due to precession about the spin-polarization direction and can be very fast (less than 100 ps) [40–42]. However, typically precise electric pulse timing is required to ensure switching. When the spin polarization is collinear with the easy-axis direction, the switching is slower but the pulse time is not a critical parameter; in general, the write error rate decreases monotonically with either increasing pulse amplitude or increasing pulse duration [43]. The electric field polarity determines the sense of reversal (i.e., from $m_y = 1$ to -1 and vice versa). The threshold spin current density for antidamping spin-current switching follows from Eq. (5), $J_{s,\mathrm{th}} = 4\alpha E_b/A_{\mathrm{int}}$. The antidamping switching mechanism is considered in the analysis presented in Sec. III.

We note a key difference between the current in the VTOPSS and that in a STT device. In a STT device, the current, carried by individual carriers, is parallel to the applied electric field and Joule heating is produced. That contrasts with our device, in which the current flows perpendicular to the surface of the topological insulator (not along it) and is perpendicular to the applied electric field, making it nondissipative. The current itself in the bulk of the topological insulator is carried by the full band (not individual carriers), corresponding to a protected spin current similar to the quantized charge current in a quantum Hall state, which cannot scatter. Moreover, the current in the VTOPSS does not need to be on during the entire switching cycle since we are using the spin accumulation that results from the applied voltage to switch the device.

As shown in Fig. 1, the readout in the VTOPSS is accomplished by exchange coupling a small section of the MI layer (storing information) to the free layer of a MTJ, which could operate with sub-100-mV supply voltages (V^+ or V^-) to generate sufficient output voltage (V_{out}) with intrinsic gain and the ability to fan out. This separates the robust information-storage aspect from the transduction within a hybrid magnetoelectric device, allowing one to probe the magnetization without disturbing the state.

While the device schematic in Fig. 1 shows the TI and the MTJ integrated laterally on the MI layer, the layers can be integrated vertically to achieve a smaller footprint of the device and higher integration density. The top view of the device for lateral and vertical integration schemes is shown in Fig. 2. In Sec. III, we highlight key differences in the scaling behavior of delay and energy dissipation with device dimensions for both layouts. For the purpose of performance benchmarking in Sec. IV, we consider only the vertically integrated VTOPSS.

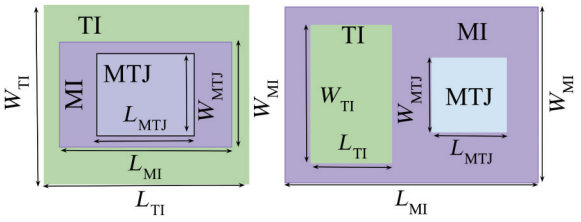

FIG. 2. Vertically integrated layers (left) and laterally integrated layers (right) in the VTOPSS. The interface area in the vertical layout is $\mathcal{A}_{\mathrm{int}} = W_{\mathrm{MI}}L_{\mathrm{MI}}$, while that in the lateral layout is $\mathcal{A}_{\mathrm{int}} = W_{\mathrm{TI}}L_{\mathrm{TI}}$.

III. PERFORMANCE MODELING

In most spin-based devices, the operating speed is limited by the time it takes to reverse the magnetization of the metallic ferromagnetic layer, which is typically on the order of 1 ns. Spin-based devices using the spin Hall effect in heavy metals, such as Pt, Pd, and W, require large electric fields in the heavy metal to generate sufficient electric current to cause STT switching of nanomagnets. The VTOPSS takes advantage of the unique properties of TI and MI material systems to achieve the following criteria for energy-efficient logic applications: (i) nonvolatility of operational states, (ii) fully-voltage-driven switching of the MI magnetization with voltages less than 100 mV, (iii) absence of dissipative electric currents during the write process, and (iv) ultrafast switching of the MI magnetization due to its low Gilbert damping.

In this section, analytic models of latency and energy dissipation of the VTOPSS are presented, followed by a comparison of metrics against those of existing spin-based and charge-based devices. Analytic models are obtained for a uniaxial MI layer subjected to antidamping STT resulting from spin accumulation at the TI-MI interface when the TI is subjected to an external electric field. Micromagnetic effects in magnetization reversal, such as reversed domain nucleation and expansion in the MI layer, are not considered in this paper. Experiments have shown that such multidomain effects could lead to faster magnetization reversal, particularly in the absence of defects and pinning sites in the magnet [44,45]. The essential physics of magnetization reversal is determined by the transfer of angular momentum (the total angular momentum that needs to be switched and the rate at which angular momentum can be changed by the interactions present). As such, the macrospin model provides the correct order of magnitude for magnetization-switching thresholds and times even in the presence of nucleation and reversed domain expansion. Here we adopt the macrospin approximation, which affords analytic insight into the device performance limits and can be used readily for the optimization of device geometry and materials.

A. Device latency

To estimate VTOPSS latency, the rate of spin accumulation at the TI-MI interface must be calculated. For a given

electric field ($E_{\rm TI}$) and spin Hall conductivity ($\sigma_{\rm SHC}$) of the TI layer, the accumulation rate of interface spins is given as

$$\frac{dn_{\rm spins}}{dt} = \frac{\sigma_{\rm SHC}}{\hbar/2}E_{\rm TI} = \frac{\sigma_{\rm SHC}}{\hbar/2}\frac{V_{\rm in}}{W_{\rm TI}}, \tag{7}$$

where $V_{\rm in}$ is the voltage applied across the TI layer and $W_{\rm TI}$ is the width of the TI layer, measured along the y axis in Fig. 1 and also marked in Fig. 2. For a given efficiency ε of coupling of spins at the TI-MI interface and the magnetic moment of the MI layer, the following condition is satisfied:

$$N_{\rm spins,MI} = \varepsilon n_{\rm spins}\mathcal{A}_{\rm int}, \tag{8}$$

where $N_{\rm spins,MI}$ is the total number of spins in the MI layer subjected to spin torque due to the interface spin accumulation and $\mathcal{A}_{\rm int}$ is the interface cross-section area. The total number of spins in a magnetic body is given as

$$N_{\rm spins,MI} = \frac{M_s V_{\rm MI}}{\mu_B} = \frac{2E_b}{\mu_B H_K}, \tag{9}$$

where H_K is the anisotropy field of the MI layer and $\mu_B = 9.3 \times 10^{-24}$ J/T is the Bohr magneton. Assuming antidamping switching of the MI layer in the ballistic limit ($J_{\rm MI} \gg J_{\rm th}$), the rate of spin accumulation at the interface will balance the rate of magnetization reversal of the MI layer. Here $J_{\rm MI}$ is the input spin current density in the MI layer, while $J_{\rm th}$ is the threshold spin current density required for STT-induced magnetization reversal. In this case, the reversal time of the MI layer is [44]

$$\tau_{\rm MI,0} = \frac{N_{\rm spins,MI}}{\varepsilon\mathcal{A}_{\rm int}dn_{\rm spins}/dt} = \frac{2eE_b}{\epsilon\mu_B H_K\sigma_0 V_{\rm in}}\frac{W_{\rm TI}}{\mathcal{A}_{\rm int}}, \tag{10}$$

where $\sigma_{\rm SHC} = \sigma_0(\hbar/2e)$. The interface area depends on the device layout as indicated in the caption for Fig. 2. The STT-driven reversal of the MI layer will be subject to thermal fluctuations, which could result in switching errors. To account for switching errors ($\mathcal{P}_{\rm err}$), the switching delay of the MI layer is modified according to

$$\tau_{\rm MI} = \tau_{\rm MI,0}\eta_{\rm st}, \tag{11a}$$

$$\eta_{\rm st} = -0.5\ln\left(-\frac{\ln(1-\mathcal{P}_{\rm err})}{4E_b/k_BT}\right). \tag{11b}$$

For $\mathcal{P}_{\rm err} = 10^{-12}$ and $E_b = 30k_BT$, the stochastic parameter $\eta_{\rm st} \approx 16$, which gives $\tau_{\rm MI} = 16\tau_{\rm MI,0}$. With new error-tolerant computing paradigms related to approximate and probabilistic computing with spin-based devices, one may not need such low error rates [46–48]. For $\mathcal{P}_{\rm err} = 0.5$, $\eta_{\rm st} \sim 2.58$. We choose $\eta_{\rm st} = 10$ and $E_b = 30k_BT$ ($\mathcal{P}_{\rm err} = 10^{-7}$) for performance benchmarking in Sec. IV. These parameters ($E_b = 30k_BT$ and $\mathcal{P}_{\rm err} = 10^{-7}$) allow us to have a fair and consistent comparison of the VTOPSS against existing spin-based devices, including all-spin logic (ASL), magnetoelectric spin-orbit (MESO) logic, and CSL devices, in which the energy barrier of the magnetic layer is approximately (5–40)k_BT [31,49–51]. Issues pertaining to circuit- and system-level error analyses are beyond the scope of this work.

Increases in $\sigma_{\rm SHC}$ of the TI layer and the spin-coupling efficiency are particularly beneficial toward reducing the device latency. While the total latency of the device must include the time needed to charge and discharge the device capacitance (sum of interconnect and TI input capacitance), the analysis presented in Sec. III E shows that the dominant time constant is due to the rate of spin accumulation at the TI-MI interface.

B. Thermal stability

The reversal delay of the MI layer can be reduced by lowering of the energy barrier E_b; however, this comes at the cost of reduced thermal stability of the MI layer. The reversal time of a uniaxial magnet subjected only to thermal noise is given as [52,53]

$$\tau_{\rm stable} = \frac{\sqrt{\pi}\left(\alpha+\alpha^{-1}\right)}{2\gamma H_K\sqrt{e_{b0}}}\left(1+\frac{1}{e_{b0}}+\frac{7}{4e_{b0}^2}\right)e^{e_{b0}}, \tag{12}$$

where $e_{b0} = E_b/k_BT$ is the normalized energy barrier of the magnet. For $\alpha = 3 \times 10^{-3}$, $H_K = 0.1$ T, and $e_{b0} = 30$, we find $\tau_{\rm stable} = 3.39 \times 10^4$ s (0.392 days). The stability increases for $\alpha = 10^{-4}$, with $\tau_{\rm stable} = 1.0171 \times 10^6$ s (11.8 days). For most computing applications with clock frequency $f_{\rm clock} = 3$ GHz and activity factor $\alpha_{\rm act} = 10\%$ (1%), a device will switch on average once per 3.3 ns (33 ns). Over the device-relevant computational time (Δt), the probability of error at a fixed $\tau_{\rm stable}$ is $\mathcal{P}_{\rm err} = 1 - \exp(-\Delta t/\tau_{\rm stable})$. For $\Delta t = 33$ ns and $\tau_{\rm stable} = 3.39 \times 10^4$ s, $\mathcal{P}_{\rm err} = 9.73 \times 10^{-13}$. As shown in Fig. 3, for $e_{b0} = 30$, the error rate stays well under 10^{-10} for $\Delta t = 100$ ns (corresponding to $\alpha_{\rm act} = 0.33\%$ at $f_{\rm clock} = 3$ GHz). These results quantitatively show that an energy barrier of $30k_BT$ could provide sufficient thermal stability for most computing applications.

C. Minimum input voltage

The input voltage, $V_{\rm in}$, across the TI is a critical parameter that affects the dynamics and the switching time of the VTOPSS. The model in Eq. (11) is valid only when $J_{\rm MI} > 2J_{\rm th}$. Therefore, an estimate of the minimum input voltage $V_{\rm in}^{\rm min,ST}$ is found by considering $J_{\rm MI} = 2J_{\rm th}$, which

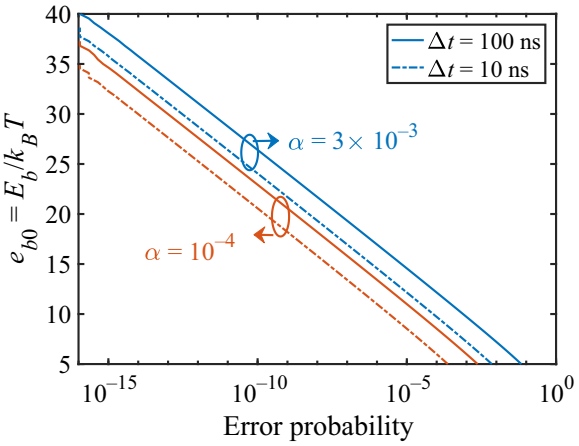

FIG. 3. Required energy barrier in a uniaxial magnet subjected to a random thermal field for a given probability of error within a time duration Δt.

results in

$$V_{\rm in}^{\rm min,ST} = \frac{8e\alpha E_b}{\hbar\sigma_0}\frac{W_{\rm TI}}{\mathcal{A}_{\rm int}}. \tag{13}$$

From thermodynamic considerations, however, the minimum input voltage will be limited by the Johnson-Nyquist (JN) noise. Considering that the output node of the VTOPSS can be represented as a low-pass RC filter, the spectral density of the thermal noise is given as $V_n^2 = 4k_BTR_{\rm eq}$, where $R_{\rm eq}$ is the equivalent resistance for charging and discharging the output capacitor, $C_{\rm out}$. To find the total noise, we integrate the spectral density over the noise bandwidth Δf , which is given as

$$\Delta f = \frac{1}{2\pi}\int_0^\infty \frac{d\omega}{1+\left(\omega R_{\rm eq}C_{\rm out}\right)^2} = \frac{1}{4R_{\rm eq}C_{\rm out}}. \tag{14}$$

The total noise voltage across the output capacitor is therefore given as $v_n^{\rm min,JN} = \sqrt{V_n^2\Delta f} = \sqrt{k_BT/C_{\rm out}}$.

If we combine the limits due to spin-torque reversal and JN noise in the system, the minimum input voltage for the VTOPSS is given as

$$V_{\rm in}^{\rm min} = \max(V_{\rm in}^{\rm min,ST}, v_n^{\rm min,JN}). \tag{15}$$

For $\alpha = 3\times 10^{-3}$, $E_b = 30k_BT$, $W_{\rm TI} = 100$ nm, $\mathcal{A}_{\rm int} = 50\times 100$ nm^2, and $\sigma_0 = 2\times 10^5$ $(\Omega\,{\rm m})^{-1}$, we get $V_{\rm in}^{\rm min,ST} \sim 0.5$ mV. For $C_{\rm out} \approx 20$ aF (sum of interconnect capacitance and capacitance of the fan-out TI layer), $v_n^{\rm min,JN} \sim 15$ mV. Therefore, in this case, $V_{\rm in}^{\rm min} = v_n^{\rm min,JN} = 15$ mV. For $V_{\rm in} = 100$ mV, $\epsilon = 0.5$, and $\eta_{\rm st} = 10$, $\tau_{\rm MI} = 860$ ps. The other parameters are the same as noted earlier. With larger spin Hall conductivity, we can expect the reversal delay of the VTOPSS to be well under 500 ps even for an error rate of 10^{-7}.

D. Minimum read voltage

In the VTOPSS, the read unit is a MTJ stack coupled to the MI layer as depicted in Fig. 1. The read voltages are labeled as V^+ and V^- and have the same magnitude but opposite polarity; that is, $V^+ = V_{\rm read}$ and $V^- = -V_{\rm read}$, where $V_{\rm read}$ is the magnitude of the voltage applied to the MTJ to read the magnetization state of the MI layer. The supply voltages are clocked such that the writing and reading of a given logic stage happen in concurrent cycles. The voltage generated at the output node $V_{\rm out}$ of the nth stage drives the write unit of the $(n+1)$th stage. The output voltage must meet the $V_{\rm in}^{\rm min}$ criterion in Eq. (15).

The equivalent-circuit model of the VTOPSS is shown in Fig. 4. The interconnect is modeled as a lumped RC network with $R_{\rm ic}$ and $C_{\rm ic}$ representing the total interconnect resistance and capacitance, respectively [54]. For a given interconnect length $L_{\rm ic}$, $R_{\rm ic} = r_{\rm ic}L_{\rm ic}$ and $C_{\rm ic} = c_{\rm ic}L_{\rm ic}$, where $r_{\rm ic}$ and $c_{\rm ic}$ are the per-unit-length interconnect resistance and capacitance, respectively. The per-unit-length interconnect resistance $r_{\rm ic} = \rho_{\rm eff}/\mathcal{A}_{\rm ic}$, where $\rho_{\rm eff}$ is the effective resistivity of the wire and depends on the material as well as grain-boundary and sidewall carrier scatterings in interconnects with scaled cross-section area [55], while $\mathcal{A}_{\rm ic} = 2W_{\rm ic}^2$ is the cross-section area of the interconnect assuming that the interconnect thickness is twice the interconnect width, $W_{\rm ic}$. The conductances of the parallel and antiparallel configurations of the free layer and the fixed layer in the MTJ stack are denoted as $G_{\rm P}$ and $G_{\rm AP}$, respectively. These conductances are typically determined from tunneling-magnetoresistance (TMR) and resistance-area-product (RA) measurements of the MTJ structure. TMR is given as $(G_{\rm P} - G_{\rm AP})/G_{\rm P}$, while the RA is given as $\mathcal{A}_{\rm MTJ}/(G_{\rm P} + G_{\rm AP})$, where $\mathcal{A}_{\rm MTJ}$ is the cross-section area of the MTJ stack. For all results reported in this paper, $\mathcal{A}_{\rm MTJ} = \mathcal{A}_{\rm int}$ unless otherwise specified.

The capacitance of the TI layer is $C_{\rm TI}$, while the leakage of electric current through the TI is modeled with the leakage conductance $G_{\rm TI}$. The TI capacitance is given as

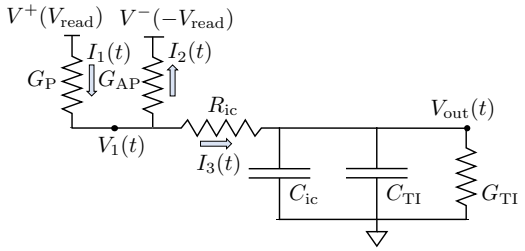

FIG. 4. Equivalent electric circuit of the read unit of a stage driving the write unit of the following stage. The MTJ stack conductances are given as $G_{\rm P}$ (parallel) and $G_{\rm AP}$ (antiparallel). The total interconnect resistance and capacitance are $R_{\rm ic}$ and $C_{\rm ic}$. The TI layer is modeled as a leaky capacitor with capacitance $C_{\rm TI}$ and shunt conductance $G_{\rm TI}$. The MTJ read voltages have the same magnitude but opposite polarity.

$C_{\rm TI} = \epsilon_0\epsilon_r\mathcal{A}_{\rm int}/W$, where $\epsilon_0 = 8.85 \times 10^{-12}$ F/m and ϵ_r is the static relative dielectric permittivity of the TI layer. For Bi_2Se_3, $\epsilon_r \approx 110$ [56]. The leakage conductance $G_{\rm TI} = G_{\rm sheet}L/W$, where $G_{\rm sheet} = en_s\mu$ [57], where n_s and μ correspond to the density and the effective mobility of surface carriers, respectively.

The leakage in the TI layer results from the conductance of topologically trivial and nontrivial surface states as well as the bulk conductivity resulting from unavoidable self-doping effects [58]. Attempts to suppress bulk conductivity include thinning the TI layer until the surface contribution dominates or use of compensation doping to suppress free carriers in the bulk. For example, in the work reported in Ref. [59], copper doping was used in Bi_2Se_3 films to fully suppress bulk states and decouple the surface states in samples as thin as 20 nm. A sheet resistance of approximately 1000 $\Omega/\square$ at room temperature (300 K) was experimentally measured in a 20-nm-thick Bi_2Se_3 film, while the sheet resistance increased to 1400 and 3000 $\Omega/\square$ in films of thickness 10 and 2 nm, respectively, in the same sample. More recently, sheet resistances on the order of tens of kilo-ohms per square have been experimentally achieved at room temperature in 5–60-nm-thick Bi_2Se_3 films grown on an insulating $In_2Se_3/(Bi_{0.5}In_{0.5})_2Se_3$ buffer layer on sapphire substrates [60].

The time-domain response of the output voltage, obtained by our solving Kirchoff's laws in the circuit shown in Fig. 4, is given as

$$V_{\rm out}(t) = V_f\left(1 - e^{-\frac{t}{\tau_{\rm eq}}}\right) + V_i e^{-\frac{t}{\tau_{\rm eq}}}, \tag{16a}$$

$$V_f = \frac{\Delta G}{G_{\rm t}}\frac{V_{\rm read}}{1 + R_{\rm int}G_{\rm TI}} = \nu V_{\rm read}, \tag{16b}$$

$$\tau_{\rm eq} = \underbrace{\frac{1 + R_{\rm int}G_t}{G_t\,(1 + R_{\rm int}G_{\rm TI})}}_{R_{\rm eq}} C_{\rm out}, \tag{16c}$$

where $\Delta G = G_{\rm P} - G_{\rm AP}$, $G_t = G_{\rm P} + G_{\rm AP}$, and V_f and V_i are the final and initial voltages, respectively, at the output node. At the end of the read or write cycle, the voltage $V_{\rm out}$ is reset to 0 V. Therefore, for all results presented in this paper, $V_i = 0$ V. The minimum read voltage required on the MTJ stack to ensure correct functionality is obtained by our equating Eqs. (15) and (16). Assuming that the read pulse duration is significantly greater than $\tau_{\rm eq}$, $V_{\rm read}^{\rm min}$ is given as

$$V_{\rm read}^{\rm min} = (1 + R_{\rm int}G_{\rm TI})\frac{G_t}{\Delta G}V_{\rm in}^{\rm min}. \tag{17}$$

In Fig. 5, the ratio of the minimum read voltage to the minimum input voltage is plotted as a function of the TMR of the MTJ in the VTOPSS. The values of the TMR and the *RA* are taken from Ref. [61] and are reproduced in the inset in Fig. 5. As the *RA* increases, the TMR increases in proportion and saturates at approximately 350% for *RA* greater than 1000 $\Omega\,\mu{\rm m}^2$. The minimum read voltage needed to reliably read the state of the VTOPSS is approximately $2V_{\rm in}^{\rm min}$ for TMR in excess of 200% (dotted line in the main plot). Assuming $V_{\rm in}^{\rm min} \approx 15$ mV (JN limit), $V_{\rm read}^{\rm min} \approx 30$ mV. While the cross-section area of the MTJ does not affect the $V_{\rm read}^{\rm min}/V_{\rm in}^{\rm min}$ ratio, the values of G_t and ΔG are affected significantly by the MTJ cross-section area as shown in the inset on the right-hand side in Fig. 5.

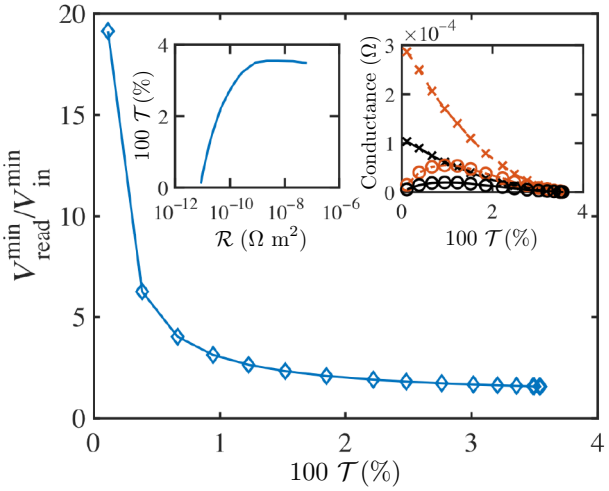

FIG. 5. Ratio of the minimum read voltage to the minimum input voltage as a function of the TMR. The left inset shows the scaling of the TMR with the *RA* (experimental data taken from Ref. [61]). The right inset shows the impact of the TMR on the total conductance (G_t) and the differential conductance (ΔG) of the MTJ for two values of the cross-section area, $\mathcal{A}_{\rm MTJ} = 30 \times 30$ nm^2 (solid line) and 50×50 nm^2 (dashed line). Increasing the MTJ cross-section area increases all conductance values without affecting the ratio of the minimum read voltage and the minimum input voltage.

E. Energy dissipation

The total energy dissipation consists of the energy required to charge and discharge the output node voltage, $V_{\rm out}$, and the direct path conduction between V^+ and V^-. Assuming that the read phase lasts for time $\tau_{\rm pulse}$, the energy supplied by the voltage V^+ is given by the following integral:

$$E_{\rm read} = \int_0^{\tau_{\rm pulse}} dt I_1(t)V^+ = \int_0^{\tau_{\rm pulse}} dt[I_2(t) + I_3(t)]V^+, \tag{18}$$

where $I_j(t)$ (j = 1,2,3) denotes the electric current flowing in the jth branches as shown in Fig. 4, $I_2(t) = G_{\rm AP}[V_1(t) - V^-]$, and $I_3(t) = C_{\rm out}dV_{\rm out}(t)/dt + G_{\rm TI}V_{\rm out}(t)$, where $C_{\rm out} = C_{\rm TI} + C_{\rm int}$ is the net capacitive

loading at the output node. By our substituting $V_1(t)$ in terms of $V_{\rm out}(t)$ and using Eq. (16), the energy dissipation of the circuit is given by Eq. (19):

$$E_{\rm read} = \underbrace{V_{\rm read}^2 G_{\rm AP}\tau_{\rm pulse}\left[1+\nu(1+R_{\rm int}G_{\rm TI})\zeta\right]}_{E_{\rm read,1}} + \underbrace{\nu V_{\rm read}^2 G_{\rm TI}\tau_{\rm pulse}\zeta}_{E_{\rm read,2}} + \underbrace{\nu V_{\rm read}^2 C_{\rm out}\left(1+G_{\rm AP}R_{\rm int}\right)\left(1-e^{-\tau_{\rm pulse}/\tau_{\rm eq}}\right)}_{E_{\rm read,3}}, \quad (19)$$

where

$$\zeta = \left[1 - \frac{\tau_{\rm eq}}{\tau_{\rm pulse}} + \frac{\tau_{\rm eq}}{\tau_{\rm pulse}}\exp\left(-\frac{\tau_{\rm eq}}{\tau_{\rm pulse}}\right)\right].$$

The term $E_{\rm read,1}$ in Eq. (19) is dominated by the energy dissipation due to the MTJ leakage. The second term, $E_{\rm read,2}$, is due to electric conduction through the TI, while the third term, $E_{\rm read,3}$, is due to the energy consumed in charging and discharging the output-node capacitance.

To reduce the leakage through the MTJ, G_t should be lower for a fixed TMR. Unfortunately, this will increase $\tau_{\rm eq}$ and therefore the net delay of the VTOPSS. For example, for $r_{\rm int} = 1.25\times10^7\ \Omega/{\rm m}$, $L_{\rm int} = 100$ nm, TMR of 222%, RA of $4.6\times10^{-11}\ \Omega\,{\rm m}^2$, $\mathcal{A}_{\rm MTJ} = 50\times50\,{\rm nm}^2$, and $C_{\rm out} = 0.1$ fF, $\tau_{\rm eq}\approx 1.85$ ps. For TMR of 350% and RA of $2.2\times10^{-9}\ \Omega\,{\rm m}^2$, $\tau_{\rm eq}$ increases to approximately 89 ps. In the latter case, the charging time of the output capacitance will be comparable to the reversal delay of the MI layer and cannot be ignored. The parameter ζ in Eq. (19) will reduce below unity when $\tau_{\rm eq}\sim\tau_{\rm MI}$ (see the discussion in Sec. IV A).

F. Dimensional scaling

The scaling of the performance metrics of the device with its dimensions depends on the interface area, $\mathcal{A}_{\rm int}$, which depends on the integration scheme adopted for the device (see layout options in Fig. 2.) Table I shows the scaling of the MI reversal delay and the energy dissipation due to leakage for vertically integrated (option A) and laterally integrated (option B) device layouts. We assume that even as the cross-section dimensions of the MI layer are scaled, the energy barrier is fixed so that the thermal stability of the MI layer is not compromised with scaling. For a fixed value of the uniaxial energy density, this can be achieved by appropriate variation of the thickness of the MI layer. Table I shows that for both layouts the speed of the writing mechanism in the VTOPSS scales inversely with a relevant length scale. This length scale is the length of the MI layer (easy axis) for option A, in which layers are stacked vertically. In option B, the relevant length scale is equal to the length of the TI layer. Likewise, the energy dissipation scales inversely with the width of the MI layer for option A and with the width of the TI layer for option B. Even though for both layouts the performance (delay and energy) scales inversely with an appropriate dimension, option B would be preferred due to its smaller footprint. In this layout the spin torque acts nearly uniformly across the cross-section area of the MI layer, promoting (or leading to) a more-uniform (or more-coherent) magnetization reversal.

IV. PERFORMANCE BENCHMARKING

To benchmark the performance of the VTOPSS against CMOS and existing spin-based devices, we first study the impact of device design on VTOPSS latency, energy, and EDP. Results are reported only for the vertically integrated device layout. For all results, $\tau_{\rm pulse} = \tau_{\rm MI} + \tau_{\rm eq}$. Simulation parameters for all benchmarks are listed in Table II unless otherwise noted. For CMOS logic at the 2020 International Technology Roadmap for Semiconductors (ITRS) technology node, the effect of local interconnects (copper low-κ) on the performance metrics is considered.

A. Latency and energy dissipation

In Fig. 6 the reversal delay of the MI layer and the total delay of the VTOPSS are plotted versus the read voltage on the MTJ. We assume a stochasticity parameter $\eta_{\rm st} = 10$ to guarantee a switching error rate as low as 10^{-7}. Our results show that sub-500-ps reversal delay of the MI layer can be achieved with $V_{\rm read}\gtrapprox 150$ mV for $\sigma_{\rm SHC} = 2\times10^5\ (\Omega\,{\rm m})^{-1}$ and spin-coupling efficiency of 100%. A major reduction in delay results from the use of a TI material with a larger spin Hall conductivity. At a read voltage of 150 mV and $\sigma_{\rm SHC} = 5\times10^5\ (\Omega\,{\rm m})^{-1}$, the MI reversal

TABLE I. Performance scaling for the device layouts depicted in Fig. 13. In option A, layers are vertically stacked, while in option B, layers are placed laterally. The energy dissipation due to the MTJ leakage scales as $E_{\rm MTJ}\propto\mathcal{A}_{\rm MTJ}/\min(L_{\rm MI},L_{\rm TI})$.

Layout	Interface area	Delay (E_b fixed)	Energy (TI leakage)
Option A	$\mathcal{A}_{\rm int} = W_{\rm MI}L_{\rm MI}$	$\tau_{\rm MI}\sim\frac{1}{L_{\rm MI}}\left(\frac{W_{\rm TI}}{W_{\rm MI}}\right)$ $\tau_{\rm MI}\sim\frac{1}{L_{\rm MI}}$ if $W_{\rm TI}$ and $W_{\rm MI}$ are scaled proportionately	$E_{\rm TI}\sim\frac{1}{W_{\rm MI}}\left(\frac{L_{\rm TI}}{L_{\rm MI}}\right)$ $E_{\rm TI}\sim\frac{1}{W_{\rm MI}}$ if $L_{\rm TI}$ and $L_{\rm MI}$ are scaled proportionately
Option B	$\mathcal{A}_{\rm int} = W_{\rm TI}L_{\rm TI}$	$\tau_{\rm MI}\sim\frac{1}{L_{\rm TI}}$	$E_{\rm TI}\sim\frac{1}{W_{\rm TI}}$

TABLE II. Material parameters used for conducting simulations and performance benchmarking considering a vertically integrated device layout.

Parameter	Value
Magnetic insulator	
Energy barrier, E_b	$30k_BT$
Uniaxial magnetic anisotropy field, H_K	0.1 T
Gilbert damping coefficient, α	3×10^{-3}
Stochasticity parameter, η_{st}	10 (300 K); 2.6 (0 K)
Width of the MI layer, W_{MI}	50 nm
Length of the MI layer, L_{MI}	100 nm
Topological insulator	
Spin Hall conductivity, σ_{SHC}	$5 \times 10^5 \hbar/2e\ (\Omega\,\mathrm{m})^{-1}$
Sheet resistance of the TI, R_{sheet}	100 k$\Omega/\square$
Relative dielectric permittivity of the TI, ϵ_r	110
Efficiency of spin coupling at the TI-MI interface, ε	1.0
Width of the TI layer, W_{TI}	100 nm
Length of the TI layer, L_{TI}	100 nm
Interconnect and magnetic tunnel junction	
Effective resistivity of the interconnect, ρ_{eff}	$2.5 \times 10^{-6}\ \Omega\,\mathrm{m}$
Capacitance per unit length of the interconnect, c_{ic}	1.6 pF/cm
Interconnect length, L_{ic}	100 nm
Interconnect width, W_{ic}	50 nm
Interconnect thickness, $t_{ic} = 2W_{ic}$ (aspect ratio 2)	100 nm
Resistance-area product of the MTJ	$2.2 \times 10^{-9}\ \Omega\,\mathrm{m}^2$
Tunneling magnetoresistance of the MTJ	350%
Area of the MTJ, $\mathcal{A}_{MTJ}$	$50 \times 50\ \mathrm{nm}^2$

delay is approximately 273 ps for 100% spin-coupling efficiency. The effect of spin-coupling efficiency on the delay is examined in the inset in Fig. 6 at $V_{read} = 150$ mV. For a practical spin-coupling efficiency of 50%, the delay of the VTOPSS is approximately 445 ps. Further reduction in delay can be achieved if the leakage through the MTJ stack is eliminated by fabrication of MTJs with a higher TMR. Finally, as shown in Table I, increasing the length of the MI layer can help reduce the delay further; however, this reduction comes at the cost of lower device integration density.

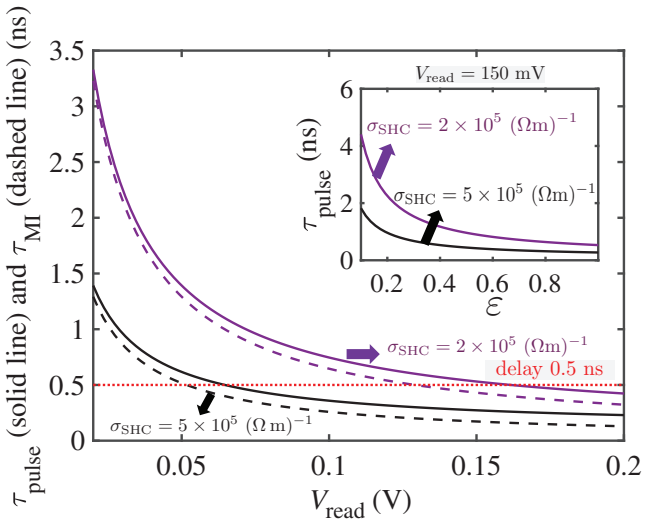

FIG. 6. Switching delay of the VTOPSS read voltage for various values of the spin Hall conductivity, σ_{SHC}, of the TI layer. We choose spin-coupling efficiency $\varepsilon = 100\%$. Other simulation parameters are given in Table II. The inset shows the impact of ε on the total delay of the device.

The effect of read voltage on the energy and EDP of the device is shown in Figs. 7(a) and 7(b). The total energy dissipation scales nearly quadratically with the read voltage. While $E_{read,3}$ scales as V_{read}^2, the product of τ_{pulse} and ζ is nearly independent of V_{read}, which also makes the dominant components of energy dissipation (i.e., due to the TI and MTJ leakage) scale as V_{read}^2 [see Fig. 7(c)]. Unlike CMOS technology, where the relationship between energy dissipation and supply voltage is exactly quadratic, in the case of the VTOPSS, the relationship depends on the values of various material and geometrical parameters of the device. For $\tau_{eq} \sim \tau_{pulse}$, E_{read} scales as V_{read}^2; however, the relationship changes to linear (i.e., $E_{read} \sim V_{read}$) for $\tau_{eq} \ll \tau_{pulse}$. At a read voltage of 150 mV, the energy dissipation of the VTOPSS for infinite sheet resistance (gapped surface states and negligible bulk conductivity) is as low as 3.5 aJ if the spin-coupling efficiency at the TI-MI interface is 100%. This energy dissipation increases by 2–3 orders of magnitude for Bi_2Se_3 thin films with a sheet resistance of 1–10 k$\Omega/\square$ measured at room temperature as reported in Ref. [59]. The EDP of the VTOPSS increases with increase of the MTJ read voltage. At 150 mV, the

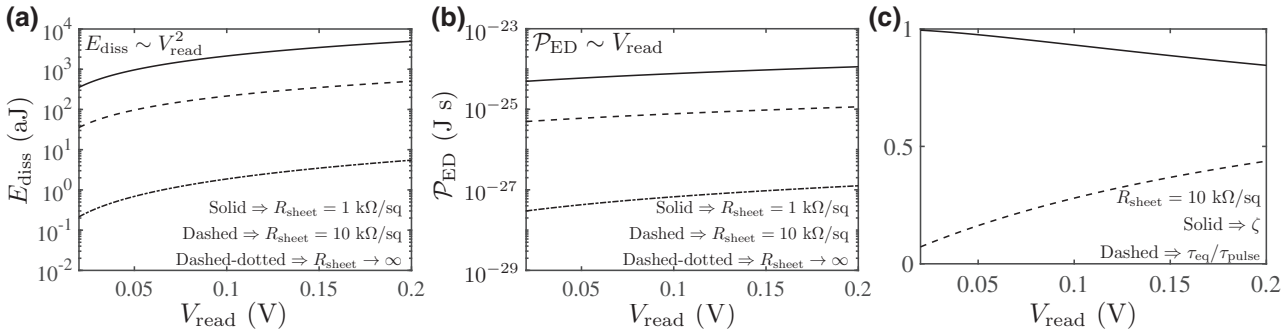

FIG. 7. Effect of read voltage on (a) energy dissipation, (b) EDP, and (c) $\tau_{\rm eq}$ and ζ.

EDP decreases from 9.5×10^{-26} J s at $R_{\rm sheet} = 10$ kΩ/□ to 9.5×10^{-28} J s when there is no leakage through the TI.

Figure 8 shows the contribution of various terms in Eq. (19) to the overall VTOPSS energy dissipation. For large TI conductance, corresponding to a large value of the sheet conductance of the TI, the net energy dissipation is limited by the TI leakage [$E_{\rm read,2}$ in Eq. (19)]. Assuming that the TI conductance can be suppressed such that $G_{\rm sheet} \to 0$, we see that the energy dissipation is limited by the MTJ leakage [$E_{\rm read,1}$ in Eq. (19)] for low values of the TMR and RA, while for large values of the TMR and RA, both MTJ leakage and charging of the output capacitance will limit the total energy of the VTOPSS. The energy associated with charging or discharging output-node capacitances remains well under 2 aJ for all cases considered here ($C_{\rm out} = 113$ aF), and is significant only when both $G_{\rm TI}$ and $G_{\rm AP}$ are low [Fig. 8(b)].

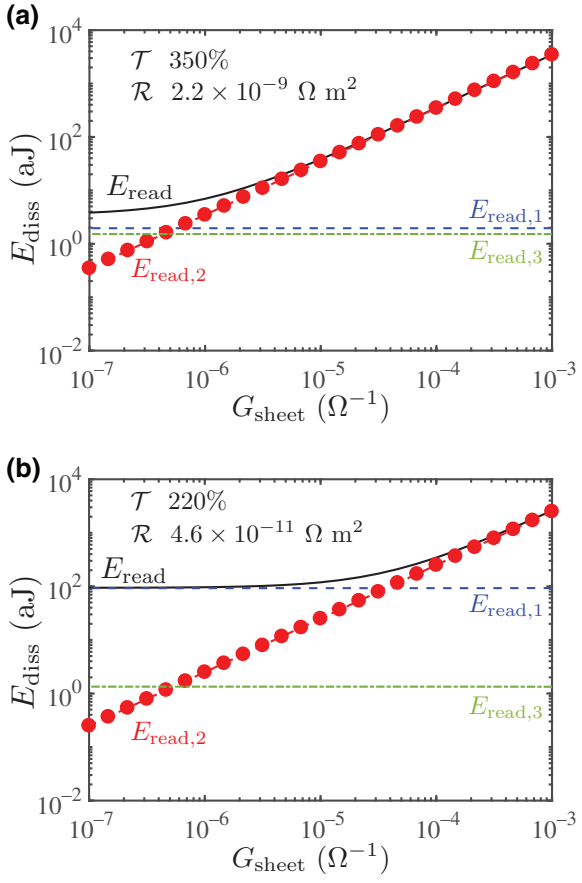

FIG. 8. Energy dissipation versus sheet conductance of the TI for (a) large and (b) small RA and TMR at $V_{\rm read} = 150$ mV.

B. Effect of MTJ design on EDP

One can reduce the EDP of the VTOPSS by designing junctions that exhibit a large TMR—an increase in TMR at a fixed RA reduces both the switching delay and the energy dissipation. As shown in Fig. 9(a), the scaling of the EDP with TMR in the VTOPSS can be expressed as $\mathcal{P}_{\rm ED} \propto 1/\mathcal{T}^b$, where the value of the exponent b, typically in the range from -0.5 to -1, depends on the material and geometrical parameters of the device.

As shown in Fig. 9(b), the EDP initially decreases with an increase in the RA. With further increase in the RA, the EDP exhibits the reverse trend and begins to increase. For RA less than the optimal value, the EDP is inversely proportional to the RA. Beyond the optimal RA, unfortunately the delay associated with charging/discharging capacitive nodes becomes much larger than the MI reversal delay. The optimal RA depends on the material and geometry of the device. For the results shown in Fig. 9, the optimal RA decreases with a reduction in $R_{\rm sheet}$. Moreover, the EDP-RA contour becomes flatter around the optimal point as $R_{\rm sheet}$ reduces. The results show that at a TMR of 600% and without any leakage through the TI, the optimal EDP of the VTOPSS is around 4×10^{-28} J s at $V_{\rm read} = 50$ mV and 8×10^{-28} J s at $V_{\rm read} = 150$ mV. For the same parameters, the energy dissipation and the delay of the VTOPSS are 0.9 aJ (5 aJ) and 486 ps (192 ps), respectively, at $V_{\rm read} = 50$ mV (150 mV). In typical MTJs, TMR increases with increasing RA, which can be harnessed to reduce the EDP of the VTOPSS. In Ref. [61], it was shown that a TMR of 600% can be obtained with a RA of 10^4 Ω μm^2 in (Co,Fe)B/MgO/(Co,Fe)B-type MTJs by annealing the structure above 500 °C. For applications involving STT

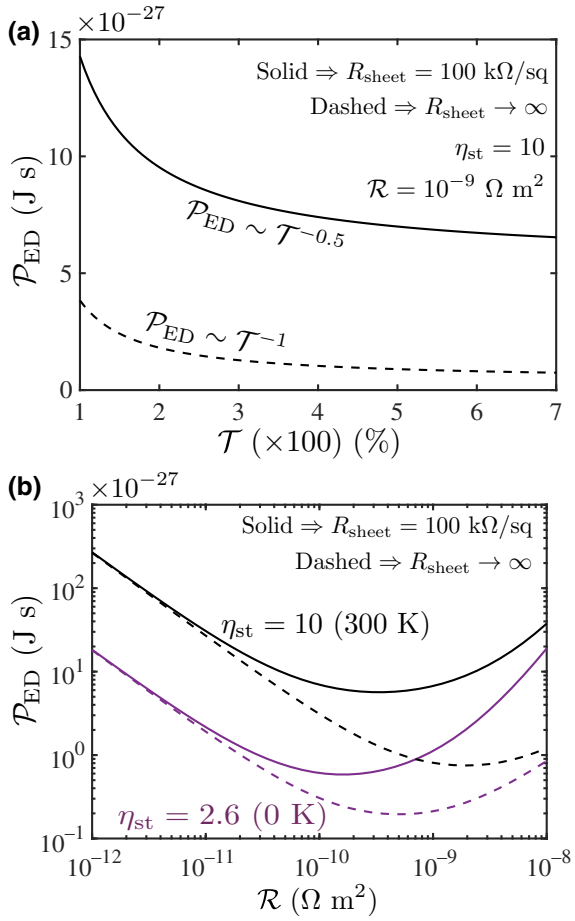

FIG. 9. Effect of (a) TMR and (b) *RA* on the EDP of the VTOPSS at $V_{\text{read}} = 150$ mV. For (b), TMR is 600%.

magnetic RAM, a large *RA* is undesirable as it increases the voltage required to switch the magnetization state via current-induced spin torques [62]. In the case of VTOPSS technology, the MTJ cell is used only to generate a rather low output voltage that must be sufficient to switch the subsequent logic stage. As such, a large *RA* of the read unit on the MTJ stack may be beneficial for the design of a VTOPSS.

C. Interconnect considerations

To transmit information between VTOPSS logic, conventional CMOS-compatible metallic interconnects, such as copper low-κ or aluminum, can be used. From examination of Eq. (16), the effect of interconnect resistance on the device performance appears in the time constant τ_{eq} for charging and discharging the output-node capacitance. In Fig. 10(a), we study the effect of interconnect length on limiting the net delay of the VTOPSS. For very low read voltages, the MI time constant dominates, allowing us to ignore the interconnect impact for interconnects as long as a few micrometers [solid line in Fig. 10(a)]. However, as we increase the read voltage, allowing faster reversal of the MI layer, interconnects as short as a few hundred nanometers become important in quantifying the performance metrics of the device. The maximum interconnect length that can be tolerated for $\tau_{\text{eq}} \lesssim \tau_{\text{MI}}$ is given as

$$L_{\text{ic}}^{\text{max}} = \left(\frac{G_{\text{TI}}\tau_{\text{MI}}}{2c_{\text{ic}}} - \frac{1}{2r_{\text{ic}}G_t}\right) + \sqrt{\left(\frac{c_{\text{ic}} - r_{\text{ic}}G_tG_{\text{TI}}\tau_{\text{MI}}}{2r_{\text{ic}}c_{\text{ic}}G_t}\right)^2 + \frac{\tau_{\text{MI}}}{r_{\text{ic}}c_{\text{ic}}}}. \quad (20)$$

For $L_{\text{ic}} > L_{\text{ic}}^{\text{max}}$, τ_{eq} exceeds τ_{MI}. As shown in Fig. 10(b), as $\rho_{\text{eff}} \to 0$, the time-constant $\tau_{\text{eq}} \to G_t^{-1}C_{\text{out}}$. For finite leakage through the TI, the maximum interconnect length is limited to approximately 1 μm for ρ_{eff} up to 10^{-5} Ω m. For negligible TI leakage ($R_{\text{sheet}} \to \infty$), the effect of the interconnect is largely suppressed, implying that highly resistive and long interconnects up to several hundreds of micrometers can be used in VTOPSS technology without negatively impacting the overall performance. As a result,

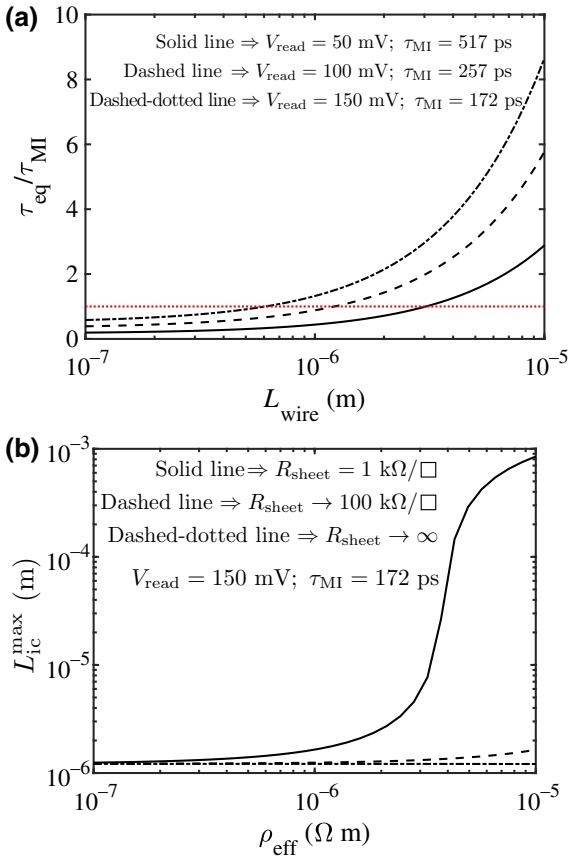

FIG. 10. (a) Impact of interconnect length on the time constant τ_{eq}, which quantifies the charging or discharging rate of the output-node capacitance. (b) Maximum interconnect length that yields $\tau_{\text{eq}} = \tau_{\text{MI}}$. For interconnects longer than $L_{\text{ic}}^{\text{max}}$, the charging/discharging time of the output node exceeds the MI reversal delay.

there exists a wide range of interconnect options, such as copper, ultrascaled wires (wire width much less than the electron mean free path), and doped semiconducting wires, to design VTOPSS logic.

D. Comparison against existing logic devices

1. CMOS metrics

The model used for computing the performance metrics of CMOS technology comprises a minimum-sized CMOS inverter driving a similarly sized load through a copper, low-κ interconnect. With the Elmore delay model, the delay of the CMOS circuit is given as [63]

$$\tau_{\mathrm{CMOS}} = 0.69 R_{\mathrm{S}} \left(C_S + C_L\right) + 0.69 \left(R_S c_{\mathrm{ic}} + r_{\mathrm{ic}} C_L\right) L_{\mathrm{ic}} + 0.38 r_{\mathrm{ic}} c_{\mathrm{ic}} L_{\mathrm{ic}}^2, \quad (21)$$

where R_S and C_S are the source resistance and capacitance, respectively, and C_L is the load resistance (assumed to be equal to C_{S}). The energy dissipation of the CMOS circuit is given as

$$E_{\mathrm{CMOS}} = \left(C_S + C_L + c_{\mathrm{ic}} L_{\mathrm{ic}}\right) V_{\mathrm{DD}}^2, \quad (22)$$

where V_{DD} is the supply voltage.

The CMOS-device metrics are taken from the ITRS for the 2020 technology node (half pitch of metal 1 of 18 nm). For a minimum-sized inverter, $R_S \approx 78$ kΩ, $C_S = 0.68$ fF/μm, $C_L = 0.38$ fF/μm, $\rho_{\mathrm{eff}} = 25$ $\mu\Omega$ cm, $c_{\mathrm{ic}} = 1.6$ pF/cm, and the interconnect aspect ratio is 2 [64]. The delay of the CMOS circuit resulting from omission of the interconnect-related delay is approximately 1.1 ps at an energy dissipation of 10 aJ per bit. This yields an EDP of 1.1×10^{-29} J s. For an interconnect length of 100 nm, the delay of the CMOS circuit is 2.1 ps at an energy dissipation of 20 aJ per bit and an EDP of 4.2×10^{-29} J s.

2. CMOS scaling

To study CMOS scaling over process nodes, we consider only the intrinsic delay of a CMOS transistor: $\tau_{\mathrm{CMOS}} = C_{\mathrm{par}} V_{\mathrm{DD}} / I_{\mathrm{DSAT}}$ (drain saturation), where V_{DD} is the supply voltage and C_{par} and I_{DSAT} are the parasitic capacitance and the maximum *on* current, respectively, of the transistor. At the same technology node, increasing the transistor width does not change its intrinsic delay as both C_{par} and I_{DSAT} are proportional to the device width. If we consider different technology nodes from ITRS, we see that the switching delay of CMOS transistors is roughly the same as the minimum feature size scales from 17.9 nm (year 2020) to 8.9 nm (year 2026), as shown in Fig. 11. This scaling is consistent with the fact that the on-chip clock frequencies have not increased over the last several years with scaling.

The intrinsic energy dissipation of CMOS transistors is given as $E_{\mathrm{CMOS}} = C_{\mathrm{par}} V_{\mathrm{DD}}^2$. At the same technology node, increasing the transistor width will increase its energy dissipation due to the increase of the parasitic capacitance. This is contrary to the scaling of energy with dimensions in the VTOPSS technology (see Table I). To interpret E_{CMOS} across technology nodes, we use ITRS projections for the years 2020–2026. ITRS data indicate that $C_{\mathrm{par}} \sim W^{1.37}$ and $V_{\mathrm{DD}} \sim W^{0.2}$ (W is the transistor width.) Therefore, as the CMOS technology scales, its intrinsic energy dissipation decreases. The results in Fig. 11 show this scaling behavior. However, the rate of decrease of energy dissipation tends to slow down towards the ITRS year 2024 with a minimum feature size of 11.3 nm.

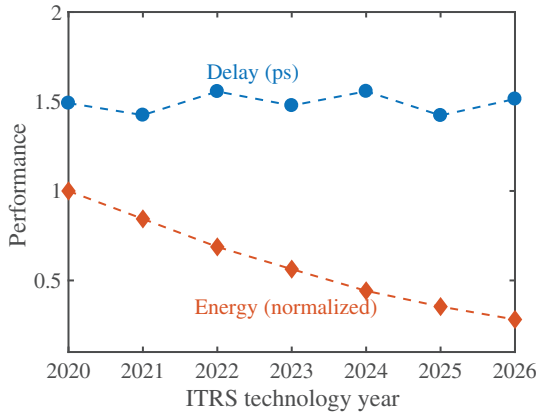

FIG. 11. Scaling of the delay and energy dissipation of a silicon transistor with technology year. The data are taken from the 2013 ITRS update.

3. Spin-based devices

Existing spin-based devices that are considered for comparison include ASL [65], CSL [66], and MESO logic [51] devices. ASL uses filtering of electric current through a nanomagnet to generate spin-polarized current, which communicates spin information between input-output nanomagnets via a nonmagnetic conductor (e.g., copper, aluminum) that serves as the interconnect. Unlike charge current, spin current is not conserved; therefore, the design of interconnects in ASL requires careful consideration [67]. On the other hand, CSL uses the spin Hall effect to convert electric current carrying information into spin-polarized current, which is used to switch the state of an input nanomagnet. The orientation of the input nanomagnet is communicated to an output nanomagnet via their mutual magnetic dipolar coupling. The magnetization state of the output nanomagnet is read through a MTJ, which generates an output electric current with the polarity and amplitude dependent on the orientation of the output nanomagnet and the voltage applied on the MTJ. Since information is communicated via electric current, there is no loss of information in the interconnect. However, because of the flow of electric current through a

heavy-metal layer with a high effective resistivity, CSL has high Joule heating. The MESO logic device, recently proposed in Ref. [51], uses magnetoelectric transduction to convert electric current into spin current at the input side, while spin-orbit coupling is used at the output end for spin-to-charge transduction. That is, the input and output state variables are encoded in electric current. Benchmarking activities have shown that magnetoelectric mediated spin devices have energy dissipation comparable to that of CMOS devices [8].

Table III shows the performance metrics of the VTOPSS in comparison with spin-based devices. The performance of the VTOPSS exceeds that of existing spin-based devices. The performance metrics of the ASL and MESO logic devices in Table III do not include switching and write errors and can be considered to be representative of operation at 0 K. The performance metrics of the CSL device reported in Ref. [31] assume ideal dipolar coupling between the read and write magnets and ignore switching errors. The physics of magnetic dipolar coupling and its impact on the reliability of CSL device is reported in Refs. [68,69]. In Ref. [70] and noted in Table III, performance estimates of the CSL device are obtained in the presence of practical dipolar coupling with $e_{b0} = 5$ and $\mathcal{P}_{\rm err} = 0.05$. The energy dissipation of the VTOPSS is 100 times lower than that of ASL and CSL devices, while the delay of the VTOPSS is 2–10 times lower than that of ASL and CSL devices, respectively. The delay of the VTOPSS is comparable to that of the MESO logic device and can be reduced further by use of MI layers with lower damping and/or MI switching via precessional dynamics. In terms of energy dissipation, the VTOPSS performs slightly better than the MESO logic device. The energy dissipation can be further reduced through material optimization, particularly with a higher TMR and *RA* of the MTJ used for sensing the state of the MI layer in the VTOPSS.

V. UNIVERSAL BOOLEAN LOGIC IMPLEMENTATION

A complete set of two-input Boolean functions can be implemented with use of the schematic shown in Fig. 12, where V_A and V_B refer to primary signal inputs and V_X denotes the tie-breaking input signal. To change the functionality between true and complementary outputs, the polarity of the supply voltage signals on the MTJ is swapped. To implement a NAND gate, V_X is set to its negative value, while for a NOR gate, V_X is set to its positive voltage. For XOR and XNOR functionality, one of the primary inputs is applied as a voltage signal on the TI, while

TABLE III. Overview of performance metrics of various spin-based devices. The performance metrics of the VTOPSS exceed those of existing spin-based technologies. The EDP of low-power CMOS technology at the 2020 ITRS technology node is approximately 4×10^{-29} J s (see the text for calculations). For ASL and MESO logic devices, the energy barrier of the magnet is $40k_BT$ and the variation in their performance due to thermal noise is ignored; therefore, their performance is representative of results at 0 K. For the CSL device, the performance is reported at 95% accuracy of computation using magnets with an energy barrier of $5k_BT$. The physics of dipolar coupling is included according to Refs. [68,69]. For the VTOPSS, the write-error probability is 10^{-7} at 300 K, while the thermal stability is 3.4×10^4 s. The energy dissipation and EDP of the VTOPSS can be reduce by an order of magnitude by suppression of leakage through the TI.

Metric	ASL [50]	CSL [70]	MESO logic [51]	VTOPSS (this work)	
				$V_{\rm read} = 0.15$ V (300 K/0 K)	$V_{\rm read} = 0.05$ V
Input-output	Voltage	Electric current	Electric current	Voltage	
Transduction	$V \rightarrow \mathbf{m} \rightarrow I_{\rm spin} \rightarrow \mathbf{m} \rightarrow V$	$I_{\rm elec} \rightarrow \mathbf{m} \rightarrow I_{\rm elec}$	$I_{\rm elec} \rightarrow \mathbf{m} \rightarrow I_{\rm elec}$	$V \rightarrow \mathbf{m} \rightarrow V$	
Energy per bit	0.34 fJ[a]	1.31 fJ	27 aJ	38 aJ/16 aJ	10 aJ/3.5 aJ
Switching delay	0.5 ns	3 ns	250 ps[b]	272 ps/145 ps	617 ps/235 ps
Energy-delay product (J s)	17×10^{-26}	3.9×10^{-24}	6.75×10^{-27}	$10^{-26}/2.3 \times 10^{-27}$	6.3×10^{-27} 8.3×10^{-28}
Area	3.8×10^{-3} μm^2	1.6×10^{-3} μm^2	1.4×10^{-2} μm^2	$(1-2) \times 10^{-3}$ μm^2[c] $(1-2) \times 10^{-2}$ μm^2[d]	
Fan-out	No	Yes	Yes	Yes	

[a]Results for perpendicular-magnetic-anisotropy magnets.
[b]Total pulse width reported in Ref. [51].
[c]Conservative estimate for a vertically integrated device.
[d]Estimate reported for a laterally integrated device assuming the areas of the TI layer and the MTJ are 100×100 nm^2 and the spacing between the TI and the MTJ is 50 nm.

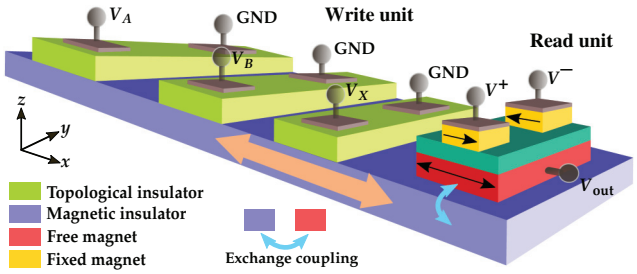

FIG. 12. All two-input Boolean logic functions can be implemented with the same device layout. The primary inputs are denoted as V_A and V_B, while the signal V_X denotes the tie-breaking signal to change the Boolean functionality. To switch between inverting and noninverting logic (different polarities of V_{out}), the polarity of the signals V^+ and V^- at the MTJ can be interchanged. GND labels show the ground contacts.

the other primary input serves as the supply voltage on the MTJ in the read unit. In the case of copy-invert functions, the tie-breaking signal V_X is set to 0 V. Alternately, the schematic shown in Fig. 1 can be used for copy and invert Boolean operations. However, by use of a generic layout as in Fig. 12, all 16 Boolean operations possible for two input signals can be implemented directly by permutation of the polarities of the MTJ supply and the control voltage. Another major advantage of the VTOPSS is its ability to support logic locking [71] and encryption at the device level by preventing optical-based reverse-engineering attacks [72]. The innate polymorphism of the VTOPSS will enable runtime reconfigurability where the actual function to be implemented is determined on the fly with a key or control input. Exploration of the resilience of the VTOPSS against existing hardware attacks, prominently those based on the Boolean satisfiability test, will be investigated in future work.

The device layout corresponding to the universal logic gate is shown in Fig. 13, where the device area for a universal gate is approximately 0.06 μm^2, assuming relatively large values of the cross-section areas of the TI-MI interface, MTJ, and the interconnect. The area can be reduced significantly by the patterning of narrower TI

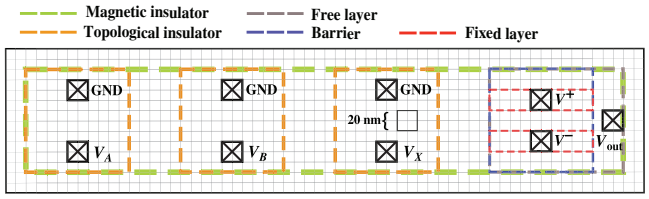

FIG. 13. Device layout for the schematic shown in Fig. 12. Here it is assumed that the cross-section area of the TI layer is 100×100 nm^2 and the spacing between adjacent TI layers is 50 nm. The MTJ cross-section area is the same as that of the TI-MI interface. The total area is approximately 0.06 μm^2. GND labels show the ground contacts.

and MI layers and reduction of the cross-section dimensions of the MTJ. The latter approach, in particular, is advantageous for reducing the device footprint without a negative impact on the device performance metrics.

VI. CONCLUSIONS

Computational electronics can, in principle, be realized with any state variable that is stable over device-relevant timescales, and with any low-loss communication mechanism between devices that allows fan-out. In this regard, storing and manipulating information in magnetic materials is promising. Magnetic materials have a large number of electron spins that are locked together by their exchange interaction such that the reorientation energy per spin to move the magnetization collectively can be on the order of millielectronvolts. Magnetization reversal solely through electric fields is critical toward paving the path for an ultralow-energy computing substrate. The efficiency of voltage-spin conversion must be significantly higher to allow ultralow-voltage operation to be competitive with CMOS technology.

In this paper, a VTOPSS based on a hybrid TI-MI magnetoelectric structure is presented. The device has the following important features: (i) innate polymorphism (i.e., it can implement all 16 two-input Boolean operations using the same layout), (ii) CMOS compatibility (input and output variables are in voltage domain), (iii) extremely large intrinsic gain for charge-to-spin conversion owing to the ultrahigh spin Hall conductivity of the TI material, (iv) ability to support fan-out, (v) sub-10-mV operation with energy of less than 10 aJ per bit, (vi) ability to lower the EDP to on the order of 10^{-29} J s (competitive with CMOS technology), (vii) elimination of electric-current-carrying wires as the operation is fully based on voltage-to-voltage conversion with transmission of information via capacitive charging and discharging of wires, amd (viii) ultralow damping of the MI layer allowing ultrafast operation on the order of a few hundred picoseconds via antidamping spin torque.

We develop analytic models to quantify the performance of the VTOPSS and benchmark the results against existing CMOS and spin-based devices. Our results conclusively show that for the current state-of-the-art material parameters, the VTOPSS exceeds the performance of all-spin logic, charge-spin logic, and magnetoelectric spin-orbit logic devices. Improvements in material parameters and device design can readily facilitate sub-attojoule-energy-per-bit operation with an energy-delay product of approximately 10^{-29} J s for the VTOPSS to be competitive against CMOS devices at the 2020 ITRS technology node. Future work will address important issues pertinent to multidomain effects in both uniaxial and biaxial magnetic insulators and the effects of thermal stochasticity for subcritical excitation. Unlike CMOS devices, the

VTOPSS can also provide logic locking due to the uniform device-level layout that makes it virtually impossible to probe the functionality with reverse-engineering hardware attacks. The ability of the VTOPSS to thwart state-of-the-art Boolean satisfiability attacks is yet to be examined and will be considered in future work.

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