Quantitative Analysis of the Density of Trap States in Semiconductors by Electrical Transport Measurements on Low-Voltage Field-Effect Transistors

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A method for extracting the density and energetic distribution of the trap states in the semiconductor of a field-effect transistor from its measured transfer characteristics is investigated. The method is based on an established extraction scheme [M. Grünewald *et al*., Phys. Stat. Sol. B 100, K139 (1980)] and extends it to low-voltage thin-film transistors (TFTs). In order to demonstrate the significance of this extension, two types of TFTs are fabricated and analyzed: one with a thick gate dielectric and high operating voltage and one with a thin gate dielectric and low operating voltage. From the measured transfer characteristics of both TFTs, the density of states (DOS) is calculated using both the original and the extended Grünewald method. The results not only confirm the validity of the original Grünewald method for high-voltage transistors, but also indicate the need for the extended Grünewald method for the reliable extraction of the trap DOS in transistors with a thin gate dielectric and low operating voltage.

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I. INTRODUCTION

In an ideal crystalline semiconductor, there are no electronic states between the valence-band edge and the conduction-band edge and, therefore, this energy range is called the energy gap [1]. In contrast, the energy gap of polycrystalline or amorphous semiconductors is typically characterized by localized states that arise from structural defects (i.e., static disorder, induced, e.g., by grain boundaries) [2,3]; intentional [4,5] or unintentional [6] impurities; interaction of the charge carriers with polar molecules [7]; and, particularly in van-der-Waals-bonded molecular crystals, from dynamic disorder due to the thermal motion of the molecules [8–10]. These nonidealities lead to localized states in the energy gap of the semiconductor that act as charge-carrier traps. The density and energetic distribution of these localized states [trap density of states (DOS)] strongly influence the electrical characteristics of field-effect transistors based on disordered semiconductors.

When the applied gate-source voltage and, thus, the gate-induced carrier density in the semiconductor are small, most of the charges are trapped deep in the energy gap. When the gate-source voltage is increased, trap states closer to the transport level are gradually filled. The density of trap states therefore affects the subthreshold slope of the transistor, i.e., the slope of the transfer curve in the exponential region below the threshold voltage. For practical applications, this slope should be as steep as possible, ideally close to the room-temperature limit of 58 mV/decade, but a large density of deep trap states will lead to a less steep subthreshold slope. At the same time, as the gate-source voltage is increased, more and more charge carriers reach the transport level where they contribute to the charge transport in the semiconductor.

The origin of the frequently observed electric-field dependence of the effective carrier mobility is often believed to be trap filling and the associated change in the ratio of the densities of localized and delocalized carriers [11,12]. Other field-effect-transistor characteristics affected by the density of trap states are the bias-stress effect [13] and the alignment of the energy levels at the interfaces between the semiconductor and the source and drain contacts [14]. Aside from transistors, the trap DOS also has a critical influence on the charge-transport properties of other electronic devices based on disordered semiconductors, such as organic light-emitting diodes

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(OLEDs), in which trap states can induce the undesirable nonradiative recombination of electrons and holes [15,16], and photovoltaic cells, in which trap states may be beneficial for the separation of the photo-induced excitons, but also detrimental as they may impede the dissociation of formed charge transfer states or disrupt the transport of the separated carriers to the electrodes [17]. The exact analysis of the density and distribution of traps in disordered semiconductors is, thus, an important task, both from a fundamental perspective and from an application point of view.

While the trap DOS cannot be measured directly, it can be accessed indirectly by means of a number of experimental techniques, including photoemission spectroscopy [18,19], Kelvin-probe force microscopy [20,21], electrical transport measurements [22], photoconductivity measurements [23,24], electron spin resonance spectroscopy [25], and capacitance-voltage measurements [26]. In the 1980s, Grünewald *et al*. developed a method, initially intended for thin-film transistors (TFTs) based on hydrogenated amorphous silicon (a-Si:H), to convert a single transfer curve of a field-effect transistor (i.e., the drain current measured as a function of the applied gate-source voltage) to the underlying density-of-states function [27–29]. Over the past decade, the Grünewald method has been employed with great success to calculate the DOS of TFTs based on a wide range of organic semiconductors and fabricated with a variety of device architectures [30–37].

However, in all these previous reports, the Grünewald method was employed exclusively to TFTs with thick gate dielectrics and high operating gate voltages of a few tens of volts. The reason is that the original Grünewald method requires that the potential drop across the semiconductor layer be negligible compared to the potential drop across the gate dielectric, which significantly simplifies the computation but limits the applicability of the method to TFTs with high operating voltages. Here, we explore an extension of the Grünewald method in which this simplification is removed, thus making the method applicable to low-voltage TFTs with very thin gate dielectrics. This extension is an important upgrade, since organic TFTs are generally targeting mobile and wearable electronics applications in which low-voltage operation and, thus, thin gate dielectrics are critical prerequisites. The formalism for this extension was recently introduced by Jeong *et al.* and applied to inorganic TFTs with a 120-nm-thick gate dielectric, but without analyzing the implications of the extension depending on the thickness of the gate dielectric [38]. In contrast, we apply both the original and the extended Grünewald method to organic TFTs with two different gate-dielectric thicknesses and are, thus, able to show that the original Grünewald method is indeed applicable to high-voltage transistors, but not to low-voltage transistors.

II. EXPERIMENT

A. Device fabrication

All TFTs are fabricated in the bottom-gate, top-contact device structure using boron-doped silicon wafers with an electrical resistivity of 0.005 Ω cm as the substrate [39]. For the TFTs with the thick gate dielectric, the doped silicon wafer also serves as the gate electrode. The thick gate dielectric is a stack of three layers: a 100-nm-thick silicon dioxide (SiO_2) layer grown by thermal oxidation in dry oxygen, an 8-nm-thick aluminum oxide (Al_2O_3) layer deposited by atomic layer deposition, and a 1.7-nm-thick self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid. This triple-layer gate dielectric has a total thickness of 110 nm and a unit-area capacitance of 34 nF/cm^2 [39]. For the TFTs with the thin gate dielectric, a 30-nm-thick layer of aluminum is deposited onto the silicon substrate by thermal evaporation in vacuum as the gate electrode. The thin gate dielectric consists of a 3.6-nm-thick aluminum oxide (AlO_X) layer obtained by briefly exposing the surface of the aluminum gate electrode to an oxygen plasma and a 1.7-nm-thick *n*-tetradecylphosphonic acid SAM. This double-layer gate dielectric has a total thickness of 5.3 nm and a unit-area capacitance of 700 nF/cm^2 [40].

For both types of TFTs, a 20-nm-thick layer of the small-molecule organic semiconductor 2,9-diphenyl-dinaphtho [2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DPh-DNTT [41,42]) is deposited by thermal sublimation in vacuum. During the semiconductor deposition, the substrate is held at a temperature of 90°C. Finally, a 30-nm-thick layer of gold is deposited through a polyimide shadow mask (CADiLAC Laser, Hilpoltstein, Germany) to define the source and drain contacts, with a channel width of 200 μm and channel lengths ranging from 10 to 100 μm. Figure 1 shows

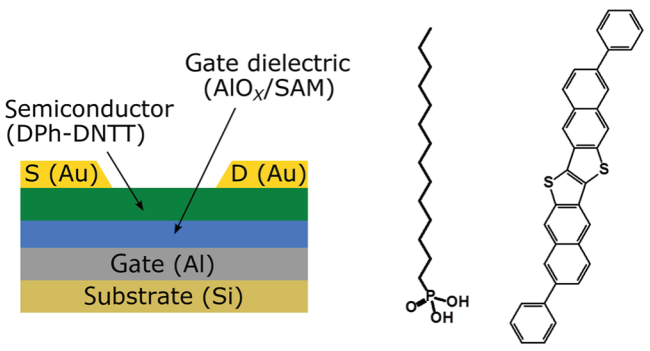

FIG. 1. Schematic cross section of the thin-film transistors with the thin gate dielectric, which consists of a 3.6-nm-thick layer of aluminum oxide (AlO_X) and a 1.7-nm-thick self-assembled monolayer (SAM) of *n*-tetradecylphosphonic acid. The chemical structures of *n*-tetradecylphosphonic acid and of the organic semiconductor 2,9-diphenyl-dinaphtho[2,3-b:2′,3′-f]-thieno[3,2-b]thiophene (DPh-DNTT) are also shown.

the schematic cross section of the TFTs with the thin gate dielectric.

B. Electrical characterization

The current-voltage characteristics of the TFTs are measured in ambient air at room temperature under yellow laboratory light using an Agilent 4156C Semiconductor Parameter Analyzer. The transfer characteristics are measured by applying a drain-source voltage V_{DS} of -2 V to the TFTs with the thick gate dielectric and -0.1 V to the TFTs with the thin gate dielectric and by sweeping the gate-source voltage in steps of -0.75 V (TFTs with the thick gate dielectric) and -50 mV (thin gate dielectric). The drain-source voltages are chosen so that the TFTs are operated in the linear regime.

The effective charge-carrier field-effect mobility μ_{eff} is calculated by fitting the following equation to the measured transfer curve:

$$\mu_{\text{eff}} = \frac{L}{WC_{\text{diel}}V_{\text{DS}}}\frac{\partial I_D}{\partial V_{\text{GS}}}, \tag{1}$$

where I_D is the drain current, L the channel length, W the channel width, C_{diel} the unit-area capacitance of the dielectric and V_{GS} the gate-source voltage.

The subthreshold slope S is calculated by fitting the following equation to the subthreshold region of the measured transfer curve:

$$S = \frac{\partial V_{\text{GS}}}{\partial[\log_{10}(I_D)]}. \tag{2}$$

For the analysis below, the value of the flat-band voltage V_{FB} is required. Following previous publications, we approximate the flat-band voltage as the turn-on voltage V_{on}, i.e., as the gate-source voltage at which the drain current starts to increase sharply above the noise floor when plotted on a logarithmic scale (see Fig. 2) [30].

III. ANALYSIS AND DISCUSSION

A. The original Grünewald method

In the following, a brief summary of the original Grünewald method is provided, including the essential equations and assumptions. More detailed information can be found in the publications by Grünewald *et al.* [27,28] and Kalb *et al.* [30].

The Grünewald method was developed to facilitate the conversion of a single transfer curve of a field-effect transistor recorded in the linear regime of operation (i.e., with a drain-source voltage that is negligibly small compared to the difference between the gate-source voltage and the threshold voltage) to the DOS of the semiconductor. For the original Grünewald method, a number of simplifying assumptions are made:

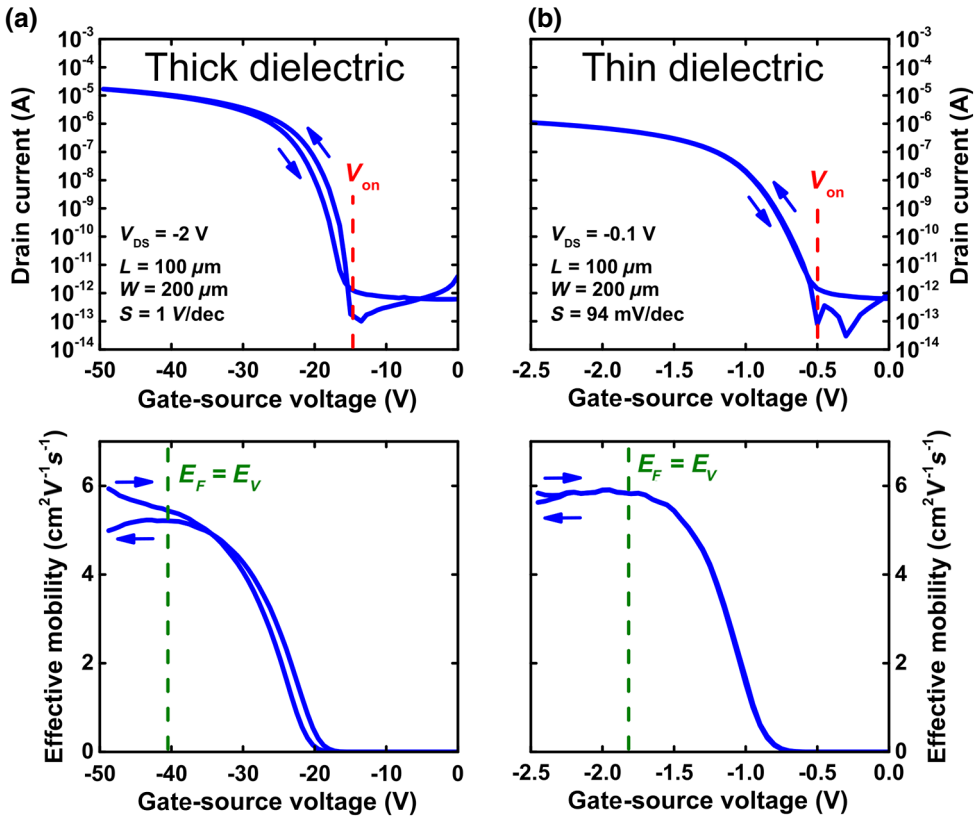

FIG. 2. Transfer curves measured on DPh-DNTT TFTs with a 110-nm-thick gate dielectric (a) and a 5.3-nm-thick gate dielectric (b). The transfer curves are measured in the linear regime of operation. From the transfer curves, the turn-on voltage V_{on} is extracted and taken as the flat-band voltage V_{FB}. The effective carrier mobility μ_{eff} is calculated using Eq. (1) and plotted as a function of gate-source voltage; from this plot, the gate-source voltage at which the mobility saturates is obtained and taken as the gate-source voltage at which $E_F = E_V$, with E_F being the Fermi energy and E_V the valence-band energy. The subthreshold slope S is calculated using Eq. (2).

(1) The gradual channel approximation is valid, i.e., the electric field E_x (created by the gate-source voltage) in the direction perpendicular to the interface between the semiconductor and the gate dielectric is much larger than the electric field E_y (created by the drain-source voltage) parallel to the semiconductor/dielectric interface. This requirement is fulfilled by operating the transistor in the linear regime, i.e., with a small drain-source voltage.

(2) The semiconductor layer is homogeneous in the direction perpendicular to the semiconductor/dielectric interface.

(3) A nonzero flat-band voltage (caused, e.g., by a difference between the work functions of the semiconductor and the gate electrode or by charged states in the gate dielectric) can be taken into account by correcting the applied gate-source voltage for the flat-band voltage: $V_G = V_{GS} - V_{FB}$.

(4) The thickness of the semiconductor layer is larger than the Debye length in the semiconductor, so that the electrostatic potential at the distance d from the semiconductor/dielectric interface (where d is the thickness of the semiconductor layer) is essentially zero.

(5) The potential drop across the thickness of the semiconductor is much smaller than the potential drop across the thickness of the gate dielectric, so that the contribution of the potential drop across the semiconductor layer to the total potential drop of the applied gate-source voltage can be neglected.

(6) The Boltzmann approximation holds for the free charge carriers.

(7) The transfer curve of the transistor is not affected by the contact resistance.

One important advantage of the Grünewald method over other DOS extraction methods is that the Grünewald method does not require any temperature-dependent measurements, as the DOS is calculated from a single transfer curve, which makes it, in principle, possible to investigate the temperature dependence of the DOS [34]. Another advantage of the Grünewald method is that it does not require any abrupt approximations, i.e., it is not necessary to assume that the charge-accumulation layer has a homogeneous charge density or a sharp edge. Instead, the band bending in the semiconductor induced by the gate-source voltage is correctly taken into account. Figure 3 shows a sketch of the band bending in the semiconductor for a gate-source voltage larger than the flat-band voltage. The electrostatic potential at the semiconductor/dielectric interface is called interface potential V_0.

The starting point for the calculation of the gate-induced carrier density is the one-dimensional Poisson equation:

$$\frac{\partial^2 V(x)}{\partial x^2} = \frac{en(x)}{\varepsilon_0 \varepsilon_S}, \tag{3}$$

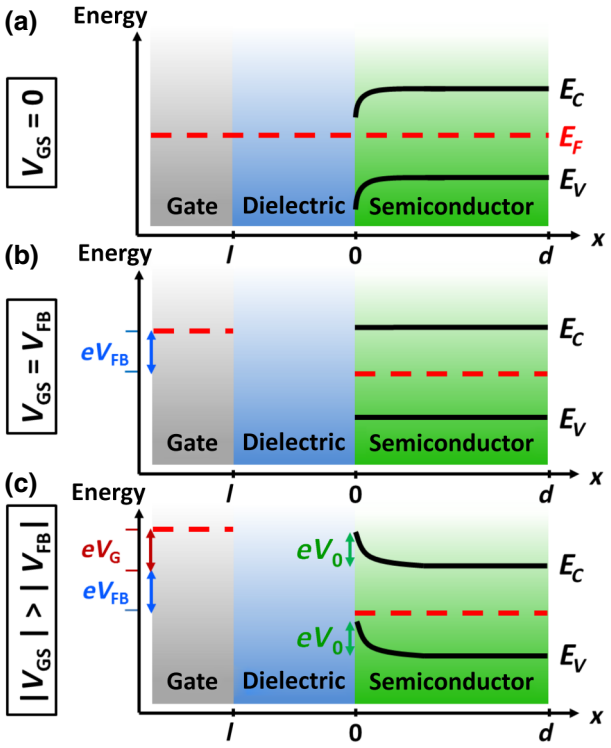

FIG. 3. Schematic cross section of a field-effect transistor showing the relevant energy levels. (a) Initial band bending in the semiconductor in the absence of an applied gate-source voltage. (b) The flat-band voltage V_{FB} is the gate-source voltage necessary to compensate this initial band bending. (c) Applying a gate-source voltage greater than the flat-band voltage ($V_G = V_{GS} - V_{FB}$) induces a band bending in the semiconductor that leads to charge accumulation in the semiconductor in close proximity to the semiconductor/dielectric interface. At this interface, the bands of the semiconductor are shifted by an energy eV_0, with V_0 being the interface potential. E_C and E_V are the conduction- and valence-band energies.

where $V(x)$ is the electrostatic potential at position x, e the elementary charge, $en(x)$ the total charge density (including free and trapped charges as well as ionized acceptors and donors), ε_0 the vacuum permittivity, and ε_S the dielectric constant of the semiconductor. As one of the boundary conditions for the Poisson equation, the following criterion is applied:

$$\varepsilon_0 \varepsilon_{\text{diel}} E_{\text{diel}} = -\varepsilon_0 \varepsilon_S E_S, \tag{4}$$

$$\varepsilon_0 \varepsilon_{\text{diel}} \frac{V_{GS} - V_{FB}}{l} = -\varepsilon_0 \varepsilon_S \left.\frac{\partial V(x)}{\partial x}\right|_{x=0}, \tag{5}$$

where E_{diel} (E_S) is the electric field in the gate dielectric (in the semiconductor) at the semiconductor/dielectric interface and oriented perpendicular to the interface, $\varepsilon_{\text{diel}}$ the dielectric constant of the gate dielectric, and l the thickness of the gate dielectric.

For the calculation of the relation between the interface potential and the gate-source voltage, it is assumed that the current that flows in the accumulation channel parallel to the semiconductor/dielectric interface can be written according to the Boltzmann approximation:

$$I = \frac{I_0}{d}\int_0^d \exp\left(\frac{eV(x)}{k_B T}\right) dx, \tag{6}$$

where I_0 is the current at flat-band conditions, d the thickness of the semiconductor layer, k_B the Boltzmann constant, and T the temperature.

By converting Eq. (6) and applying the first boundary condition (5) and the second boundary condition $V(d) = 0$ (see assumption 4 in the list above), the following differential equation for the interface potential V_0 can be derived:

$$\frac{dV_0}{d(V_{\rm GS} - V_{\rm FB})} = \frac{\varepsilon_{\rm diel} d}{\varepsilon_S l}\frac{1}{I_0}\frac{dI}{d(V_{\rm GS} - V_{\rm FB})} \times \frac{V_{\rm GS} - V_{\rm FB}}{\exp\left(\frac{eV_0}{k_B T}\right) - 1}. \tag{7}$$

The form of this differential equation allows a partial integration to be performed, which yields an equation that implicitly contains V_0 as a function of $V_{\rm GS}$:

$$\exp\left(\frac{eV_0}{k_B T}\right) - \frac{eV_0}{k_B T} - 1 = \frac{e}{k_B T}\frac{\varepsilon_{\rm diel} d}{\varepsilon_S l I_0}\left[(V_{\rm GS} - V_{\rm FB}) \times I(V_{\rm GS} - V_{\rm FB}) - \int_0^{V_{\rm GS}-V_{\rm FB}} I(\tilde{V}_{\rm GS}) d\tilde{V}_{\rm GS}\right]. \tag{8}$$

From Eq. (8), the relation $V_0(V_{\rm GS} - V_{\rm FB})$ can be determined numerically, so that for all gate-source voltages, the interface potential V_0 is known. With this knowledge of V_0, a conversion of the Poisson equation (3) using the first boundary condition (5) and the second boundary condition [$V(d) = 0$] leads to an expression for the total carrier density n:

$$n(V_0) = \frac{\varepsilon_{\rm diel}^2 \varepsilon_0}{\varepsilon_S l^2 e}(V_{\rm GS} - V_{\rm FB})\left(\frac{\partial V_0}{\partial(V_{\rm GS} - V_{\rm FB})}\right)^{-1}. \tag{9}$$

Finally, within the zero-temperature approximation (which requires that the Fermi-Dirac function be a step function), the density-of-states function, which is therefore probed at the energy $E_F + eV_0$ (see Fig. 3), can be written as

$$\frac{1}{e}\frac{dn(V_0)}{dV_0} \approx \mathrm{DOS}(E_F + eV_0). \tag{10}$$

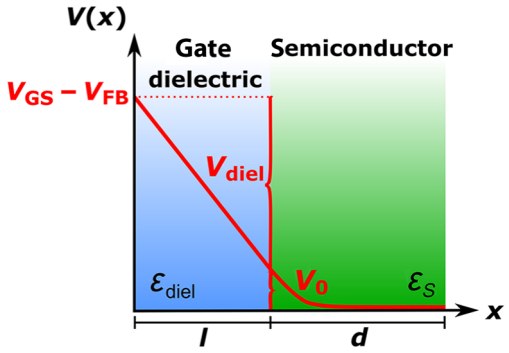

FIG. 4. Sketch of the potential drop across the gate dielectric and the semiconductor layer of the transistor. In the original Grünewald method, it is assumed that $|V_0| \ll |V_{\rm GS}|$ and, hence, V_0 is ignored. In the extended Grünewald method proposed here, this simplification is removed, and the contribution of V_0 is correctly taken into account.

B. Extension of the original Grünewald method

As mentioned in the Introduction, the original Grünewald method makes a critical simplification in the choice of the first boundary condition for the Poisson equation: The contribution of the interface potential V_0 to the total potential drop across the semiconductor and the gate dielectric is neglected (this is assumption 5 in the list above). A schematic of the potential across the semiconductor-gate dielectric stack is shown in Fig. 4. As will be shown, this simplification holds only for transistors with a high operating voltage (i.e., a thick gate dielectric), but not for transistors with a low operating voltage (i.e., with a gate dielectric that is either very thin, as shown here, or has a large permittivity [43]). For low-voltage transistors, the final result of the density-of-states function is greatly affected by the simplification regarding V_0.

For the purpose of this analysis, the gate dielectric can be considered as "thin" if its thickness is no greater than a few times the Debye length in the semiconductor, since in this case the capacitance of the gate dielectric will be similar to the capacitance of the charge-accumulation layer at the flat-band voltage and, thus, the potential drop across the gate dielectric $V_{\rm diel}$ will be similar to the potential drop across the thickness of the semiconductor layer V_0, which implies that the contribution of V_0 to the total voltage drop cannot be neglected [44]. As will be shown later, the average Debye length in the semiconductor is 2 nm, which implies that the gate dielectric with a thickness of 5.3 nm can be considered indeed as thin.

In order to extend the original Grünewald method and make it applicable to any gate-dielectric thickness and operating voltage, we repeated the mathematical derivation of the original Grünewald method, but instead of using Eq. (5), which reflects the simplification

$$V_{\rm GS} = V_{\rm FB} + V_{\rm diel}, \tag{11}$$

we included the term V_0 in this equation in order to properly take into account the contribution of V_0 to the total potential drop:

$$V_{GS} = V_{FB} + V_{diel} + V_0. \tag{12}$$

As a consequence, Eq. (5) transforms into

$$\varepsilon_0 \varepsilon_{diel} \frac{V_{GS} - V_{FB} - V_0}{l} = -\varepsilon_0 \varepsilon_S \frac{\partial V(x)}{\partial x}\bigg|_{x=0}. \tag{13}$$

This adjustment has profound implications on the subsequent equations. Following the original derivation, the differential equation (7) translates to

$$\frac{dV_0}{d(V_{GS} - V_{FB})} = \frac{\varepsilon_{diel} d}{\varepsilon_S l} \frac{1}{I_0} \frac{dI}{d(V_{GS} - V_{FB})} \times \frac{V_{GS} - V_{FB} - V_0}{\exp\left(\frac{eV_0}{k_B T}\right) - 1}. \tag{14}$$

This differential equation cannot be simplified analytically. However, it is possible to determine the relation $V_0(V_{GS} - V_{FB})$ using numerical methods (e.g., using the ordinary differential equation solver `scipy.integrate.odeint` included in the open-source PYTHON library SciPy [45]). Because the extended boundary condition (13) now includes the term V_0, the equation for the total carrier density must be adjusted as well:

$$n(V_0) = \frac{\varepsilon_{diel}^2 \varepsilon_0}{\varepsilon_S l^2 e}(V_{GS} - V_{FB} - V_0) \times \left[\left(\frac{\partial V_0}{\partial (V_{GS} - V_{FB})}\right)^{-1} - 1\right]. \tag{15}$$

All subsequent steps in the analysis are identical to the original Grünewald method.

A general issue of the Grünewald method is that the DOS is calculated as a function of $E_F + eV_0$, i.e., that the energy is referenced to the initial Fermi energy E_F. This may make it difficult to compare the DOS functions of transistors in which the difference between the energy of the transport level and the initial Fermi energy is not the same, e.g., because the transistors are fabricated using different materials. For this reason, it may be more convenient to reference the DOS to the transport level [30,46–48], i.e., to the lowest unoccupied molecular orbital (LUMO) or conduction band edge (E_C) in the case of *n*-channel transistors, and the highest occupied molecular orbital (HOMO) or valence-band edge (E_V) in the case of *p*-channel transistors. One way to accomplish this was recently suggested by Za'aba *et al.* [35]. In their approach, the gate-source voltage at which the measured effective charge-carrier mobility saturates (i.e., no longer increases with increasing gate-source voltage) is translated to the corresponding value for the interface potential V_0 using Eq. (14) and this value is then taken as the energetic position at which the Fermi level crosses the transport level. This approach is adopted here, as illustrated in Fig. 2. We note, however, that this approach produces a reliable result only if the gate-source voltage at which the effective carrier mobility saturates is unambiguously identified, which will usually require that the measurement of the transistors' transfer curve is conducted over a wide range of gate-source voltages.

C. Experimental comparison of the original and extended Grünewald method

In the previous section, we showed how the Grünewald method is extended by eliminating the simplification regarding V_0, which leads to extended forms of two of the three key equations of the Grünewald method, namely, Eqs. (14) and (15). In order to test how this extension affects the result of the Grünewald method depending on the gate-dielectric thickness, we fabricate two types of transistors: one with a thick gate dielectric (110 nm thick) and one with a thin gate dielectric (5.3 nm thick). After device fabrication, the transfer curves (drain current as a function of applied gate-source voltage) of both TFTs are measured in the linear regime of operation, i.e., with a drain-source voltage that is negligible compared to the difference between the gate-source voltage and the threshold voltage (see Fig. 2).

From each of these transfer curves, the DOS of the semiconductor is calculated once using the original Grünewald method [Eqs. (7), (9), and (10)] and once using the extended Grünewald method [Eqs. (14), (15), and (10)]. Consequently, any deviations between the DOS calculated using the original Grünewald method (i.e., with the simplification regarding V_0) and the DOS calculated with the extended Grünewald method (i.e., without this simplification) can be ascribed to the simplification regarding V_0.

In the first step, the relation between the interface potential and the gate-source voltage [$V_0 = f(V_{GS} - V_{FB})$] is calculated numerically using PYTHON, once from Eq. (7) and once from Eq. (14). In the case of the TFT with the thick gate dielectric, the results are essentially identical, as shown in Fig. 5(a). In contrast, for the TFT with the thin gate dielectric, the original differential equation (7) and the extended differential equation (14) produce notably different results [see Fig. 5(b)], because the magnitude of the gate-source voltage is, in this case, comparable to the magnitude of the interface potential V_0 (a few hundred millivolts), so that the latter can no longer be ignored without introducing a significant error.

In the second step, the relation between the total carrier density and the interface potential [$n = f(V_0)$] is calculated, once from Eq. (9) and once from Eq. (15), and

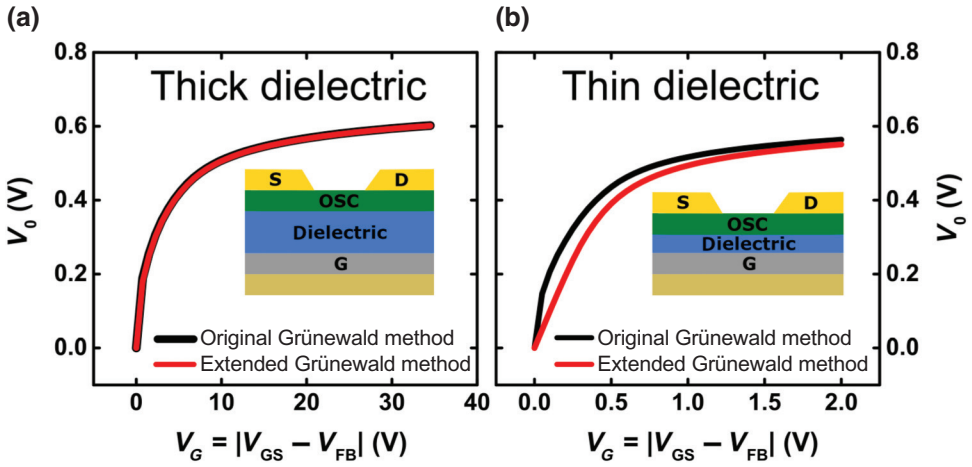

FIG. 5. Results of the first step of the Grünewald method in which the relation between the interface potential and the gate-source voltage is calculated from the measured transfer curves. This calculation is performed once using Eq. (7) (original method, shown with black lines) and once using Eq. (14) (extended method, shown with red lines). (a) For the TFT with the thick gate dielectric, the results show that the simplification in the original Grünewald method is indeed justified. (b) For the TFT with the thin gate dielectric, the original differential equation (7) and the extended differential equation (14) produce notably different results, because the magnitude of the gate-source voltage is, in this case, comparable to the magnitude of the interface potential V_0 (a few hundred millivolts), so that the latter can no longer be ignored without introducing a significant error.

the results are shown in Fig. 6. From the total carrier density, the Debye length in the semiconductor is calculated according to

$$\lambda_D = \sqrt{\frac{\varepsilon_S \varepsilon_0 k_B T}{e^2 n(V_{GS})}}. \tag{16}$$

The average value of the Debye length in the semiconductor over the range of gate-source voltages considered here is 2 nm; only for a narrow range of gate-source voltages just above the flat-band voltage, the Debye length exceeds the thickness of the semiconductor layer (20 nm). This range of gate-source voltages is excluded for the following analysis in order not to violate assumption 4 from the list above and to keep the analysis self-consistent.

In the third step, the trap DOS is calculated using Eq. (10), yielding the DOS as a function of $E_F + eV_0$. In the final step, the DOS is obtained as a function of $E - E_V$ by determining the gate-source voltage at which the carrier mobility saturates and translating it to the corresponding value for the interface potential V_0. This value of V_0 is taken as the energetic position at which the Fermi level crosses the transport level (see Fig. 2).

The results are shown in Fig. 7. As can be seen, in the case of the TFT with the thick gate dielectric, the deviation between the DOS functions obtained using the original and the extended Grünewald method is extremely small, which confirms that, for transistors with high operating voltages, the commonly employed simplification regarding the contribution of the interface potential V_0 to the total potential drop is indeed justified [30–37]. In contrast, the choice of the method has a profound effect on the DOS extracted from transistors with low operating voltages, as the simplification regarding V_0 that is made

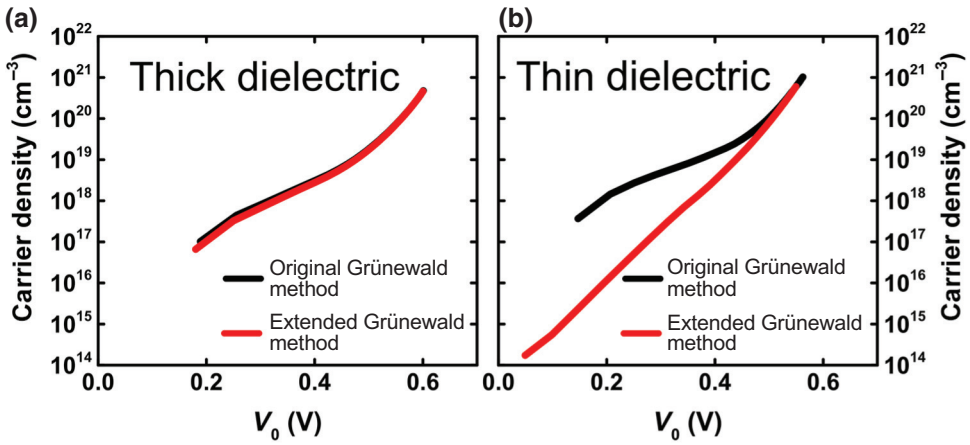

FIG. 6. Results of the second step of the Grünewald method in which the relation between the carrier density and the interface potential is calculated. This calculation is performed once using Eq. (9) (original method, shown with black lines) and once using Eq. (15) (extended method, shown with red lines).

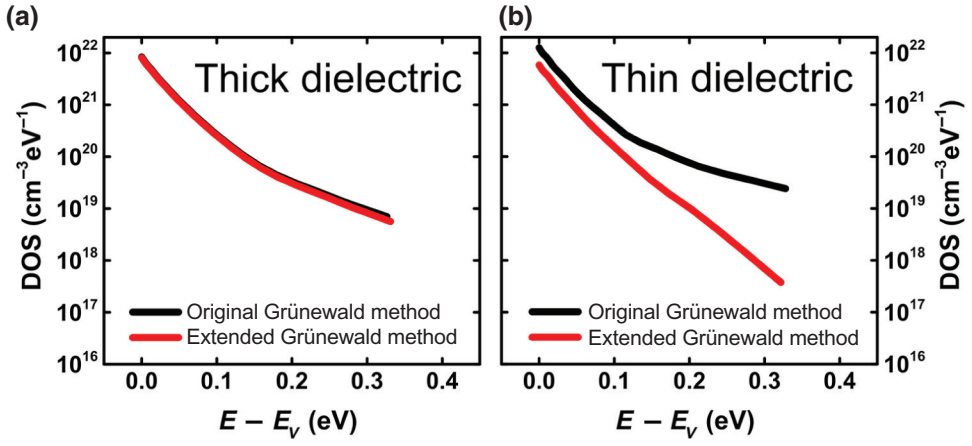

FIG. 7. Results of the final steps of the Grünewald method. Using Eq. (10), the trap DOS is calculated, yielding the DOS as a function of $E_F + eV_0$, which is then converted into the DOS as a function of $E - E_V$ by taking the gate-source voltage at which the carrier mobility saturates (see Fig. 2) as the gate-source voltage at which the Fermi level crosses the transport level E_V. The DOS is calculated once using the results from Eq. (9) (original method, shown with black lines) and once using the results from Eq. (15) (extended method, shown with red lines). (a) For the TFT with the thick gate dielectric, the results show that the simplification in the original Grünewald method does not affect the calculated trap DOS and is thus justified. (b) For the TFT with the thin gate dielectric, the trap DOS functions obtained with and without the simplification deviate substantially, as the original Grünewald method significantly overestimates the trap DOS in this case.

in the original Grünewald method leads to an overestimation of the DOS compared to the result from the extended Grünewald method.

It is important to note that both the original and the extended Grünewald method yield reliable results only if the transfer curve of the transistor is not dominated by the contact resistance, i.e., if the potential drops across the contact resistances are small. To evaluate whether this requirement is fulfilled in the TFTs examined here, we measure the width-normalized contact resistance of both TFTs using the transmission-line method (TLM) [49,50] (for details, see Fig. S3 of the Supplemental Material [51]) and calculated its contribution to the width-normalized total resistance. The results are shown in Fig. 8. As can be seen, in the TFT with the thin gate dielectric, the contribution of the contact resistance to the total TFT resistance is indeed no greater than 10%, which means that the error in the calculation of the DOS in the TFT with the thin gate dielectric is relatively small. In the TFT with the thick gate dielectric, the contribution of the contact resistance to the total TFT resistance is about 20% and will thus introduce a somewhat larger error. On the other hand, Fig. 8 also indicates that the ratio between the contact resistance and the total TFT resistance is essentially independent of the gate-source voltage, which means that the overall shape of the density-of-states function is not significantly affected. One possibility to further reduce the influence of the contact resistance on the extraction of the DOS would be to perform the measurements on TFTs with an even greater channel length [31].

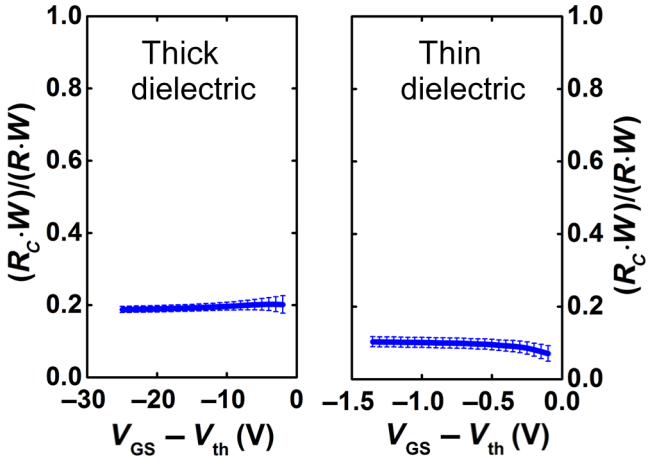

FIG. 8. Ratio between the channel-width-normalized contact resistance ($R_C \cdot W$) and the channel-width-normalized total device resistance ($R \cdot W$) for TFTs with a channel length of 100 μm, measured using the transmission line method (TLM) and plotted as a function of the difference between the gate-source voltage and the threshold voltage. For both types of TFT (thick and thin gate dielectrics), the contact resistance is small compared to the total resistance.

IV. CONCLUSION

We explore an extension of the Grünewald method for the extraction of the density and energetic distribution of the trap states in the semiconductor of a transistor from its measured transfer characteristics to transistors with low operating voltage. The contribution of the interface potential V_0 to the total potential drop of the applied gate-source

voltage is incorporated correctly into the formalism, leading to the extension of two of the three key equations for the Grünewald method. To demonstrate the significance of this extension, we perform the calculation of the trap DOS on TFTs with a thick and with a thin gate dielectric, once using the original Grünewald method and once using the extended Grünewald method. For the TFT with the thick gate dielectric, the original and the extended method yield essentially the same result, which confirms the validity of the original Grünewald method for such transistors. In contrast, for the TFT with the thin gate dielectric, the need for the extended Grünewald method is verified, as in such transistors, the contribution of the interface potential cannot be ignored without introducing a significant error in the calculated trap DOS.

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