Editors' Suggestion

Balance of Horizontal and Vertical Charge Transport in Organic Field-Effect Transistors

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High-performance organic field-effect transistors (OFETs) are an essential building block for future flexible electronics. Although there has been steady progress in the development of high-mobility organic semiconductors, the performance of lateral state-of-the-art OFETs still falls short, especially with regard to the transition frequency. One candidate to overcome the shortcomings of the lateral OFET is its vertical embodiment, the vertical organic field-effect transistor (VOFET). However, the detailed mechanism of VOFET operation is poorly understood and a matter of discussion. Proposed descriptions of the formation and geometry of the vertical channel vary significantly. In particular, values for lateral depth of the vertical channel reported so far show a large variation. This is an important question for the transistor integration, though, since a channel depth in the micrometer range would severely limit the possible integration density. Here, we investigate charge transport in such VOFETs via drift-diffusion simulations and experimental measurements. We use a (vertical) organic light-emitting transistor [(V)OLET] as a means to map the spatial distribution of charge transport within the vertical channel. Comparing simulation and experiment, we can conclusively describe the operation mechanism which is mainly governed by an accumulation of charges at the dielectric interface and the channel formation directly at the edge of the source electrode. In particular, we quantitatively describe how the channel depth depends on parameters such as gate-source voltage, drain-source voltage, and lateral and vertical mobility. Based on the proposed operation mechanism, we derive an analytical estimation for the lateral dimensions of the channel, helping to predict an upper limit for the integration density of VOFETs.

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I. INTRODUCTION

The concept of the vertical organic field-effect transistor (VOFET), as introduced by Stutzmann *et al.* [1], offers the possibility to reduce the geometric channel length of the transistor to a few tens of nanometers with a comparably low structuring effort. In these vertical transistors, the charge transport is redirected from the lateral—like in classical thin-film transistors—to the vertical direction. In this way, high current densities can be reached, which ultimately enables high switching frequencies as required for future flexible electronic applications, such as flexible radio-frequency identification tags (RFID) or active-matrix displays. A large diversity of different vertical transistor architectures has been proposed and a steady progress concerning the device performance and reliability is observed [2]. The working principle of lateral organic field-effect transistors (OFETs) has already been broadly investigated [3–5], while the interest in the device physics of the VOFET has just recently increased [6,7]. In particular, the vertical arrangement of source, drain, and gate electrode and the comparable strength of the gate and drain field lead to complex field- and charge-carrier distributions in the device [cf. Fig. 1(a)]. In particular, the lateral extension of the channel is controversially discussed in the literature. This question is of significant technological relevance, though, because an extension in the micrometer range would severely limit the possible integration density of the devices. For very similar devices, Ben-Sasson *et al.* propose that the formation of the vertical channel starts far away from the edge of the source electrode [8–10]. In their particular case, they argue that this lateral extension of the channel provides a limit for the current density because the extension of the channel is comparable to the distances between adjacent source electrodes (with a spacing of 100 nm). A different approach by Sheleg *et al.* [11], based

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on simulations, shows a formation of the vertical channel far away from the source insulator as well. Their explanation is based on an electrostatic repulsion of charge carriers from the source insulator. In both descriptions, the channel requires a significant space next to the source, which would result in channels of adjacent transistors influencing and limiting each other. However, studying the formation of the channel in order to provide an improved understanding of the device physics is rather difficult since methods to distinguish between contact and channel resistance such as four-probe measurements or transmission-line characterization cannot be used for VOFET devices, because the channel length is not well defined.

Here, we study the charge transport in VOFETs using drift-diffusion simulations and experiments on (vertical) organic light-emitting transistors [(V)OLETs]. These devices are based on the design of Nakamura *et al.* [12,13] and are a combination of a VOFET and an organic light-emitting diode (OLED) near the top drain electrode [cf. Fig. 1(a)]. Since the charge-carrier transport is partly in the vertical direction, the spatial distribution of light emission from the OLED can reveal the size, geometry, and current distribution of the vertical channel. Moreover, since a top-emission OLED is employed, we can use the high spatial resolution of light emission to map the local vertical current density. Our approach of combining experiments with numerical simulations provides results that are in contradiction to previous findings and therefore allows for new insights into the device-operation mechanism, in particular, the channel formation directly at the edge of the source insulator and the formation mechanism very similar to the planar OFET.

II. INVESTIGATION METHODS

A. Sample preparation

The (V)OLET structure is shown in Fig. 1(a). It is the VOFET configuration that we described in an earlier publication [14], where the upper pentacene layer is exchanged by an OLED stack [emission material: Alq_3 [aluminum-tris(8-hydroxychinolin)]+DCM [4-(dicyanomethylene)-2-methyl-6-(p-dimethylaminostyryl)-4H-pyran]] [15]. In contrast to similar devices from Nakamura *et al.* [12,13], these devices are top emitting. Thus, the light has a much shorter path through dispersive matter, which should result in a higher lateral resolution. Samples are built on p-doped Si substrates, serving as a gate electrode. The wafers are covered with either 300 nm of wet-oxidized SiO_2 or 35 nm Al_2O_3 as a gate dielectric. The Al_2O_3 is deposited with an Atomic Layer Deposition System SI ALD LL by Sentech in a plasma-assisted process at 250°C. The thus-prepared wafers are cleaned in acetone, ethanol, and isopropanol in an ultrasonic bath for 5 min each. Afterward, they are treated in oxygen plasma for 10 min. As a last step, they are dipped into hexamethyldisilazane (HMDS) for 30 min for surface passivation and cleaned with isopropanol again.

The following layer of pentacene (25 nm) is evaporated under a base pressure of 10^{-7} mbar at a rate of 0.5 Å s^{-1}. The gold electrodes of 30 nm (1 Å s^{-1}) for the source electrode are structured using orthogonal double-resist lithography employing the procedure explained in [16]. The lithographic exposure tool is a SUESS MJB4 mechanical mask aligner in a nitrogen atmosphere. The source insulator used is a photoactive negative resist called OSCOR4000 by Orthogonal Inc. It is structured with a mask aligner after the gold lift-off to exactly match the shape and position of the source electrode pads. In contrast to the SiO_2 used in Ref. [14], the area of the insulator, and therefore the overlap of the insulator with respect to the source electrode itself, can be influenced during the photolithography via controlled overexposure. The feature size of a negative resist only increases with increased exposure, which allows for higher control over the device geometry.

The OLED stack and the drain electrode are evaporated through a shadow mask, while the layer thicknesses and the doping of the individual layers are varied to investigate the channel formation behavior in dependence of the conductivity of the OLED stack. The detailed layer sequence of the OLED is as follows: Spiro-TTB [$2,2',7,7'$-tetrakis-(N,N-dimethylphenylamino)-9,9′-spirobifluoren]: 50 to 150 nm at 1 Å s^{-1}, Alq_3+DCM (1 wt %): 15 nm at 0.3 Å s^{-1}, Alq_3: 0 to 50 nm at 0.5 Å s^{-1}. Some samples have a Spiro-TTB layer doped with F_6-TCNNQ [2,2′-(perfluoronaphthalene-2,6-diylidene)dimalononitrile] (4 wt %). At last, 5 nm Al

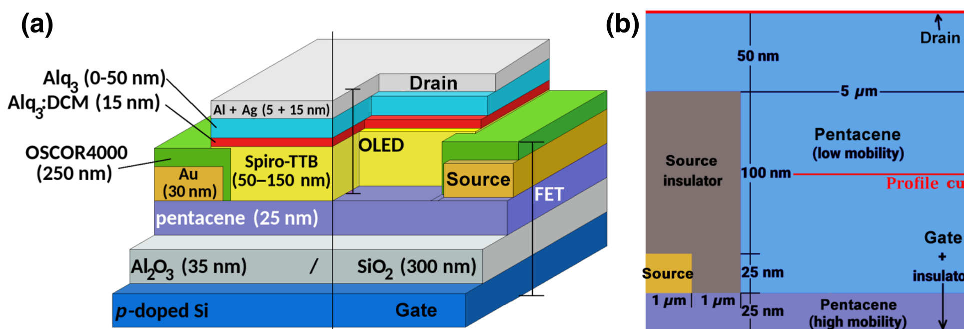

FIG. 1. (a) Sample structure and stack of experimental (V)OLET devices. (Some of the samples are made with doped Spiro-TTB, and some are undoped.) (b) Device geometry used for drift-diffusion simulations.

at 0.3 Å s^{-1} and 15 nm Ag at 1 Å s^{-1} is added as a semitransparent top electrode.

A Hewlett Packard HP4145B parameter analyzer is used for electrical characterization and driving of the transistor. The light-emission distribution is measured in a vibration-damped setup with micropositioners for electrode contacting. The images are recorded with a Basler Ace ac1300-30uc connected to an infinity-corrected ten-times magnifying, long-working-distance lens by Mitutoyo. The setup provides a resolution of around $(0.3 \times 0.3)\ \mu m^2\ px^{-2}$ and a total image size of $430 \times 320\ \mu m$. Light intensity is taken with an 8-bit resolution; thus, low-intensity values are folded with a linear dependency. After image acquisition, the pictures are rotated, transferred into gray scale, and corrected by a dark picture. The final data output is an average along the channel width of the dark-corrected light output. All images are acquired with an exposure time of 2 s.

B. Carrier transport model and simulation platform

The operation principle of the VOFET is studied by two-dimensional simulations of the carrier flow based on drift-diffusion models. In relation to the simulations, the emission layer of the (V)OLET can be seen as a virtual drain electrode of a p-type VOFET where all holes recombine. Considering p-type devices based on pentacene, we neglect electrons and thus all recombination processes and reduce the system to a unipolar version of the van Roosbroeck system [17], consisting of a drift-diffusion equation for the hole density p coupled to the Poisson equation for the electrostatic potential φ,

$$-\nabla \cdot (\varepsilon_0 \varepsilon_r \nabla \varphi) = q(C + p), \tag{1}$$

$$\frac{\partial p}{\partial t} + \frac{1}{q} \nabla \cdot j_p = 0. \tag{2}$$

Here, ε_r, ε_0, and q are the relative dielectric constant, vacuum permittivity, and the elementary charge, respectively, and C denotes the doping profile. The current density j_p is assumed to be in drift-diffusion form

$$j_p = -q\mu_p p \nabla \varphi - q D_p \nabla p, \tag{3}$$

where the hole mobility μ_p and the diffusion coefficient D_p are related via the Einstein relation, $D_p = \mu_p k_B T/q$, with Boltzmann's constant k_B and temperature T.

The simulations are carried out on one half of a vertical (mirror symmetric) cross section of the device; compare Fig. 1(b). To take the anisotropy in mobility of pentacene into account, the organic areas are split into two subregions of different mobilities: a low mobility for vertical transport and a high mobility for lateral transport. A constant mobility is assumed for the simulation and the experimental evaluation. This assumption is justified, because the mobility is almost constant in the areas of high charge-carrier density that contribute predominantly to the charge transport [18]. The vertical layer structure of the VOFET between the gate and drain contact contains a gate electrode of unspecified thickness and a gate oxide of 35 nm, followed by a 25-nm-thick pentacene layer. This bottom pentacene layer is set to have the higher mobility. On the top of the left-hand side is a 25-nm-thick and 1-μm-wide source electrode that is covered by an insulator (from above 100 nm thick and from the right-hand side 1 μm wide). The region to the right of the source and oxide, as well as a covering layer on top, (50 nm) consist of pentacene. These areas of organic semiconductor are set to the lower mobility. The drain electrode is the topmost layer, covering the full width of the device.

The simulation domain consists of the regions filled with the organic semiconductor and the insulator above and beside the source, while the metal contacts and the gate oxide are completely excluded and are realized by boundary conditions. The Poisson equation is solved on the whole simulation domain, whereas the drift-diffusion equation is considered in pentacene only. The boundary conditions at the source and drain contacts are treated as Ohmic contacts defined by the applied voltages and local charge neutrality. Outside the source and drain contact regions, we assume no flux boundary conditions for the drift-diffusion equation.

The stationary van Roosbroeck system is solved on the simulation domain [Eqs. (1) and (2)] using the WIAS software DDFERMI [19], which is based on a finite-volume approach in combination with the Scharfetter-Gummel scheme [20]. The hole densities are modeled via a Boltzmann distribution. The spatial discretization of the simulation domain achieved via tensor product meshes involves approximately 28 000 nodes, while the resolution of the mesh is higher at the source.

All physical parameters used in the simulations are collected in Table I. Moreover, the dielectric constant of pentacene is assumed to be equal in the lateral and vertical direction. Values for lateral and vertical charge-carrier mobility are taken from our previously published set of data [18], where we have determined the mobility at a

TABLE I. Physical parameters of the simulations.

Physical parameter	Value
ε_r (source oxide)	3.8
ε_r (gate oxide)	7.5
ε_r (pentacene)	3.3
μ_{lat} (pentacene)	$0.45\ cm^2\ V^{-1}\ s^{-1}$ [18]
μ_{vert} (pentacene)	$4 \times 10^{-3}\ cm^2\ V^{-1}\ s^{-1}$ [18,21]
E_g (pentacene)	2.0 eV
T	300 K
C (pentacene)	$1 \times 10^{13}\ cm^{-3}$ [22]

hole density of about 1×10^{16} cm^{-3}. However, higher values for the vertical charge-carrier mobility in pentacene (up to 0.1 cm^2 V^{-1} s) are reported for higher electric fields in high-frequency diodes [21]. We assume no oxygen background doping for the semiconductor.

III. RESULTS

A. Simulation results

We simulated the charge-carrier density in the given geometry in dependence on different external bias conditions and deduced the resulting lateral and vertical current flow. This analysis allows for a detailed understanding of the channel formation and estimation of maximum channel size.

Figures 2(a)–2(c) shows the charge-carrier density as obtained from the simulation at different gate-source voltages and constant drain-source voltage of −0.5 V. The transistor is switched off for a positive gate bias and the charge-carrier density is generally low (limited by the background doping concentration). It is elevated directly underneath the source insulator due to the accumulation caused by the high drain-source field, forming a region of high conductivity. Additionally, a thin area of slightly higher charge density is forming along the insulator edge to the drain electrode. This effect can be attributed to the diffusion-assisted transport of the charge carriers accumulated underneath the insulator. Comparison between simulations with different geometries shows a change in the shape of this stripe. Increasing the length of the source insulator overlap decreases the off-current, since a longer path has to be overcome via diffusion. This dependence of the off current on the insulator size can also be seen in real devices [23], but this topic is not in the scope of this paper.

The turn on of the transistor [Fig. 2(b)]—at negative gate bias—is accompanied by an increase in charge-carrier density underneath the source, similarly to a lateral OFET. A thin area with the same high charge-carrier density arises underneath and along the insulator edge, which allows charge transport to the drain. For even higher gate-source voltages [Fig. 2(c)], only the width of the area that contributes to the charge transport increases. However, the absolute charge-carrier density in the already conducting area only grows slightly, due to the field distribution.

The resulting current density acts accordingly. The vertical current [Fig. 2(g)] is almost nonexistent for the device switched off, while the lateral current [Fig. 2(d)] feeds the accumulation underneath the source insulator, caused by the drain-source field. For negative gate bias, the lateral current is conducted via a channel at the gate insulator created by the accumulation of the gate field. The lateral current is spread out underneath the source insulator. In contrast to the lateral OFET, where accumulation occurs

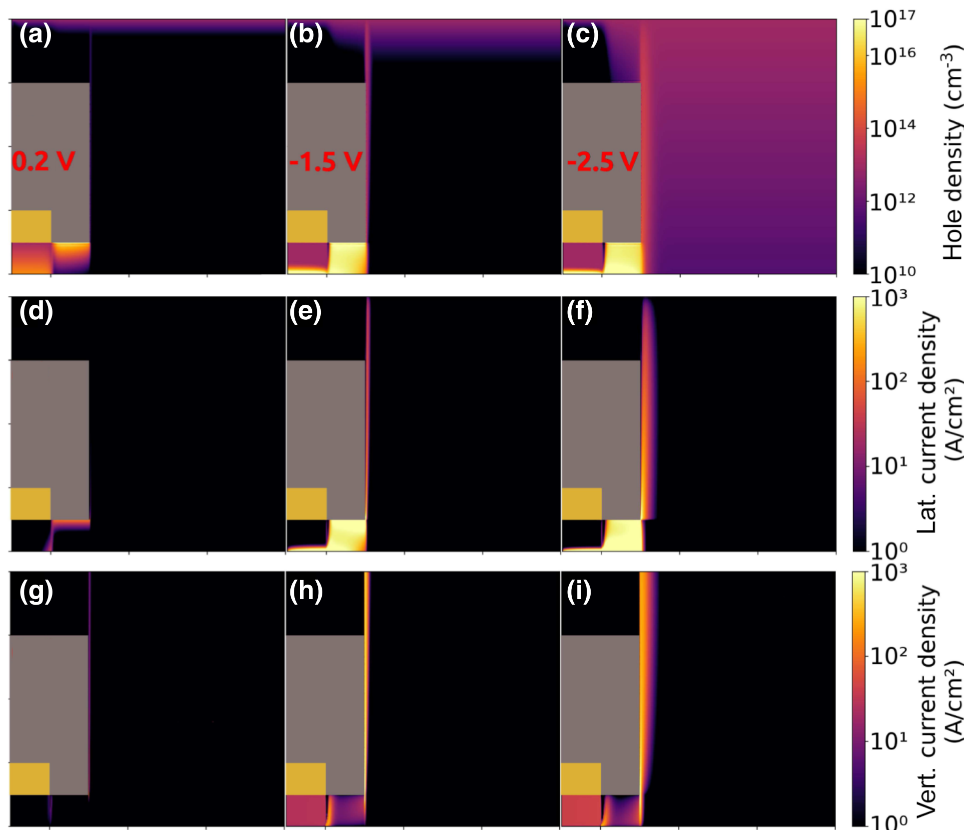

FIG. 2. Drift-diffusion simulations of pentacene-based VOFET at different gate-source voltages: (a,d,g) switched off ($V_{GS} = 0.2$ V), (b,e,h) switched on ($V_{GS} = -1.5$ V), (c,f,i) switched on ($V_{GS} = -2.5$ V) $V_{DS} = -3$ V for all three cases. (a,b,c): Hole density distribution. (d,e,f): Lateral component of local current density. (g,h,i): Vertical component of local current density.

only at the gate interface, the gate and the drain field cause accumulation at the individual interfaces. The vertical current does not play a major role underneath the source and source insulator.

Entering the area next to the source insulator, the vertical current is increasing significantly. The stripe of high current density—which is governing the output current of the overall device—has a distinct distribution. At the edge of the insulator, the density is high and decreases with distance. The overall width of this distribution is increasing the closer it is to the drain [visible in Fig. 2(i)]. The extent of the resulting vertical channel is also increasing with higher gate-source voltages, while the absolute density at the edge is growing only slightly. The lateral current has a similar distribution. Here, the lateral transport gets weaker the closer it gets to the drain electrode.

Based on these simulations, several deductions for the working principle of the VOFET can be made: similar to the lateral OFET, charge carriers are accumulated at the semiconductor-dielectric interfaces (gate and source). These accumulated charge carriers are extracted by the drain field in the areas where they are not shielded by the source and source insulator. The source provides a steady supply of new charge carriers and, thus, the carrier density is high next to it. Far away from the source, the density is low, because all charge carriers are already extracted by the drain field. The width of the vertical channel—called channel depth—is, therefore, defined by the diffusion of charge carriers due to this density gradient. It is a consequence of the balance between the charge-carrier accumulation via the gate field and the extraction via the drain field. The width of the channel is defined by the width of the source and drain electrodes, while the length of the channel consists of the full charge-carrier path from source to drain. It is not well defined and can only be estimated as an effective value.

A higher drain-source field in the vertical direction pulls the charge carriers more strongly toward the drain, resulting in a narrower vertical channel with higher density. The output current increases due to more current passing through the same volume. On the other hand, a higher gate bias increases the accumulation at the interface and, thus, the diffusion in the lateral direction. This diffusion increases the overall depth of the vertical channel. The current increase is here driven by an increase in the size of the channel. The lateral and vertical mobilities of the individual layers define parameters for this balance.

Since the channel requires a certain space next to the source-insulator edge, two adjacent channels could theoretically overlap and limit each other. However, in the simulation, the channel depth for the fully switched-on state is below 1 μm. Since this channel depth is a consequence of the balance between the lateral and vertical transport, choosing materials with sufficiently high vertical mobilities could reduce this figure substantially.

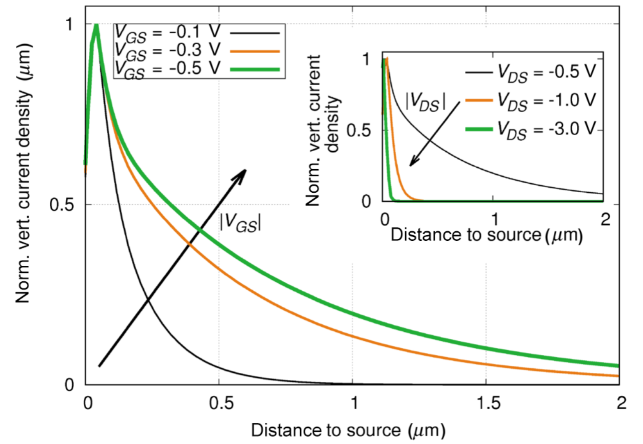

FIG. 3. Profile cuts of the vertical component of local current density. [The cutting line is indicated in Fig. 1(b)] at different gate-source voltages ($V_{DS} = -0.5$ V for all.) The data are normalized to the maximum value. Inset: Variation of drain-source voltage at constant $V_{GS} = -0.5$ V.

How a change in voltage effects the extent of the channel can be seen in the profile cuts shown in Fig. 3. To quantitatively analyze the dependencies of the channel geometry, we fit these current density distributions to an exponential drop ($j_0 e^{-x/d_{\mathrm{eff}}}$)—defining d_{eff} as the effective channel depth and j_0 as the maximum current density at the edge of the source insulator. The effective channel depth can be linked to the applied bias voltages utilizing the field-effect transistor current equations. Integrating the current density over the depth of the channel gives the total current:

$$I \propto \int_0^{x_{\mathrm{end}}} j_0 e^{-x/d_{\mathrm{eff}}} dx \propto -d_{\mathrm{eff}} j_0 \left(e^{-x_{\mathrm{end}}/d_{\mathrm{eff}}} - 1\right). \quad (4)$$

The current density is negligible at the end of the channel; thus,

$$I \propto j_0 d_{\mathrm{eff}}. \quad (5)$$

Since we only aim to investigate the formation of the channel to find an estimate for its maximal extent, we will limit further analysis to the linear regime. Applying a higher V_{DS} will only decrease the channel depth (cf., e.g., Fig. 2). Thus, for a field effect transistor, the current can be calculated within the gradual channel approximation [24]:

$$I_D(V_{GS}, V_{DS}) \propto (V_{GS} - V_{\mathrm{Th}})V_{DS} - \frac{V_{DS}^2}{2} \quad (6)$$

in the linear regime, where V_{Th} is the threshold voltage of the transistor. This equation is very broad and only assumes the validity of Ohm's law and describes the transistor by a plate capacitor. As a first approximation, this simple model should also hold true for the vertical transistor. That the current is controlled via charge-carrier

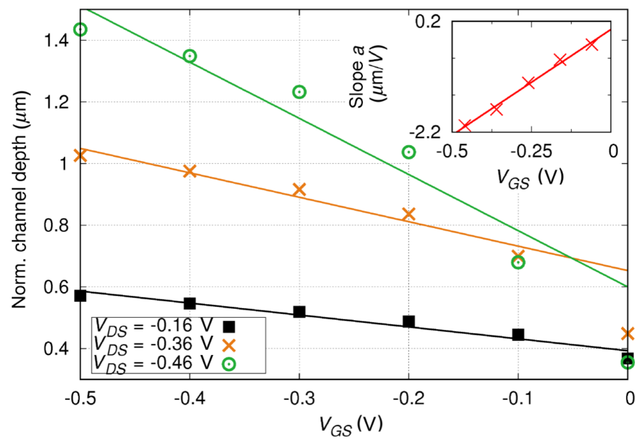

FIG. 4. Effective channel depth gained from exponential fits of the vertical current density distribution at different drain-source voltages in dependence of the gate-source voltage. To compare different V_{GS}, the channel depth is normalized to account for changing j_0. Inset: Slope "a" of the linear fit of the effective channel depth in dependence (normalized by j_0) of the gate-source voltage: $d_{\text{eff}} = aV_{GS} + b$. Added is a linear fit of the slope in dependence of the drain-source voltage.

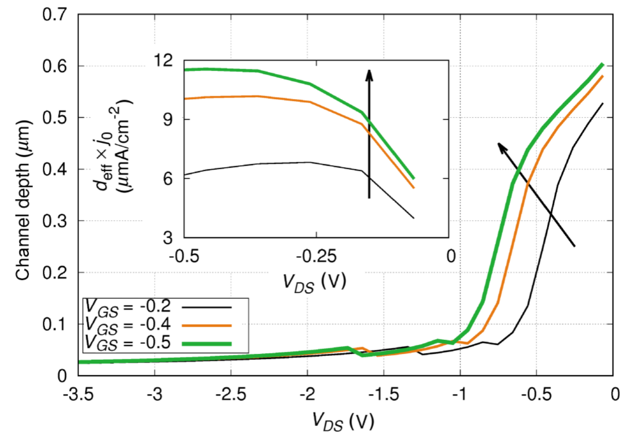

FIG. 5. Effective channel depth gained from exponential fits of the vertical current density distribution at different gate-source voltages in dependence of the drain-source voltage. Inset: $d_{\text{eff}}j_0$ in dependence on drain-source voltage, in the linear regime.

accumulation at the gate can be seen in the simulations. For the linear regime, we conclude

$$j_0 d_{\text{eff}}^{\text{lin}} \propto (V_{GS} - V_{\text{Th}})V_{DS} - \frac{V_{DS}^2}{2}. \tag{7}$$

When the maximum current density at the beginning of the channel is not significantly changing—especially if only the gate-bias is changed—this relation can be further specified to

$$d_{\text{eff}}^{\text{lin}} \propto (V_{GS} - V_{\text{Th}})V_{DS} - \frac{V_{DS}^2}{2}. \tag{8}$$

Figures 4 and 5 show the very good agreement of the simulation results to the model predictions. In the investigated voltage range, the channel depth depends linearly on the applied gate-source voltage. To compare this dependency at different drain-source voltages, we normalized the channel depth so that all distributions would have the same j_0. The effect of a different drain-source voltage is a change in the slope and absolute position of these lines. In agreement with the model, the change in slope should depend linearly on the drain-source voltage, which can be seen in the inset of Fig. 4.

Figure 5 shows that increasing the drain-source voltage decreases the channel depth steadily in the linear regime. When reaching the saturation point, the channel is strongly confined to a narrow stripe. The validity of the model can be seen in the inset. The product of $j_0 d_{\text{eff}}^{\text{lin}}$ is increasing linearly and saturating quadratically when reaching V_{GS}, as predicted by the model using the full relation (7).

B. Experimental results

We test how the findings from the simulations translate into actual device behavior by studying the channel formation with the previously mentioned (V)OLETs. We employ the light emission to visualize the vertical current-density distribution in the channel. Although the (V)OLET stack is a more complex organic heterostructure than the stack chosen for the drift-diffusion simulations, conceptually, the mechanism of channel creation is expected to be similar. In particular, the large contrast in lateral and vertical mobility applied in the simulations is realized in the (V)OLET devices by using the high-mobility pentacene layers and low-mobility Spiro-TTB and Alq_3 layers for lateral and vertical transport, respectively. Thus, the (V)OLET can be used to investigate the scaling behavior of the channel depth. However, the absolute values obtained from the devices cannot be compared to the simulations, primarily because of the neglect of contact resistance in the simulations and since the ratio between the vertical and lateral mobilities is not exactly known in the actual (V)OLET devices. Additionally, the emission interface layer introduces a further charge-carrier barrier.

The results of a measurement set can be seen in Fig. 6. The drain-source voltage is the same ($V_{DS} = -10$ V) for all three different gate-source voltages. No light is emitted by the device when the gate is at zero bias. For devices with none or just a very small insulator overlap, the devices show a small and weak light emission even at zero gate bias, indicating the influence of the source-insulator geometry on the turn-off behavior of this transistor design.

At the threshold-voltage, the device starts to emit light directly at the source insulator edge. The size of the emission zone grows further with higher gate-source voltage. Thus, it is evident that the light emission is controlled by the gate bias.

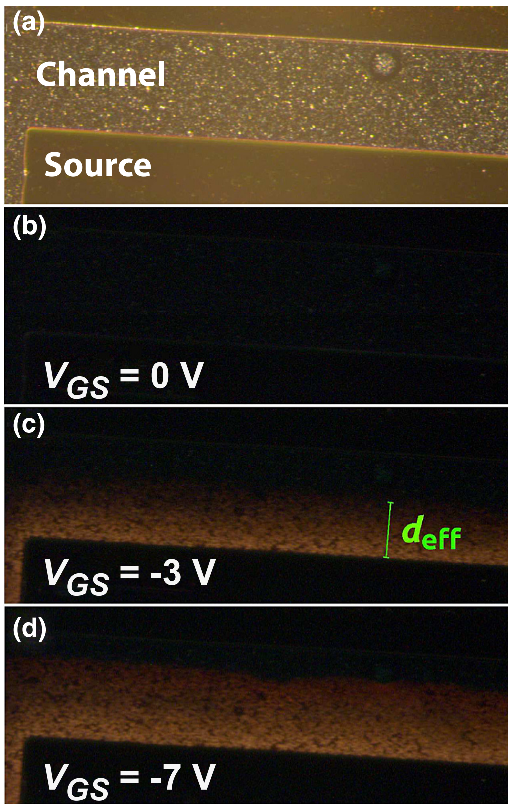

FIG. 6. Light distribution measurement of an Alq_3:DCM (V)OLET ($V_{DS} = -10$ V). (a) Channel region under external illumination. The solid brown areas at the top and bottom are the two adjacent-source electrodes, of which only the bottom one is connected. (b) $V_{GS} = 0$ V (off-state). (c) $V_{GS} = -3$ V (partly on). (d) $V_{GS} = -7$ V (fully on). The exposure time $t_{exp} = 2$ s for (b)–(d).

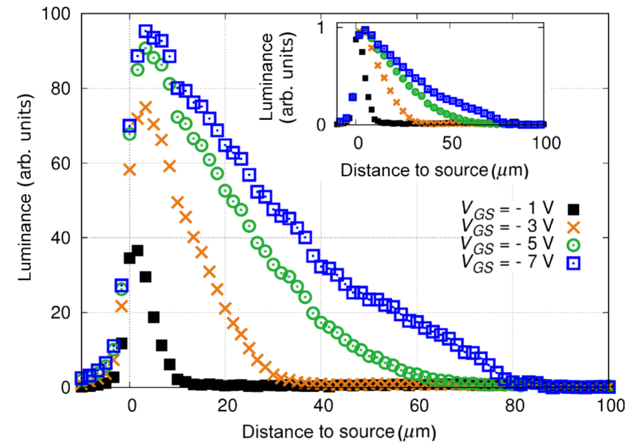

FIG. 7. Light-intensity distribution of an exemplary (V)OLET with 100-nm undoped Spiro-TTB and 25-nm Alq_3. $V_{DS} = -12$ V for all gate biases. Once the transistor is switched on, the light intensity directly at the edge is not increasing significantly. A further increase in gate bias increases the size of the area contributing to the light emission. Inset: Light-intensity distribution normalized to the highest value at the source edge.

Figure 7 shows the intensity distribution of a device with 100-nm undoped Spiro-TTB and 25-nm Alq_3 in the respective layers at $V_{DS} = -12$ V and various gate-source voltages. Like in the simulations, the light emission starts from the edge of the source insulator and decays into the bulk of the device. With the exception of very low gate bias, the absolute light intensity directly at the edge rises just slightly with higher gate-source voltage, whereby the size of the emission zone grows strongly. This effect is even further pronounced in the normalized inset in Fig. 7, which shows clearly that the absolute luminance and, therefore, the total increase in current, is carried by an increase in channel depth. Thus, the simplified relation (8) can be used for comparison with the model.

This dependence on the gate bias supports the findings on charge transport gained from the simulations. A higher gate-source voltage changes the balance between lateral diffusion and vertical drift and, thus, creates a deeper channel. Measurements at different drain-source voltages, however, show a more intricate behavior. Similar to the current distributions in the simulations, exponential functions ($A_0 e^{-x/d_{\mathrm{eff}}}$) can be used to fit the light intensity distribution of the (V)OLETs, where A_0 is the light intensity at the edge. The results for one sample are presented in Fig. 8. The data clearly show a linear dependence of d_{eff} with gate bias. Changing V_{DS} has the same effect as observed in the simulation: the fitted lines are shifted along the ordinate and the slope of the gate-dependence changes. This effect can be described quantitatively using the equations derived earlier.

All optical measurements are carried out in the linear regime of the transistor. Drain-source voltages needed to reach the saturation regime would destroy the insulation on top of the source electrode. According to the IV-characteristics of the single OLED, the diode should be sufficiently switched on and behave like an Ohmic resistance for all applied V_{DS}. The light intensity at each point depends on the current density; therefore, we can exchange j_0 with A_0 and end up with the same set of Eqs. (4)–(8).

Although this model is just a first rough deduction, it describes nicely the linear dependence of the effective channel depth on the gate-source voltage and the shift and change of slope as a function of the drain-source voltage. The agreement between model and measurement is the highest for higher gate-source voltages, where the transistor is switched on and the assumption that the coefficient of the light distribution is independent of V_{GS} is sufficiently satisfied. To test the model, we take a closer look at the dependence of the slopes and intercepts of the linear fits from Fig. 8. The model predicts that the slope of these fits is linear and the intercept negatively quadratic in V_{DS}. The inset in Fig. 8 shows that this prediction is very well fulfilled for the linear dependence of the slope and slightly

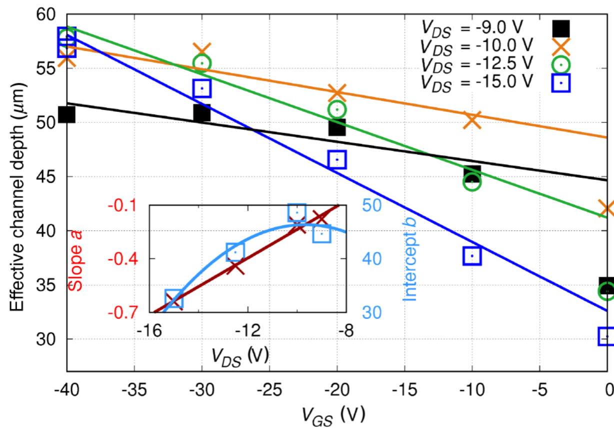

FIG. 8. Effective channel depth obtained from exponential fits of an exemplary (V)OLET with 100-nm undoped Spiro-TTB and 50-nm Alq_3. Except for no or very low gate bias, the dependence on the gate-source voltage shows linear behavior. (The signal is very low for near-zero gate bias; therefore, the inaccuracy is very large.) For increasing drain-source voltage, these linear curves shift to absolute lower channel depth, while the slope increases. Inset: Slope (a) (in red) and intercept (b) (in blue) of the linear fit of the effective channel depth in dependence of the gate voltage ($d_{\mathrm{eff}} = aV_{GS} + b$). Added are a linear fit of the slope in dependence of the drain-source voltage and a quadratic fit of the intercept.

less for the intercept. This finding supports the quality of the model not just in simulations, but for real devices as well.

The channel depths obtained from the devices are much larger than what we see in the simulations. This effect can to a large degree be explained by the charge-carrier balance at the OLED interface. For further investigation, the thicknesses of hole- and electron-transport layers (HTL and ETL, respectively) are varied and the former is doped. A decrease of the topmost Alq_3 layer from 50 to 0 nm decreases the channel depth substantially from 67 ± 1.8 to 4 ± 0.9 μm. However, the total light output of the device with the most shallow channel is also the weakest. This finding can be explained by the dependence of the intensity on the efficiency of the sole OLED and is the highest for the sample with 15 nm of ETL, but lowest for the device without an additional ETL. Decreasing the Spiro-TTB layer thickness from 150 to 100 nm (with an Alq_3 layer of 50 nm) increases the light emission by a factor of 3.25 but does not change the channel depth significantly. However, adding dopants (4 wt % F_6-TCNNQ) to a Spiro-TTB layer of 100 nm (Alq_3 25 nm) decreases the channel depth from 37 ± 1 to 18.1 ± 0.9 μm.

We conclude that the thicker the overall OLED stack, the deeper the channel. This result is easily explainable by the balance between lateral and vertical transport. However, the effect of the layer thickness change of the Alq_3 is much greater than that of the Spiro-TTB. This result can be understood by the different hole and electron mobilities [25,26] of the two materials and the resulting charge-carrier balance at the interface between them [27]. An accumulation of one charge-carrier type (in this case, holes) at the interface can increase the measured channel depth through smearing out the recombination zone. This hypothesis is also supported by the great impact of the doping on the channel depth. In particular, the injection of the holes into the emission zone is increased and, therefore, unwanted accumulation and charge-carrier imbalance are decreased. All these factors will inevitably increase the channel depth in comparison to a transistor without any additional interfaces. The smallest channel depth obtained for a fully switched-on device must hence be an upper limit. Because of the poor transport properties of the Alq_3 and possible interfaces (e.g., between pentacene and Spiro-TTB), the channel depth might be significantly larger in (V)OLETs than in VOFETs. In particular, the large difference between the vertical mobility of pentacene used in the simulations (1×10^{-3} cm^2 V^{-1} s^{-1}) and the mobility of Spiro-TTB used in (V)OLET experiments (5×10^{-5} cm^2 V^{-1} s^{-1}) is expected to lead to an overestimation of channel depth. Finally, even for a fully balanced OLED, the channel depth will be smeared out due to the different lateral and vertical mobilities of the pentacene. Considering the ratio between the mobilities to be 100 and the thickness of the pentacene layer to 25 nm, this would roughly result in a broadening of 2.5 μm. This is close to but lower than the smallest measured channel depth.

IV. SUMMARY

We present an analysis of the working principle of VOFETs deduced from simulations and experiments. Similar to the situation in lateral OFETs, charge carriers are accumulated at the semiconductor dielectric interface and get extracted at the drain. Strong evidence is found that the VOFET acts, in principle, as an OFET, with the only distinction being the short channel length and a special channel geometry. We utilize drift-diffusion simulations and a light-emitting transistor to measure the dimension of the vertical channel in dependence of the bias conditions. Size and shape of the channel area are determined by the gate-source voltage, the drain-source voltage, and the lateral and vertical mobility of the organic semiconductor. We deduce the dependencies of the channel size on gate- and drain-source voltages from the standard FET output characteristics and find good agreement between simulations and experiments. The area of light emission in the (V)OLETs grows with the overall thickness of the OLED stack and the charge-carrier imbalance at the light-emitting interface. From experiments, we find an upper limit for the required distance between adjacent VOFETs of 4 μm. The simulations predict a minimal channel depth of under 1 μm

for pentacene-based VOFETs of this design. This required distance is even lower when driving the device in the saturation regime. Additionally, having a more favorable mobility configuration (e.g., higher vertical than lateral mobility) will decrease the channel size even further. Thus, there is no relevant limit for the integration of vertical organic transistors to be expected within the currently used alignment and patterning limits.

This method of using light emission for charge-carrier path detection could potentially be used for many other vertical design stacks, such as organic permeable-base transistors or VOFETs with nanostructured electrodes [28, 29]. Our findings from experiments and simulations contradict previous reports analyzing charge transport in vertical organic transistors by simulations. In particular, we find strong evidence that the main path of current flow in the vertical direction is in close vicinity to the source insulator. A potential reason for the discrepancy might be the high density of grid points needed for accurate modeling.

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