Simulations of Quantum Transport in Sub-5-nm Monolayer Phosphorene Transistors

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Two-dimensional (2D) semiconductors, e.g., MoS_2 and phosphorene, are promising candidates for the channel materials of next-generation field-effect transistors (FETs). Although 2D MoS_2 FETs with the gate length L_g scaled down to 1 nm have been fabricated with a quite small threshold swing, they suffer from a rather low ON current and are unsuitable for a high-performance device. Herein, we simulate sub-5-nm monolayer (ML) phosphorene MOSFETs using *ab initio* quantum-transport simulations. We predict that the ON current, delay time, and power dissipation indicator of the sub-5-nm double-gated ML phosphorene MOSFETs with proper underlap structure can fulfill the requirements of the international technology roadmap for semiconductors for both high-performance (along both the armchair and zigzag directions) and low-power (along the zigzag direction) devices in 2028 until L_g is scaled down to 2 nm. Therefore, phosphorene is more suitable for ultrascaled FETs than 2D MoS_2 in the post-silicon era as far as the ON current is concerned.

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I. INTRODUCTION

A 5-nm node is believed to be the physical limit of silicon CMOS technology [1–3]. To extend Moore's law down to the sub-5-nm scale, low-dimensional semiconducting materials, such as two-dimensional (2D) transition metal dichalcogenides (TMDs), phosphorene, and one-dimensional (1D) carbon nanotubes (CNTs), have been intensively studied as the potential channel materials of the post-silicon era field-effect transistors (FETs) [1,2,4–8]. Their atomically thin body allows for excellent electrostatic gate control and geometric scaling behavior, and their dangling bond-free surfaces allow for efficient carrier transport [1]. The fast development of nanofabrication technology enables the characteristic length of the FETs based on the low-dimensional semiconductors scaling down to the sub-10-nm and even sub-5-nm regime [9]. Very recently, monolayer (ML) and bilayer MoS_2 FETs [10–13] and CNT FETs [14] with characteristic lengths less than 10 nm have been fabricated.

Although small subthreshold swing (SS) down to 65 mV/dec has been observed [10], the ON currents in the fabricated sub-10-nm 2D MoS_2 FETs are low (<250 μA/μm) [11,13,15], which is consistent with previous predictions [16]. A low ON current means a slow switching speed in the logic device, and such low ON currents in 2D MoS_2 FETs cannot meet the requirements of the international technology roadmap for semiconductors (ITRS) for both high-performance (HP) and low-power (LP) devices in 2024. By contrast, the CNT FETs with a gate length of 5 nm reveal a high ON current as large as approximately 1000 μA/μm [14]. However, the large-scale integration of CNT is still hard to realize [17,18]. Although developed in a rather short period (less than three years) [19–21], the fabricated phosphorene FETs have been scaled down to 20 nm [22]. By similar experimental techniques, realization of sub-10-nm and even sub-5-nm phosphorene FETs can be anticipated. The theoretical calculations reveal that ML black phosphorus (BP) FETs with gate length above 5 nm have excellent device performance, with ON currents superior to the case of ML MoS_2 and meeting the ITRS HP goal of 2024 [23–26], but whether the devices with gate length less than 5 nm can keep this

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excellent performance is unknown. Actually, doubt is even cast on the performance of BP FETs at the sub-5-nm region [27,28]. To check the performance limit of the BP FETs, a rigorous simulation of the sub-5-nm ML BP FETs is needed.

Besides the necessity to study ML BP FETs in the smaller scale, the MOSFET instead of the Schottky barrier FET (SBFET) configuration is suitable to predict the upper device performance. This is because no barrier exists between the electrode and channel regions in the former, while the Schottky barriers in the latter impede the carrier transport. Moreover, to optimize the device performance, the effect of an underlap, i.e., a spacer between the source and gate regions, is worthy of being studied in detail.

In this paper, we simulate sub-5-nm double-gated (DG) ML BP MOSFETs by using rigorous *ab initio* quantum-transport simulations. Owing to the anisotropic nature and large DOS near the VBM of ML BP, excellent gate control is achieved in the p-doped sub-5-nm DG ML BP MOSFETs. Compared with the MoS_2 counterpart, the DG ML BP MOSFET can achieve an up to eight times greater ON current at the gate length of 1 nm along the zigzag direction, implying a faster switching speed. When the gate lengths are scaled down to 2 nm, the ON-state current, delay time, and power dissipation indicator (PDP) of the DG ML BP transistors with proper underlap structure still could fulfill the ITRS goals for the HP (both the armchair and zigzag directions) and LP (zigzag direction) devices in 2028. Such a remarkable device performance makes ML BP a competitive candidate for the channel of FETs in the sub-5-nm nodes.

II. COMPUTATIONAL DETAILS

Transport properties are calculated using the density-functional theory (DFT) coupled with the nonequilibrium Green function (NEGF) formalism, as implemented in the Atomistix ToolKit 2016 package [29]. The drain current at a given bias voltage V_b and gate voltage V_g is calculated through the Landauer-Bűttiker formula [30]:

$$I(V_b,V_g)=\frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E,V_b,V_g)[f_s(E-\mu_s)\times f_d(E-\mu_d)]\}dE, \quad (1)$$

where $T(E, V_b, V_g)$ is the transmission coefficient, f_s and f_d the Fermi-Dirac distribution functions for the source and drain, respectively, and μ_s and μ_d the electrochemical potentials of the source and drain, respectively. The transmission coefficient $T(E)$ is the average of k-dependent transmission coefficients $T^{k_\parallel}(E)$ over the two-dimensional Brillouin zone perpendicular to the transport direction. The direction of the reciprocal lattice vector $k_\parallel$ is vertical to the transport direction. The k-dependent transmission coefficient at energy E is

$$T^{k_{||}}(E)=Tr\{\Gamma_L^{k_{||}}(E)G^{k_{||}}(E)\Gamma_R^{k_{||}}(E)[G^{k_{||}}(E)]^\dagger\}, \quad (2)$$

where $G^{k_{||}}(E)$ $\{[G^{k_{||}}(E)]^\dagger\}$ represents the retarded (advanced) Green function and $\Gamma_{L(R)}^{k_{||}}(E)=i[\sum_{L(R)}^{k_{||}}-(\sum_{L(R)}^{k_{||}})^\dagger]$ represents the level broadening originating from the left (right) electrode expressed in terms of the electrode self-energy $\Sigma_{L(R)}^{k_\parallel}$ [31,32]. The self-energy is calculated using an exact diagonalization of the Hamiltonian [33].

A single ζ plus polarization (SZP) basis set is adopted. A higher double ζ plus polarization (DZP) basis set is tested, with consistent results obtained from those of SZP, as shown in Fig. S1 [34]. Generalized gradient approximation (GGA) in the form of the Perdew-Burke-Ernzerhof (PBE) functional is employed to describe the exchange and correlation interaction [35]. Because of the heavily screened electron-electron interaction by doping carriers, DFT GGA-based single-electron approximation is good in the description of the device electronic structure [3,4,6,36]. $\boldsymbol{k}$-point meshes [37] are sampled with a separation of about 0.01 $Å^{-1}$ in the Brillouin zone. The real-space mesh cutoff is 75 hartree, and the temperature is set to 300 K. The effective mass of ML phosphorene calculated by our method is in good agreement with previous works [1,7,8], as shown in Table S1 [34].

III. RESULTS AND DISCUSSION

The lattice parameters of ML BP are $a=4.62$ Å and $b=3.35$ Å. A two-probe model of the DG ML BP MOSFET is constructed with intrinsic ML BP as the channel and degenerately doped ML BP as the electrode, as shown in Fig. 1(a). Because of the anisotropic electronic properties of ML BP, both the armchair and zigzag directions of BP have been considered as the transport directions in the MOSFETs. The leads of the model are explicitly represented in the DFT calculation. The leads are semi-infinite and parts of them are present in the schematic model. The orientation of the lead is consistent with the channel. Underlap (UL) configuration, which is the spacer between the gate and source (or drain), has been considered with length ranging from 0 to 4 nm.

We focus on p-type doping in our simulations, because of the higher anisotropy degree of holes than that of electrons in ML BP and easier experimental realization of p doping of BP due to its small work function [2,7]. The doping concentration of the source and drain are 4.0×10^{13} cm^{-2}, which can be obtained in experiments with layered materials [38]. Details of the doping method are provided in the Supplemental Material. The equivalent oxide thicknesses (EOTs) in the MOSFETs are set to 0.43–0.49 nm, a range close to the ITRS requirement. The oxide constant is 4.3. Estimated with a vacuum thickness

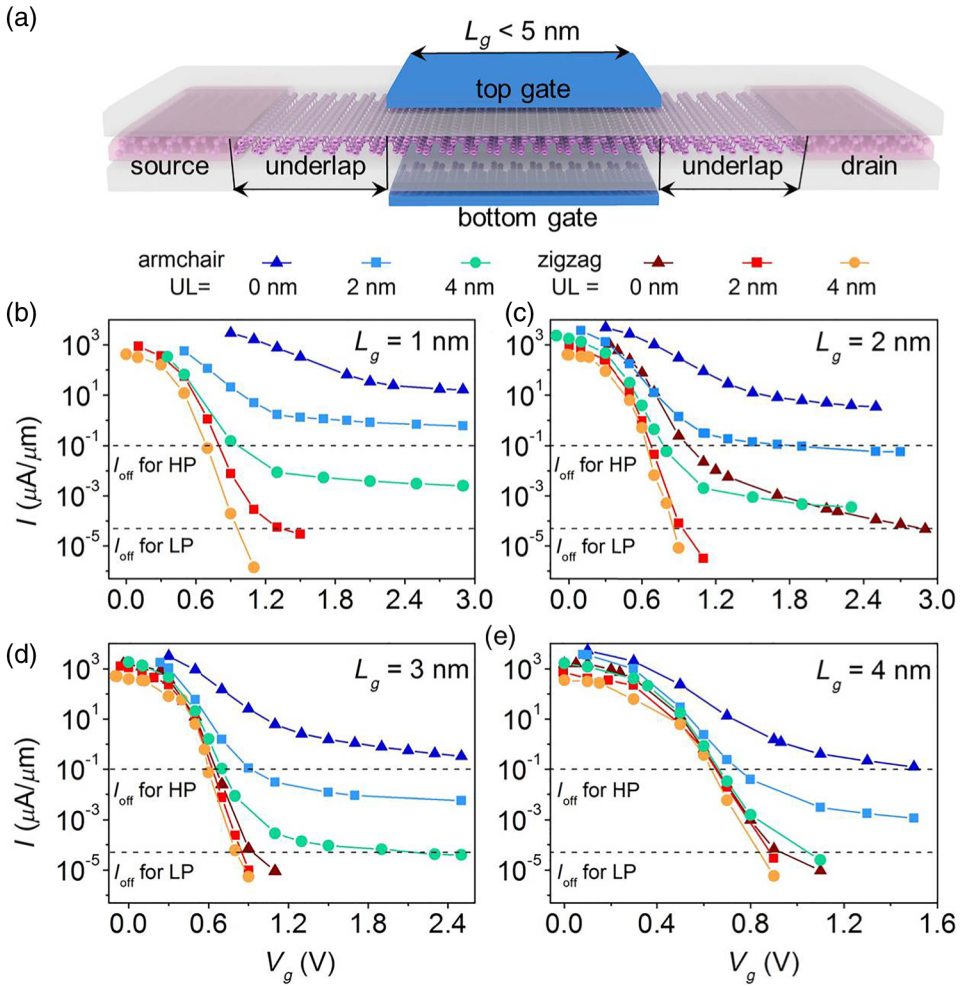

FIG. 1. (a) Schematic view of the DG ML BP MOSFET. (b)–(e) I-V_g characteristics of the p-type DG ML BP MOSFETs at bias of $V_b = 0.69$ V along the armchair and zigzag directions with different ULs and gate lengths, respectively. The blue and translucent regions stand for gate electrode and dielectric layer, respectively.

of 100 Å, the dielectric constant of the ML phosphorene calculated at the PBE level is 1.8 along the armchair direction, 1.7 along the zigzag direction, and 1.1 along the out-of-plane direction. These calculated dielectric constants for ML phosphorene are close to the reported values estimated with similar vacuum thickness at the Heyd-Scuseria-Ernzerhof hybrid functional (HSE) level [6].

The typical transfer characteristics of the p-type sub-5-nm DG ML BP MOSFETs at a bias of $V_b = 0.69$ V along the armchair and zigzag directions with different gate length L_g and ULs are shown in Figs. 1(b)–1(g). Maximum drain currents around the order of 10^3 μA/μm are observed in all the sub-5-nm DG ML BP MOSFETs. At a given V_g, the currents of the armchair-directed devices are generally higher than those of the zigzag-directed ones due to the smaller hole effective mass ($m_x = 0.16m_0$ vs $m_y = 5.40m_0$) and higher carrier mobility in the armchair direction of ML BP. The difference in the maximum drain current between the armchair- and zigzag-directed sub-5-nm DG ML BP MOSFETs is less than one order of magnitude but that in the minimum leakage current is up to 10^5. It is noted that the phosphorene's anisotropic effective mass can be used to suppress direct source-to-drain tunneling leakage in the ultrascaled MOSFET and to obtain a large ON:OFF ratio in the ultrascaled L-gate tunnel FET (TFET) [39]. The application of UL leads to the reduction of drain current, and this drain-current reduction is more apparent in the armchair direction and the subthreshold region than in the zigzag direction and the superthreshold region. The key figures of merit of the simulated sub-5-nm DG ML BP MOSFETs are summarized in Tables S2 and S3 [34].

A. Gate control

Subthreshold swing is an important indicator of the gate electrostatics in the subthreshold region, and the values of the sub-5-nm DG ML BP MOSFETs are shown in Fig. 2(a). It is shown that the zigzag-directed DG ML BP MOSFET exhibits a better subthreshold electrostatics with SS about half of that of the armchair-directed one, given the same L_g and UL. This is because SS primarily relates to the subthreshold characteristics and is greatly affected by the leakage current. Compared with the case of the armchair direction, the effective mass in the zigzag

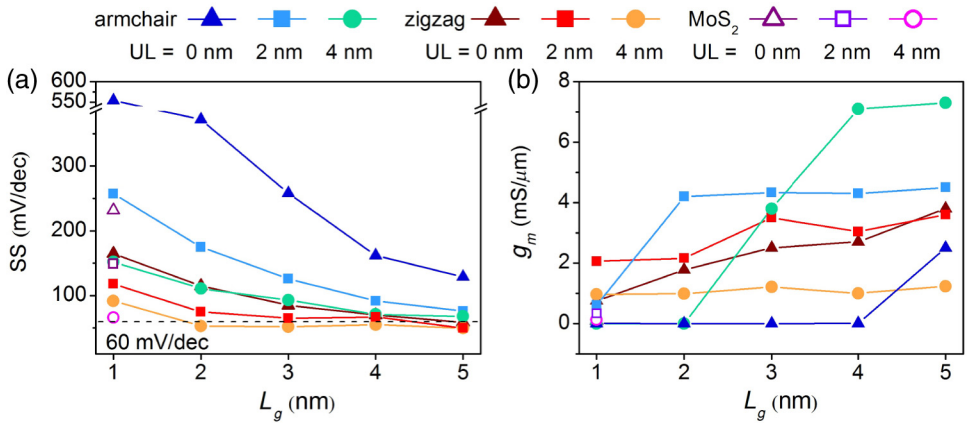

FIG. 2. SS and g_m as a function of the gate length in the armchair- and zigzag-directed DG ML BP MOSFETs with different ULs, respectively. The data from the simulated DG ML MoS_2 MOSFETs at $L_g = 1$ nm with different ULs are shown for comparison. The black dashed line in (a) indicates the Boltzmann limit of 60 mV/dec for SS at room temperature.

direction of BP is larger, and the transmission rate is thus lower, leading to the suppressed source-to-drain leakage and thus reduced SS. The SS of the armchair-directed DG ML BP MOSFETs degrades faster with the reduced gate length than the zigzag-directed devices.

Introduction of the UL structure improves the subthreshold electrostatics of the sub-5-nm DG ML BP MOSFETs in both the armchair and zigzag directions because it increases the effective channel length and thereby suppresses the source-to-drain leakage. The improvement of SS with the 4-nm UL is more significant than that with the 2-nm UL. For the armchair-directed devices, the UL leads to a 41%–73% reduction of SS. The adoption of the 4-nm UL improves the SS of the armchair-directed sub-5-nm DG ML BP MOSFETs from 129–554 mV/dec to 68–192 mV/dec. For the zigzag-directed ones, the effect of UL on the SS is not apparent at $L_g = 4$ or 5 nm but becomes significant when $L_g < 4$ nm.

It is noted that SS lower than 60 mV/dec (50–59 mV/dec) is observed in several zigzag-directed DG ML BP MOSFETs. The sub-10-nm ML arsenene MOSFET is also calculated to have SS down to 55 mV/dec [40]. Generally, 60 mV/dec is believed to be the fundamental limit of SS in MOSFETs at room temperature, termed Boltzmann's tyranny. This limit is true for conventional MOSFETs with long channels in the μm range, since the current is mainly from the thermionic injection. However, in the MOSFETs with an ultrashort channel down to a few nm, the tunneling current apparently cannot be neglected. In this case, achieving a SS lower than 60 mV/dec is possible.

Considering both the tunneling and thermionic currents $I = I_{\text{tunnel}} + I_{\text{therm}}$ at a V_g where the transfer characteristic curve is the steepest (i.e., close to the state where the SS value is estimated), the subthreshold swing can be expressed as follows:

$$\text{SS} = \left(\frac{\partial lgI}{\partial V_g}\right)^{-1} = [r_{\text{tunnel}}\text{SS}_{\text{tunnel}}^{-1} + (1 - r_{\text{tunnel}})\text{SS}_{\text{therm}}^{-1}]^{-1}, \quad (3)$$

where

$$\text{SS}_{\text{tunnel}} = \left(\frac{\partial lgI_{\text{tunnel}}}{\partial V_g}\right)^{-1}, \quad \text{SS}_{\text{therm}} = \left(\frac{\partial lgI_{\text{therm}}}{\partial V_g}\right)^{-1},$$

$$\text{and } r_{\text{tunnel}} = \frac{I_{\text{tunnel}}}{I},$$

respectively. When $r_{\text{tunnel}} = 0$, the current is all from thermionic injection, and $\text{SS} = \text{SS}_{\text{therm}}$, setting the lowest limit to 60 mV/dec; when $r_{\text{tunnel}} \neq 0$, the tunneling current cannot be neglected, and a SS value lower than 60 mV/dec is possible.

To illustrate this possibility clearly, we take the zigzag-directed DG ML BP MOSFET with $L_g = 3$ nm and UL = 4 nm as an example (Fig. S2(a) [34]). First, the significant contribution of I_{tunnel} to the total current is observed ($r_{\text{tunnel}} \approx 0.9$) at $V_g = 0.6$ V. Second, the average channel barrier height ϕ_B, which is the energy difference between the chemical potential of the source electrode μ_s and the lowest channel VBM, decreases rapidly from 0.28 to 0.10 eV with a V_g variation of 0.2 V. This decrease of ϕ_B will lead to a substantial increase of I_{tunnel}, as $I_{\text{tunnel}} \propto e^{-w\sqrt{m^*\phi_B}}$, where w is the barrier width [41]. Thus, the value of $\text{SS}_{\text{tunnel}}$ could be extremely small. In fact, a necessary condition for SS < 60 mV/dec is $\text{SS}_{\text{tunnel}} < \text{SS}_{\text{therm}}$ when $0 < r_{\text{tunnel}} < 1$ (see Supplemental Material for details [34]). The large percentage of I_{tunnel} and extremely small value of $\text{SS}_{\text{tunnel}}$ collectively result in a very small total SS of 52 mV/dec in this zigzag-directed DG ML BP MOSFET. As the gate voltages modulate amplitudes for quantum tunneling, the device has begun to act as a TFET. However, it is inter-band tunneling in the traditional TFETs but inner-band tunneling in the studied sub-5-nm ML BP MOSFETs here.

Keeping in mind that only the significant contribution of the tunneling current alone cannot guarantee a SS < 60 mV/dec. An extreme example is the case of the armchair-directed MOSFET with $L_g = 1$ nm and UL = 0 nm (Fig. S2(b) [34]), whose SS is 554 mV/dec though its current is nearly all from tunneling ($r_{\text{tunnel}} \approx 1$).

In contrast with the zigzag-directed case, ϕ_B remains almost constant, and I_{tunnel} changes less than 0.01 μA/μm under a V_g variation of 0.2 V, leading to a large value of SS_{tunnel} and thus the large total SS in this armchair-directed MOSFET.

Transconductance g_m measures the gate electrostatics in the superthreshold region. As shown in Fig. 2(b), the transconductance degrades from 2.5 to approximately 10^{-3} mS/μm and 3.8 to 0.8 mS/μm with the decreasing L_g for the armchair- and zigzag-directed DG ML BP MOSFETs without UL, respectively. In the armchair-directed devices, the use of 4-nm UL always improves the superthreshold gate control, with g_m increasing to 0.6–4.5 mS/μm. With UL = 2 nm, g_m is improved to as large as 7 mS/μm at 3 nm $< L_g \leq$ 5 nm, but nearly no improvement at $L_g \leq$ 3 nm. In the zigzag-directed devices, the degradation trend of g_m with shorter L_g becomes slower after adopting a UL of 2 nm. However, at a given L_g, the improvement of g_m value by using UL is not as significant as the armchair-directed cases. The UL of 4 nm even leads to a 45%–68% decrease of g_m at $L_g >$ 1 nm compared with the case without UL in the zigzag-directed devices.

B. ON current

In a digital device, a high ON-state current is desired to maximize the switching speed of logic transitions. The introduction of UL makes the channel barrier longer and transmission possibility $T(E)$ smaller, suppressing the tunneling leakage current; this is advantageous to device performance. On the other hand, the control of the gate to the UL part of the channel is not as strong as the overlap part; this is a disadvantage to device performance. Therefore, the length of the UL has to be optimized to achieve the best device performance. Figure 3 shows the ON-state current of the sub-5-nm DG ML BP MOSFETs at different gate lengths and ULs. The OFF currents are fixed to 0.1 and 5×10^{-5} μA/μm according to the ITRS standards for the HP and LP applications in 2028, respectively, and the supply voltage is set to 0.69 V.

As shown in Fig. 3(a), the optimal UL is 2 nm at 3 nm $\leq L_g \leq$ 5 nm while 4 nm at $L_g <$ 3 nm for the armchair-directed DG ML BP MOSFETs in the HP application. In the absence of UL, the ON current of the armchair-directed DG ML BP MOSFETs at L_g = 5 nm (1373 μA/μm) can meet the ITRS goal of 900 μA/μm for the HP applications but drop rapidly to only approximately 1 μA/μm at L_g = 4 nm and fail to meet the ITRS requirement. With UL = 2 nm, the ON currents of the armchair-directed DG ML BP MOSFETs can meet the ITRS goal until L_g = 3 nm (I_{on} = 1760–4500 μA/μm). With a longer UL of 4 nm, the ON currents of the armchair-directed DG ML BP MOSFETs can meet the ITRS goal until L_g = 2 nm (I_{on} = 1800–2293 μA/μm).

Unlike the armchair-directed ones, the sub-5-nm zigzag-directed HP devices show the largest ON current of 1052–2200 μA/μm in absence of UL (except for L_g = 1 nm) [Fig. 3(b)]. With UL = 0 nm, the ON currents of the zigzag-directed DG ML BP MOSFETs can meet the ITRS HP goal until L_g = 2 nm. With UL = 2 nm, the ON currents of the zigzag-directed MOSFETs fluctuate around the ITRS goal and surprisingly reach as high as 860 μA/μm even at L_g = 1 nm, which is quite close

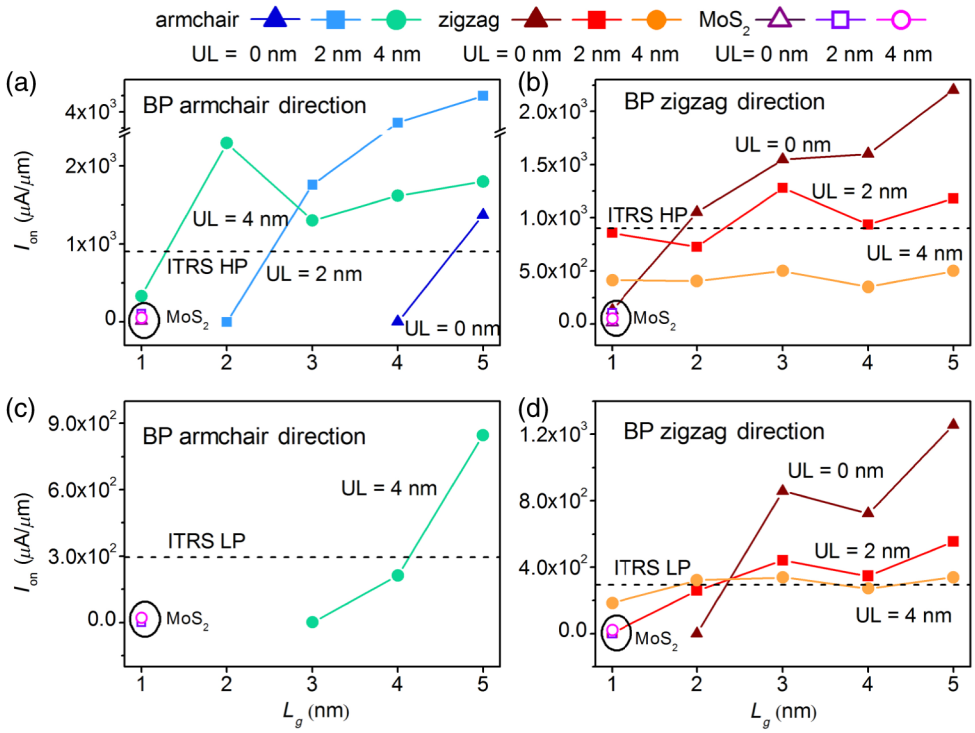

FIG. 3. (a)–(d) ON-state current as a function of the gate length in the armchair- and zigzag-directed DG ML BP MOSFETs for the HP (a),(b) and LP (c),(d) applications. Black dashed lines represent the ITRS HP and LP requirements in 2028. The data of the simulated DG ML MoS_2 MOSFET at L_g = 1 nm with different ULs are also shown for comparison.

to the ITRS goal of 900 μA/μm. With UL = 4 nm, the ON currents (350–500 μA/μm) of the zigzag-directed DG ML BP MOSFETs only fulfill 39%–56% of the ITRS requirement.

To illustrate the function of UL more clearly, we have computed the LDOS and transmission spectra of the 1-nm-gate zigzag-directed DG ML BP MOSFETs with different ULs. In Fig. 4, a maximum hole-barrier height ϕ_{max} is defined as the energy barrier for the holes of the distribution tail at the VBM ($E = -0.25$ eV) to transport from the source to drain. The barriers for all the source holes inside the bias window are not larger than ϕ_{max}. At the HP OFF state with the same current of 0.1 μA/μm, ϕ_{max} decreases from 0.69 eV at UL = 0 nm to 0.50 eV and 0.49 eV at UL = 2 nm and 4 nm, respectively. At the HP ON state, I_{ON} with the 2-nm UL case is the highest, followed by the case with UL = 4 nm, and I_{ON} in the one without UL is the lowest. The low ON current in the case without UL is because the barrier at the OFF state is so high that the supply voltage of 0.69 V is not able to drive the VBM upward enough to make the barrier diminish and there is still a ϕ_{max} of 0.23 eV at the ON state. With UL = 4 nm, the UL region far from the gate is not effectively controlled by the gate electrode, and the VBM of the left UL region close to the source has not been pushed up efficiently by the gate, leaving a small ϕ_{max} of 0.17 eV. By contrast, ϕ_{max} nearly vanishes in the case of UL = 2 nm due to a collective effect of small ϕ_{max} in the OFF state and moderate UL. Correspondingly, the ON-state transmission spectra edge at UL = 2 nm is the upmost within the bias window, leading to the highest ON current in the 1-nm-gate length zigzag-directed DG ML BP MOSFET.

Next, we study the sub-5-nm BP MOSFETs for LP applications. An ultralow OFF-state current is required as saving static energy is a major concern for LP applications. Therefore, the ON current of the LP applications relies mainly on the subthreshold characteristic of the MOSFET. For the armchair-directed MOSFETs shown in

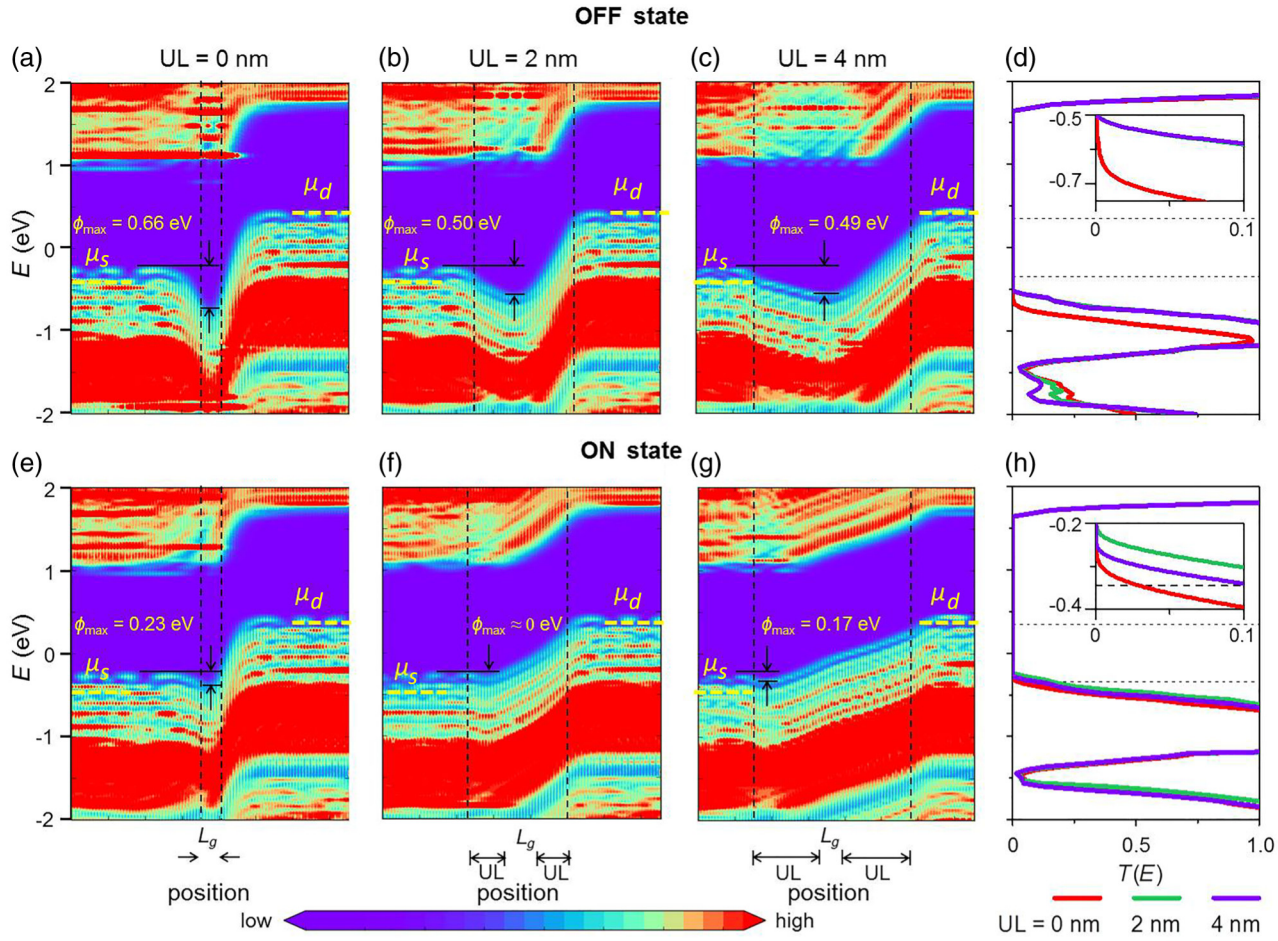

FIG. 4. (a)–(h) Spatial resolved LDOS and transmission spectra of the zigzag-directed 1-nm-L_g DG ML BP MOSFETs under $V_b = 0.69$ V with different UL at the HP OFF (a)–(d) and ON states (e)–(h), respectively. Transmission spectra near the VBM of BP are shown in the insets in (d) and (h). μ_s and μ_d are the electrochemical potential of the source and drain, respectively. ϕ_{max} is the energy barrier for the holes of the distribution tail at the VBM ($E = -0.25$ eV) to transport from the source to drain. The HP OFF state has a current of 0.1 μA/μm, and the ON state is the state with a gate difference of $V_{dd} = 0.69$ V to the OFF state.

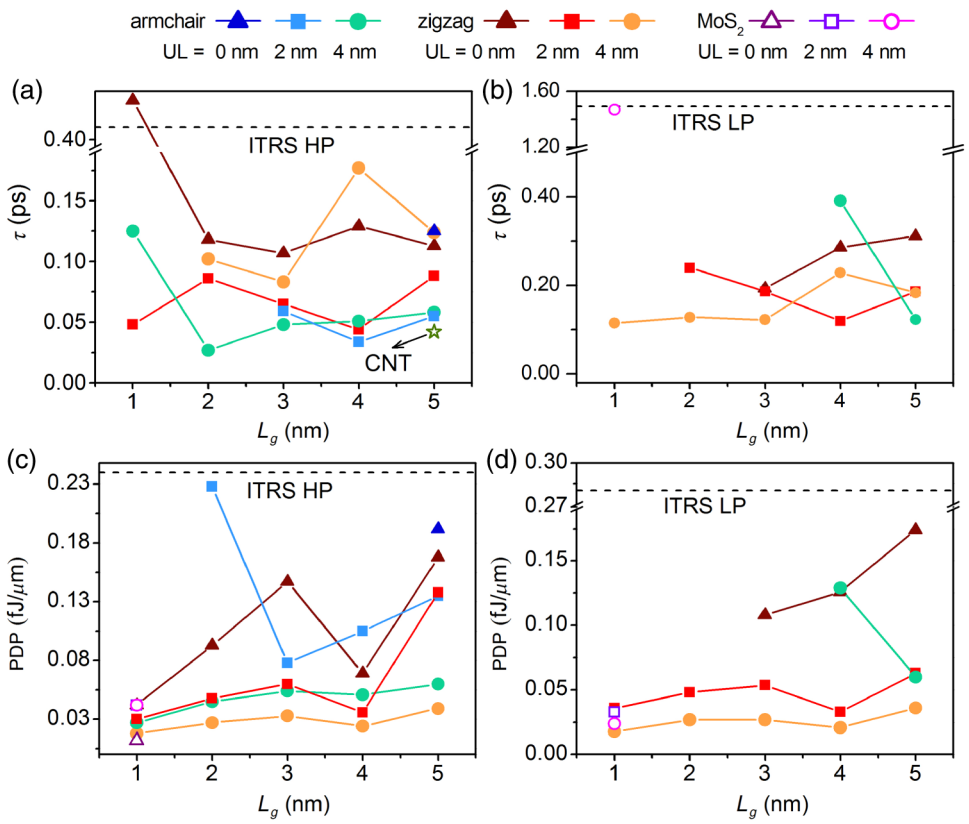

FIG. 5. (a),(b) Intrinsic delay time and (c),(d) power dissipation as functions of the gate length in the armchair- and zigzag-directed DG ML BP MOSFETs with UL = 0, 2, and 4 nm, respectively. Black dashed lines are the ITRS HP and LP requirements for τ and PDP in 2028, respectively. Only the delay time and PDP of the DG ML BP MOSFETs that meet or are close to the ITRS requirements are shown. For details, please check Tables S1 and S2. Delay time of the experimental 5-nm-gate-length CNT transistor (star) from Ref. [14] is also provided in (a).

Fig. 3(c), only the one with $L_g = 5$ nm and UL = 4 nm ($I_{on} = 847$ μA/μm) can meet the ITRS LP ON-current requirement of 295 μA/μm. For the zigzag-directed MOSFETs shown in Fig. 3(d), the optimal UL is 0 nm at 3 nm $\leq L_g \leq 5$ nm, while it is 4 nm at $L_g < 3$ nm. With UL = 0 and 2 nm, the ON currents of the zigzag-directed DG ML BP MOSFETs meet the ITRS LP goal until $L_g = 3$ nm ($I_{on} = 442$–857 μA/μm). With UL = 4 nm, the ON currents of the zigzag-directed MOSFETs range around the ITRS LP requirement and can meet the ITRS requirement at $L_g = 2$ nm ($I_{on} = 323$ μA/μm).

C. Delay time and power consumption

Switching speed is an essential figure of merit for a digital circuit. The switching speed is usually measured by the intrinsic delay time, which is calculated by the formula:

$$\tau = C_{total} V_{dd} / I_{on}, \quad (4)$$

where C_{total} is the total gate capacitance, V_{dd} the supply voltage, and I_{on} the ON-state current. C_{total} is the sum of intrinsic gate capacitance C_g and fringing capacitance C_f, and C_f is assumed to be double that of C_g in accordance to the ITRS requirements. Noticeably, using Eq. (3), only the delay time of the device with a well-defined I_{on} (lowest current of this device is below the ITRS HP or LP OFF current) can be calculated. The total gate capacitance of the armchair- and zigzag-directed devices are 0.06–0.48 fF/μm and 0.03–0.48 fF/μm, respectively, lower than both the ITRS HP (0.60 fF/μm) and LP (0.69 fF/μm) requirements.

Figure 5 shows the intrinsic delay time and PDP of the DG ML BP MOSFETs that meet the ITRS requirement. Detailed values of all devices are provided in Tables S2 and S3. As a result of the small C_{total} and high ON current, the intrinsic delay time is generally small, indicating a fast switching speed. For the HP applications, the use of UL significantly improves the switching speed of the armchair-directed devices. The delay times of the armchair-directed devices with UL = 0 nm only meet the ITRS goal of 0.423 ps at $L_g = 5$ nm (0.166 ps) and increase suddenly to 228 ps at $L_g = 4$ nm. With UL of 2 and 4 nm, the delay times of the armchair-directed devices decreases to 0.034–0.059 ps ($L_g = 3$–5 nm) and 0.027–0.125 ps ($L_g = 1$–5 nm), respectively, meeting the ITRS HP standards until $L_g = 3$ and 2 nm, respectively. Along the zigzag direction, the delay times of all the sub-5-nm DG ML BP MOSFETs with UL = 0–4 nm (0.044–0.481 ps) meet the ITRS HP standards except for the one with UL = 0 nm and $L_g = 1$ nm. Remarkably, the delay times of the simulated DG ML BP MOSFET with UL of 2 and 4 nm (0.055–0.058 ps) in the armchair direction at $L_g = 5$ nm are close to the reported 0.046 ps in the experimental 5-nm gate-length CNT transistor [14].

For the LP applications, the delay times of the armchair-directed devices with UL = 4 nm meet the ITRS goal of 1.493 ps at $L_g = 4$ and 5 nm (0.122–0.391 ps), but

increase sharply to approximately 10^5 ps at $L_g = 3$ nm due to the extremely low I_{on} of approximately 10^{-4} μA/μm. Along the zigzag direction, the delay times of the DG ML BP MOSFETs with UL = 0 nm are much lower than the ITRS LP goal at $L_g = 3$–5 nm (0.193–0.311 ps) but increase sharply to 10^5 ps at $L_g = 2$ nm. With UL = 2 and 4 nm, the delay times in the zigzag-directed devices fulfill the ITRS LP standard until $L_g = 2$ and 1 nm, respectively.

Besides speed, power consumption is important for digital applications. Power efficiency can be measured by power dissipation indicator, which is determined as PDP $= (Q_{on} - Q_{off})V_b/W$ (Q_{on} and Q_{off} are the total charges in the ON and OFF states, and W the channel width, respectively). In Figs. 5(c) and 5(d), the PDP shows a strong monotonous decreasing trend with increasing UL. Notably, the calculated PDP of all the checked sub-5-nm DG ML BP MOSFETs with minimum current $I_{min} < 0.1$ μA/μm are significantly lower (0.027–0.228 fJ/μm), compared with the ITRS HP goal of 0.24 fJ/μm. For the LP applications, the PDP of the x-directed sub-5-nm DG ML BP MOSFETs only in the $L_g = 4$–5 nm and UL = 4 nm cases (0.060–0.129 fJ/μm) can meet the ITRS goal of 0.28 fJ/μm. Along the y direction, the PDP meets the ITRS LP standard only at $L_g = 3$–5 nm in the absence of UL (0.108–0.174 fJ/μm) but meets it at $L_g = 1$–5 nm with resort of UL.

To evaluate how good the device is in a real circuit with interconnects and parasitic capacitances, energy-delay calculations of a 32-bit adder circuit based on the sub-5-nm ML BP MOSFET are performed. The 32-bit adder simulation is performed using the software BCB 3.0 [42,43]. In the energy-delay figure (Figs. S3 and S4 [34]), the bottom left corner with the lowest energy-power product (EDP) is preferred.

For HP applications, EDPs of the 32-bit adders based on the armchair-directed sub-5-nm ML BP MOSFETs with UL = 4 nm and all the studied zigzag-directed MOSFETs are better than those based on the ITRS HP standard, similar to the case of intrinsic ones. In particular, the variation of EDP of the adders based on the zigzag-directed MOSFETs with UL = 4 nm is less than two times. For LP applications, EDP of the 32-bit adder remains to be better than the ITRS standard if the intrinsic EDP is better than the ITRS standard. The variation of EDP of the 32-bit adders based on the zigzag-directed MOSFETs with UL = 4 nm is also less than two times like the HP case. Such a small deviation of EDP might be beneficial for achieving a uniform device performance for massive production.

D. Benchmark against the simulated DG ML MoS_2 MOSFETs

It is instructive to compare the key figures of merit of the simulated DG ML BP MOSFETs with those of the simulated DG ML MoS_2 MOSFETs at the ultimate gate length. N-type doping is applied for ML MoS_2 with a concentration of 4.0×10^{13} cm^{-2} since it is typically observed due to a large work function of MoS_2. Different ULs ranging from 0 to 4 nm are considered to optimize device performance. The simulated transfer characteristics of the n-type ML MoS_2 MOSFETs at $L_g = 1$ nm are shown in Fig. 6(a). The simulated SS of the 1-nm-gate-length ML MoS_2 MOSFETs is as large as 232 mV/dec without UL and is significantly improved to 149 and 66 mV/dec with a UL of 2 and 4 nm, respectively.

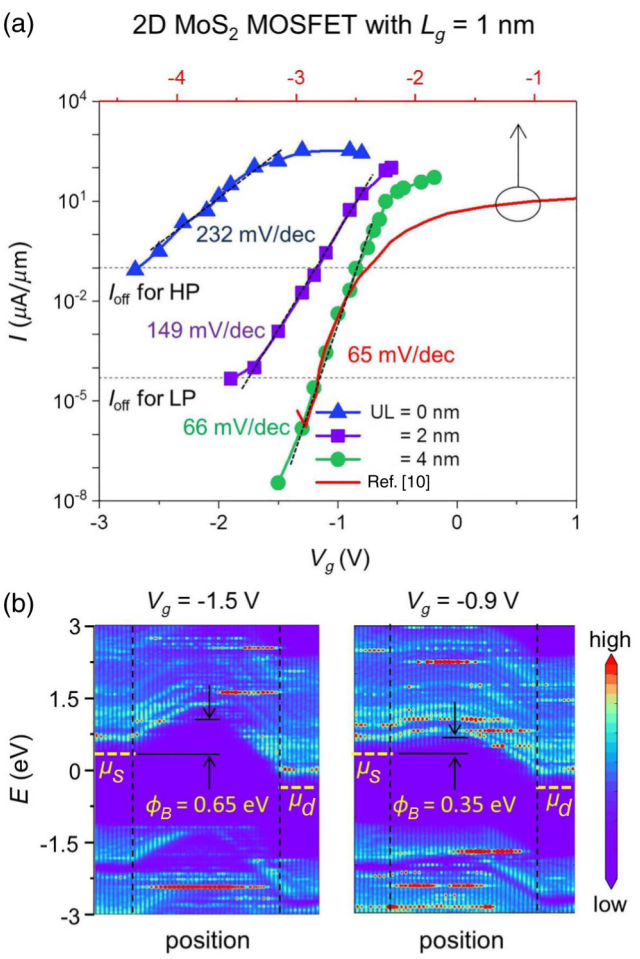

FIG. 6. (a) Simulated transfer characteristics of the DG ML MoS_2 MOSFETs with $L_g = 1$ nm and different ULs at $V_b = 0.69$ V, which is benchmarked against the experimental data (red solid line) of the 1-nm-gate-length 2D MoS_2 MOSFETs. Reprinted in part with permission from Ref. [10]. Copyright 2016 American Association for the Advancement of Science. (b) LDOS of the DG ML MoS_2 MOSFETs with $L_g = 1$ nm and UL = 4 nm at $V_g = -1.5$ (left panel) and -0.9 V (right panel). μ_s and μ_d are the electrochemical potential of the source and drain, respectively. Vertical dashed lines are the edges between the electrode and channel regions.

Remarkably, the overall transfer characteristic of the simulated 1-nm-gate-length DG ML MoS_2 with UL = 4 nm shows an agreement with the experimental result [red line in Fig. 6(a)], especially in the subthreshold region [10]. The simulated SS of 66 mV/dec is in good agreement with the experimental one of 65 mV/dec in the 1-nm-gate-length MoS_2 FET [10]. Such an agreement validates the reliability of our simulations. The maximum current of the simulated one with UL = 4 nm is several times greater than that of the experimental one. This discrepancy is ascribed to the fact that the MOSFET model is adopted in our simulation with Ohmic contact features and ideal ballistic transport, while the experimental MoS_2 FET has metal electrodes and a rather long channel (9 nm in theory vs 1 μm in experiment), which cause the Schottky barrier and scattering effect, respectively (both factors decrease the maximum current).

The optimal SS of 66 mV/dec in the simulated DG ML MoS_2 MOSFETs at UL = 4 nm are superior to that of the simulated armchair-directed DG ML BP MOSFETs (152 mV/dec at UL = 4 nm) and even better than that of the zigzag-directed ones (92 mV/dec at UL = 4 nm). The nice gate control of the 1-nm-gate-length DG ML MoS_2 MOSFET in the subthreshold region can be attributed to the large change of the channel conduction-band minimum (CBM) with V_g. Take the 1-nm-gate-length DG ML MoS_2 MOSFET with UL = 4 nm in Fig. 6(b) as an example. By comparing the LDOS between the states at $V_g = -1.5$ and -0.9 V, a CBM movement of 0.50 eV/V by gate is estimated in the DG ML MoS_2 MOSFET, slightly larger than that of the zigzag-directed DG ML BP MOSFET (0.46 eV/V) at $L_g = 1$ nm and UL = 4 nm. However, in the superthreshold region, the gate control of the DG ML MoS_2 MOSFET is poorer than that of both the armchair- and zigzag-directed DG ML BP MOSFETs. The largest transconductance of 0.34 mS/μm in the 1-nm-gate-length DG ML MoS_2 MOSFETs (at UL = 2 nm) is only 1/2 and 1/6 of those of the armchair- and zigzag-directed ML BP cases, respectively (Fig. 2).

The smaller transconductance leads to a smaller ON current. Since the minimum current of the armchair-directed DG ML BP MOSFETs at $L_g = 1$ nm is larger than the ITRS HP and LP OFF-current standard in most cases, the well-defined ON current and delay time are lacking in these armchair-directed devices. Therefore, we compare I_{on} and delay time of the 1-nm-gate-length DG ML MoS_2 MOSFETs with those of the zigzag-directed DG ML BP MOSFETs. The optimal ON current of the 1-nm-gate-length DG ML MoS_2 MOSFETs is 102 (at UL = 2 nm) and 21 μA/μm (at UL = 4 nm) for the HP and LP applications, respectively, which are apparently smaller than the corresponding values of 860 (at UL = 2 nm) and 180 μA/μm (at UL = 4 nm) of the zigzag-directed ML BP counterparts. The optimal ON currents in the DG ML MoS_2 MOSFET only fulfill 11 and 7% of the ITRS goals for the HP and LP applications, respectively, while they fulfill 96 and 61% in the BP case (zigzag direction), respectively (Fig. 3).

The lower ON currents of the DG ML MoS_2 MOSFETs make their delay time much longer. As shown in Figs. 5(a) and 5(b), the optimal delay times are $\tau = 0.23$ ps (at UL = 2 nm) and 0.49 ps (at UL = 4 nm) for the HP and LP applications in the DG ML MoS_2 devices, while they are 0.02 ps (at UL = 2 nm) and 0.05 ps (at UL = 4 nm) for the HP and LP applications in the zigzag-directed ML BP devices. Correspondingly, the switching speeds of the DG ML MoS_2 MOSFET are much slower than those of the DG ML BP cases at $L_g = 1$ nm. However, the PDP of the 1-nm-gate-length ML MoS_2 and BP MOSFETs are in a similar range of 0.004–0.014 fJ/μm [Figs. 5(c) and 5(d)]. This low power consumption of the DG ML MoS_2 MOSFETs might be related to its nice subthreshold gate control.

The larger transconductance in the p-type DG ML BP MOSFETs than those of the n-type DG ML MoS_2 MOSFETs is attributed to the higher DOS near the VBM of ML BP than those near the CBM of ML MoS_2. The DOS obeys the relation

$$\mathrm{DOS} = \frac{g_s g_v}{2\pi\hbar^2}\sqrt{m_x m_y}, \tag{5}$$

where $m_x = 0.16m_0$ and $m_y = 5.40m_0$ for the holes in the infinite ML BP and $m_x = m_y = 0.45m_0$ for the electrons in the infinite ML MoS_2 (the subscripts x and y stand for the armchair and zigzag directions, respectively). The anisotropic effective mass in ML BP make its DOS near the VBM twice that in ML MoS_2 near the CBM, given the same spin and valley degeneracies g_s and g_v. A large DOS of the infinite ML BP will lead to a large partial DOS (PDOS) of the ML BP channel in the device [23].

Given a large PDOS of the channel, only a small variation of the gate voltage ΔV_g is needed to drive a certain variation of the channel charge ΔQ_{ch}, leading to a large transconductance g_m in terms of the equation

$$g_m \propto v_{\mathrm{eff}}\frac{\Delta Q_{ch}}{\Delta V_g}, \tag{6}$$

where v_{eff} is the effective carrier velocity in the channel [27]. By contrast, the FETs with a low-channel PDOS may suffer from a depressed control effect in the superthreshold region, which is the so-called DOS bottleneck. Although the transport effective mass of the zigzag-directed DG ML BP MOSFET is large and thus the effective carrier velocity v_{eff} is small, the positive effect of the large DOS on $\Delta Q_{ch}/\Delta V_g$ overcompensates the negative influence of the large effective mass on v_{eff}. Therein, not only the armchair-directed but also the zigzag-directed DG ML BP MOSFETs show g_m larger than that of the DG ML MoS_2 MOSFET at $L_g = 1$ nm.

The larger DOS of ML BP also contributes to the higher ON currents of both the armchair- and zigzag-directed ML

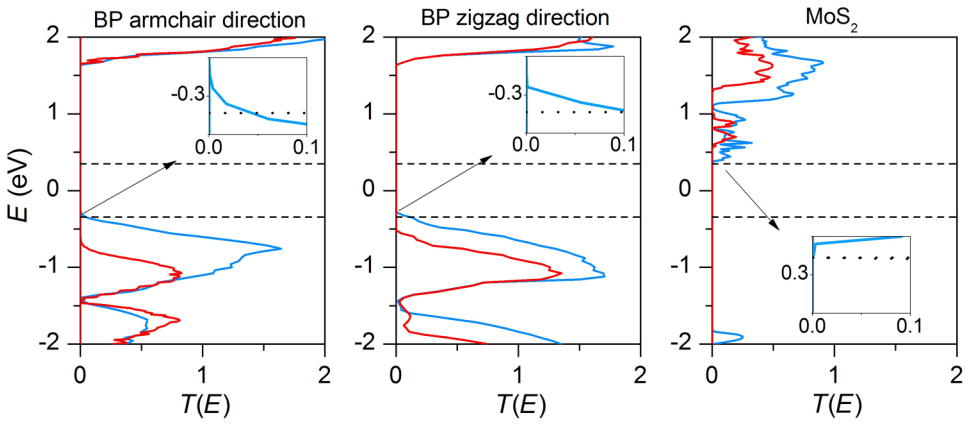

FIG. 7. Comparison of the transmission spectrum among the armchair-directed ML BP, zigzag-directed ML BP, and ML MoS_2 DG MOSFETs at $L_g = 1$ nm and UL = 4 nm. The HP OFF and ON states are colored in red and blue, respectively. The bias window of $V_b = 0.69$ V is indicated by the black dashed lines.

BP MOSFETs compared with the ML MoS_2 ones. As shown in Eq. (1), the current of the MOSFET is mainly decided by the transmission possibility $T(E)$ inside the bias window. $T(E)$ is directly proportional to the PDOS and inversely proportional to the transport effective mass of the channel material [44]. Therefore, the large PDOS and low effective mass in the armchair-directed DG ML BP MOSFETs lead to a large $T(E)$ inside the bias window and thus a high ON current (Fig. 7). With a heavy transport effective mass, the zigzag-directed DG ML BP MOSFET still shows higher $T(E)$ than the ML MoS_2 one inside the bias window, indicating the large DOS is more preferable than the small transport effective mass for achieving a large ON current in the $L_g = 1$ nm case.

E. Discussion

The traditional TFETs based on BP and related heterostructures demonstrate promising steep transfer characteristics. The fabricated BP-MoS_2 TFET shows a subthreshold swing of 65 mV/dec at room temperature with the highest current in the order of 1 μA/μm [45]. Compared with the BP-MoS_2 TFET, the sub-5-nm BP MOSFETs demonstrate smaller SS (down to 50 mV/dec) and larger current (up to 10^3 μA/μm). Even smaller SS down to 40 mV/dec in a BP-BN-BP TFET is predicted by DFT-derived analytical simulations [46]. The extremely small SS in the BP-BN-BP TFET is attributed to the strong suppression of interlayer thermal-carrier injection by the BN barrier in between the BP layers.

It is noted that the sub-5-nm DG ML BP MOSFETs are studied in the ballistic limit, neglecting the influence of electron-phonon scattering. In practical transistors, the scattering might degrade the current, especially in those with long channel length. It has been proved that if the channel length of ML BP is 10 nm, the ballisticity (defined as the current ratio between the scattering case and the ballistic limit) can exceed 88% [25,47]. Since the channel lengths ($= L_g + 2 \cdot$UL) in the studied sub-5-nm DG ML BP MOSFETs are less than 13 nm, it is reasonable to expect a similar ballisticity in these simulated devices.

Besides, our simulated BP transistors are MOSFETs, in which the source and drain are highly doped ML BP and no barrier exists between the electrode and channel regions. Due to the lack of an effective substitutional-doping approach in 2D materials, the actual BP transistors often have to be fabricated with the channel in direct contact with the bulk metal electrode [48]. In this way, Schottky barriers are often formed between BP and bulk metal electrodes and thus impede the carrier transport. Such a FET is referred to as a Schottky barrier FET (SBFET) [49], which is inferior to MOSFET.

However, by proper selection of electrode materials with a smaller or even vanishing Schottky barrier height (SBH), the device performance of the ML BP transistors could be greatly improved and approach that of the corresponding MOSFET. For example, compared with the case of Ti electrodes, the ON current in ML BP SBFET with graphene electrodes is significantly greater and reaches up to 90% of that in the MOSFET in the 5–10 nm scale [23], owing to the formation of Ohmic contact (vanishing SBH) as a result of weak Fermi-level pinning and weak electrostatic screening to the gate [50–53]. Other 2D metal electrodes such as borophene and $NbSe_2$ might also lead to a performance approaching the MOSFET limit [45,51], due to the formation of Ohmic contact. Hence, the ON-state current in an actual sub-5-nm ML BP FET with its channel length less than 10 nm and a good contact should reach about 80% [a product of the decay induced by the phonon scattering (88%) and contact (90%)] of the MOSFET ideal limit. Hence, we believe the predicted excellent device performance of the sub-5-nm ML BP FET in the ballistic limit and Ohmic contact limit is highly likely to be realized in experiment.

In the experimental 2D BP transistors, the few layer (FL) form is more popular than the ML one because it has higher stability. Compared with the ML case, FL BP can deliver more current due to the increased channel number while the gate electrostatics

is weaker simultaneously due to the increased thickness. Fortunately, the increase of the ON current in the 20-nm BP MOSFETs [24] and the degradation of SS in the 9-nm BP MOSFETs [54] are very small as the layer number decreases from 5 to 1. The sub-5-nm FL BP MOSFETs are anticipated to show as excellent performance as their ML counterparts.

Since the large band edge DOS of the channel material is the key of the high ON current of the ML BP FETs in the sub-5-nm node, other 2D semiconductors with a large band edge DOS should be paid attention. Among 2D semiconductors, hydrogenated group IV-ene (graphane and silicane) and monochalcogenides (InSe, InS, GaSe, and GaS) possess the CBM or VBM DOS that is comparable with that of BP [55]. Therefore, a high ON current may be expected in the FETs based on the above channel materials.

IV. CONCLUSIONS

From our *ab initio* quantum-transport simulations, the ON currents of the zigzag-directed DG ML BP MOSFET are apparently higher than that of its MoS_2 counterpart at an ultimate gate length of 1 nm. With proper UL configurations, the armchair-directed sub-5-nm DG ML BP MOSFETs fulfill the requirements of the ITRS for the HP devices in 2028 in terms of the ON current, delay time, and power dissipation indicator until L_g is scaled down to 2 nm. More encouragingly, the zigzag-directed sub-5-nm DG ML BP MOSFETs can even meet the ITRS goals for both the HP and LP applications in 2028 until L_g is 2 nm. We expect the predicted excellent performance of the sub-5-nm 2D BP transistors could be verified in the near future.

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