Editors' Suggestion

Phase-Tunable Thermal Logic: Computation with Heat

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Boolean algebra, the branch of mathematics in which variables can assume only true or false values, is the theoretical basis of classical computation. The analogy between Boolean operations and electronic switching circuits, highlighted by Shannon in 1938, paved the way for modern computation based on electronic devices. The growth in the computational power of such devices, after an exciting exponential—Moore's trend—is nowadays blocked by heat dissipation due to computational tasks, which are very demanding due to the miniaturization of chips. Heat is often a detrimental form of energy which increases the system's entropy, decreasing the efficiency of logic operations. Here, we propose a physical system that is able to perform thermal-logic operations by reversing the old heat-disorder epitome into a heat-order paradigm. We lay the foundations of heat computation by encoding logic state variables in temperature and introducing the thermal counterparts of electronic logic gates. Exploiting quantum effects in thermally biased Josephson junctions (JJs), we propound a possible realization of a functionally complete logic. Our architecture ensures high operational stability and robustness, with switching frequencies reaching the GHz range.

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I. INTRODUCTION

The simplicity of Boolean algebra [1] is one of the major motivations accounting for the development of classical computation during the past century. The physical realization of mathematical operations defined in a binary environment [i.e., 0 (false) and 1 (true)] requires systems to be employed where the variables can acquire only two stable values. Usually, this requirement is fulfilled through the use of electronic digital circuits implementing switching elements such as diodes and transistors [2–4]. Modern devices entrain control systems able to perform logic operations without passing through electronic interfaces or external calculus apparatus [5]. What makes a calculation scheme appealing for technological applications is the operation speed. The most popular approach is quantum computation [6], in which coherent quantum states exploit high-fidelity quantum bits (qubits) in order to implement computation algorithms [7–9]. Unfortunately, all logic architectures share one inescapable side effect: heat generation due to dissipation [10–12]. Even the most efficient computation architecture dissipates a minimum amount of heat estimated by the Landauer fundamental limit [13]. The ability to recycle part of the heat that has already been produced in a computation architecture in order to perform further logic operations pursues the goals of energy harvesting, i.e., the storage and conversion of ambient energy into autonomous new functions. On the one hand, this can be achieved by employing high-temperature phase-change materials, such as VO_2, to build hybrid thermal and/or electronic logic gates working at room temperature [14]. On the other hand, the definition of a heat logic compatible with other computation schemes could pave the way for new combined calculation architectures.

Here, we discuss the grounds of a thermal logic by constructing a functionally complete architecture [15] through the definition of thermal-logic gates. The latter employ temperature as the logic state variable, which can acquire only two digital values: cold (logic state 0) and hot (logic state 1). A thermal-logic device controls the energy flow between a reservoir and the output lead by means of a control mechanism (actuator) coupled to the input contacts. In such systems, the balance between the transmitted energy (which depends on the configuration of the input temperatures) and the power losses defines the output temperature (the output logic state). The modulation of electron heat currents in solid-state nanostructures [16,17] can be realized in the framework of coherent caloritronics [18–21]. Heat currents are mastered by manipulating the superconducting quantum phases across thermally biased Josephson junctions through the application of an external magnetic flux [22–25]. The latter can be generated by taking advantage of another quantum effect: the very efficient thermoelectric effect in temperature-biased normal-metal–ferromagnetic-insulator–superconductor (N-

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FI-S) tunnel junctions [26,27]. In this paper, we show how the marriage of these two quantum effects leads to the development of a functionally complete thermal logic. The proposed structure guarantees full complementarity with low-temperature electronic-computation systems. In particular, the N-FI-S junctions allow the thermal signals to be reconverted into electrical ones. As a consequence, the design of hybrid thermal and/or electrical systems (where areas of the circuit perform electrical computation and other thermal calculations) is possible. This could pave the way for new computation concepts and architectures.

II. COMPUTATION WITH HEAT

The three main operations of Boolean algebra [1] are negation (NOT), conjunction (AND), and disjunction (OR). All the other two-bit operations can be obtained by a composition of negation with conjunction or disjunction (NOT-AND or NOT-OR), i.e., a functionally complete logic is defined. Figure 1(a) conveys the essence of thermal logic: the distinctive shapes and the related truth tables of the negation, conjunction, and disjunction thermal-logic gates are shown. For instance, the output temperature of a NOT thermal-logic gate is 1 (hot) when the input is 0 (cold), and vice versa. The specific values of the two logic states cold and hot only depend on the technology chosen to realize the architecture.

The most generic concept of a thermal-logic gate is a device with one or more binary temperature inputs that set the binary output. Such a system consists of one or more thermal inputs that control the heat current flowing through a valve connecting a power supply to an output contact, as schematized in Fig. 1(b). The steady-state output temperature of such a general device T_C, i.e., the result of the logic operation, derives from the balance between the output and loss heat currents—the amount of heat transferred per unit of time—which in the following we denote as $\dot{Q} = dQ/dt$ (where Q is the heat and t the time). Therefore, the output temperature can be calculated by solving the following equation:

$$\dot{Q}_{\mathrm{OUT}}\left(T_A, T_B, T_P, T_C\right) - \dot{Q}_{\mathrm{loss}}\left(T_A, T_B, T_P, T_C\right) = 0, \quad (1)$$

where $\dot{Q}_{\mathrm{OUT}}$ is the heat current flowing through the thermal valve, $\dot{Q}_{\mathrm{loss}}$ includes all the heat losses of the device, T_A and T_B are the input temperatures, and T_P is the power-supply temperature (always kept at T_{hot}). Note that the source of the temperature signals (T_A, T_B, and T_P) arises from waste heat and the type of implemented logic gate (OR, AND, or NOT) is exclusively defined by the structure of the actuators.

In solid-state structures, phonons carry only heat, while electrons carry both heat and charge. Since phonons are difficult to control, up to now the advancements in phononics [28] are less groundbreaking than in electronics. Therefore, the use of phonons for thermal-logic operations [29] is challenging. On the contrary, in coherent caloritronics [18–20,22–25], electron heat currents are precisely manipulated through the control of phases in superconducting mesoscopic circuits, such as superconducting quantum-interference devices (SQUIDs) [16,17] and superconducting quantum-interference proximity transistors (SQUIPTs) [24]. In such systems (i.e., thin metal nanostructures), the vanishing Kapitza resistance [16] ensures that the phonons of every element are completely thermalized with the substrate at a constant bath temperature T_{bath}. At low temperatures (usually $T_{\mathrm{bath}} < 1$ K), the electron-phonon coupling is weak [30]. As a consequence, the electron and phonon ensembles are in thermal disequilibrium (i.e., $T_e \neq T_{\mathrm{ph}}$, where T_e and T_{ph} are the electron and phonon temperature, respectively) and the sum of the power losses due to the electron-phonon thermal gradient in each element of the device $\dot{Q}_{e\text{-ph}}$ is the principal cause of the heat losses in the system ($\dot{Q}_{\mathrm{loss}} = \sum_i \dot{Q}_{e\text{-ph},i}$).

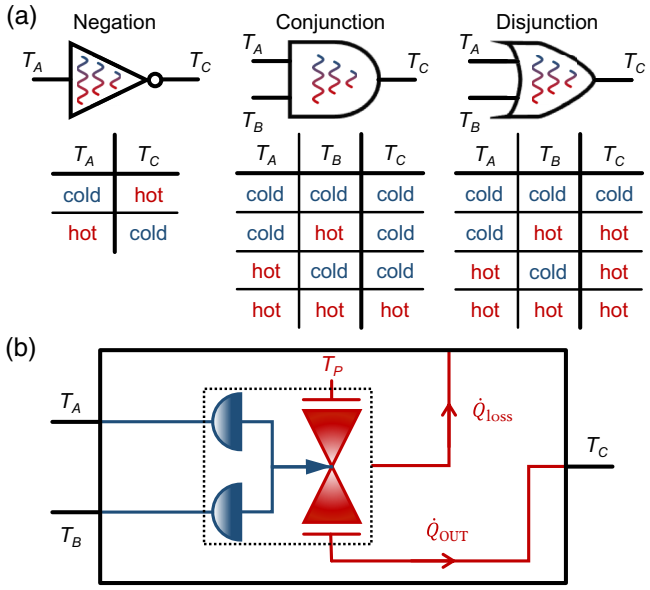

FIG. 1. Thermal-logic gates. (a) The distinctive shapes and logic truth tables of NOT, AND, and OR thermal-logic gates ("cold" is the logic state 0, while "hot" is the logic state 1) are depicted. (b) A schematic representation of a generic thermal-logic gate. The device consists of two inputs (at temperature T_A and T_B, respectively) controlling the heat flow between the power supply (at temperature T_P) and the output (at temperature T_C) through a valve (red hourglass) by means of an actuator (blue half-circumference). The output ($\dot{Q}_{\mathrm{OUT}}$) and loss ($\dot{Q}_{\mathrm{loss}}$) heat currents are shown.

III. PHASE-TUNABLE THERMAL LOGIC

An ideal logic architecture requires the input and output states to be identical variables (to allow for scalable networks) and fully decoupled (to avoid cross talk).

Both requirements are fulfilled by the recently proposed first fully thermal caloritronic device, the phase-tunable temperature amplifier (PTA) [31]. It employs a thermal nanovalve (i.e., a temperature-biased SQUIPT [24]) controlled by the magnetic flux Φ resulting from the closed-circuit current generated by a low-temperature thermoelectric element (i.e., a N-FI-S tunnel junction) [26,27,32] closed by a superconducting coil. This inductive coupling guarantees an almost infinite input-to-output impedance, making the PTA an ideal fully thermal transistor when operated at unitary gain [31].

In the following, we briefly introduce the temperature-biased SQUIPT and the N-FI-S junction, and we show how the synergy between these two building blocks can be used to implement a functionally complete thermal-logic architecture.

The SQUIPT is composed of a superconducting ring interrupted by a normal-metal wire. The latter acquires a superconducting character through the superconducting proximity effect. A normal-metal tunnel probe acting as output lead is coupled to the wire [33]. A magnetic flux Φ threading the ring modulates the density of states (DOS) of the proximized wire [34,35] and, as a consequence, the thermal conductance between the wire and the tunnel probe is periodic with the magnetic flux, with period $\Phi = \Phi_0$ [24]. In particular, the heat current is at a minimum (smaller than the power losses due to electron-phonon coupling) for $\Phi = 0$ (when the full superconducting minigap is developed in the wire DOS) and at a maximum for $\Phi = \Phi_0/2$ (when the wire shows a normal-metal DOS). A detailed description of the thermal nanovalve (SQUIPT) can be found in the Appendix.

On the other hand, a thermoelectric effect can be generated by breaking the electron-hole symmetry in the DOS of a conductor. In a superconductor, this condition can be accomplished by Zeeman spin-splitting the DOS through an exchange field and spin-filtering the quasiparticles [26]. Both of the mechanisms can be provided by a single ferromagnetic insulator layer of a N-FI-S junction. A temperature gradient between the normal metal and the superconductor produces a thermoelectric signal: an open-circuit thermovoltage V_T in the Seebeck regime or a closed-circuit thermocurrent I_T in the Peltier regime [26,27,32]. A detailed description of the thermoelectric element can be found in the Appendix.

The controlling system (actuator) is realized by shorting the thermoelectric element with a superconducting coil that inductively controls the thermal valve, as depicted in Fig. 1(b). This allows different thermal-logic gates, which use the otherwise-lost dissipated power from other (electrical) circuits to perform logic operations, to be designed. For the sake of completeness, in this proposal of a coherent caloritronic-based logic, we will theoretically demonstrate the behavior of the three basic logic gates: NOT, AND, and OR.

A. The negation logic gate—NOT

The thermal inverter logic gate NOT can, in outline, be conceived as a normally open valve, as depicted in Fig. 2(a). In this way, when $T_A = T_{\rm cold}$ (input logic state 0), a thermal current flows through the valve and the output temperature is $T_C = T_{\rm hot}$ (output logic state 1). The energization of the actuator interrupts the flow of the heat current from the power supply to the output lead and, as a consequence, the output temperature T_C is lowered to $T_C = T_{\rm cold} = T_{\rm bath}$ (output logic state 0). This can be realized by controlling a temperature-biased SQUIPT (thermal valve) through two N-FI-S junctions shorted by two coils: one connected to the input T_A while the other is always kept at $T_{\rm hot}$ [see Fig. 2(b)]. The total magnetic flux threading the superconducting ring $\Phi_{\rm NOT}(T_A)$ is the sum of the contributions due to the opening Φ_O and the input Φ_A coil, and takes the following form:

$$\begin{aligned}\Phi_{\rm NOT}(T_A) &= \Phi_O(T_{\rm hot}) + \Phi_A(T_A)\\ &= M_O I_{T,O}(T_{\rm hot}) + M_A I_{T,A}(T_A),\end{aligned} \tag{2}$$

where M_i (with $i = O, A$) is the mutual inductance between the superconducting ring and the opening L_O or input coil L_A, and $I_{T,i}$ is the thermocurrent generated by the opening or input thermoelectric element. The mutual inductance M_i is chosen in order to have maximum conduction through the valve when $T_i = T_{\rm hot}$, i.e., $\Phi_i(T_{\rm hot}) = \Phi_0/2$ (with $i = O, A$). In summary, the behavior of the not thermal-logic gate is expressed by the following system:

$$\Phi_{\rm NOT}(T_A) = \begin{cases} \frac{\Phi_0}{2} + 0, & \text{if } T_A = T_{\rm cold} \implies T_C = T_{\rm hot},\\ \frac{\Phi_0}{2} + \frac{\Phi_0}{2}, & \text{if } T_A = T_{\rm hot} \implies T_C = T_{\rm cold}. \end{cases} \tag{3}$$

The opening coil L_O provides a constant contribution $\Phi_0/2$ to the flux. As consequence, when $T_A = T_{\rm cold}$, the input coil does not give any contribution to the total flux and the SQUIPT conducts ($T_C = T_{\rm hot}$), while for $T_A = T_{\rm hot}$ the total flux is $\Phi_{\rm NOT} = \Phi_0$ and the heat current through the valve is almost completely suppressed ($T_C = T_{\rm cold}$).

In order to demonstrate the feasibility of our architecture, we employ a Cu-EuS-Al tunnel junction [32] as the thermoelectric element and an Al-based SQUIPT with a Cu output electrode as the thermal nanovalve [24,33]. Further details on the materials and geometry can be found elsewhere [31]. In our setting, we define as logic state 0 the temperatures ranging from 100 to 105 mK (with optimum value $T_{\rm cold} = 100$ mK) and as logic state 1 the temperatures in the range 120–150 mK (with optimum value $T_{\rm hot} = 150$ mK). These temperature values depend on the employed materials and are chosen to ensure good separation between logic states 0 and 1, and to place the thermoelectric element in the best-performance window.

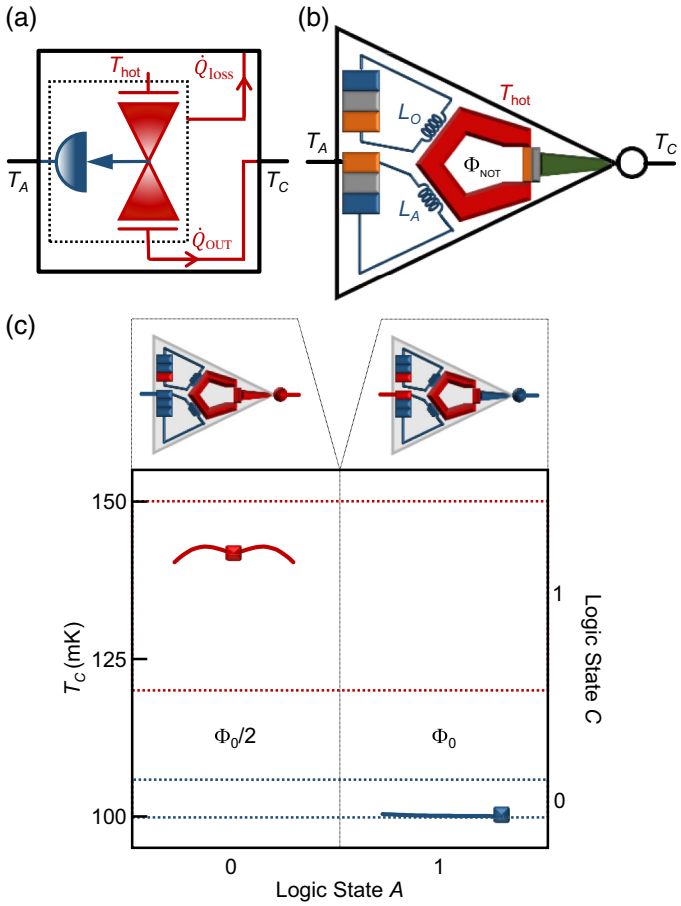

FIG. 2. The NOT logic gate. (a) A thermal schematic: an actuator (blue half-circumference) at input temperature T_A controls, through an normally open valve (red hourglass), the heat flow from the power supply (at temperature T_{hot}) to the output (at temperature T_C). The output ($\dot{Q}_{OUT}$) and loss ($\dot{Q}_{loss}$) thermal currents are shown. (b) A schematic of the coherent caloritronic realization: the thermoelectric elements are constituted of a metal (orange), a ferromagnetic insulator (gray), and a superconductor (blue). The blue spirals depict the superconducting coils L_A and L_O. The SQUIPT is composed of a superconductor ring, kept at temperature T_{hot} (red), interrupted by a metal wire (orange) tunnel-coupled to a metal probe (green) through a thin insulator (gray). (c) The output temperature T_C and output logic state C versus the logic input configuration for $T_{cold} = T_{bath} = 100$ mK and $T_{hot} = 150$ mK. The output temperature T_C for optimum (squares) and fluctuating (lines) input is shown.

The output characteristic of the thermal inverter is shown in Fig. 2(c). For an ideal logic input 0 ($T_A = 100$ mK), the output temperature is $T_C = 142$ mK, while for logic input 1 ($T_A = 150$ mK), the output becomes $T_C = 100$ mK. In order to evaluate the operational stability with oscillations of the input signal, we impose fluctuations on the order of 10% around the optimum T_A, evaluate the changes in the magnetic flux controlling the SQUIPT, and, as a consequence, calculate the resulting variations in the output temperature T_C. The resulting curves [depicted as continuous lines in Fig. 2(c)] show a good thermal stability of the proposed architecture.

B. The conjunction logic gate—AND

The thermal conjunction logic gate AND can be represented as a valve which is always closed, except when both actuators are energized ($T_C = T_{hot}$ only if $T_A = T_B = T_{hot}$), as depicted in Fig. 3(a). In the coherent caloritronic realization, the heat flow across a temperature-biased SQUIPT is modulated by means of the total magnetic flux $\Phi_{AND}(T_A, T_B)$ generated by the coils L_A and L_B shorting two thermoelectric elements (input leads) at temperatures T_A and T_B. The total magnetic flux threading the superconducting ring is the sum of the contribution due to the two inputs (Φ_A and Φ_B) and is given by

$$\begin{aligned}\Phi_{AND}(T_A, T_B) &= \Phi_A(T_A) + \Phi_B(T_B) \\ &= M_A I_{T,A}(T_A) + M_B I_{T,B}(T_B),\end{aligned} \tag{4}$$

where M_i (with $i = A, B$) is the mutual inductance between the superconducting ring and the input coils L_i, and $I_{T,i}$ is the thermocurrent generated by the input thermoelectric elements. Both mutual inductances M_i are chosen in order to have $\Phi_i(T_{hot}) = \Phi_0/4$ (with $i = A, B$). As a consequence, the behavior of the and thermal-logic gate can be summarized by the following system:

$$\Phi_{AND}(T_A, T_B) = \begin{cases} 0 + 0, & \text{if } T_A = T_{cold},\ T_B = T_{cold} \\ & \implies T_C = T_{cold}, \\ 0 + \dfrac{\Phi_0}{4}, & \text{if } T_A = T_{cold},\ T_B = T_{hot} \\ & \implies T_C = T_{cold}, \\ \dfrac{\Phi_0}{4} + 0, & \text{if } T_A = T_{hot},\ T_B = T_{cold} \\ & \implies T_C = T_{cold}, \\ \dfrac{\Phi_0}{4} + \dfrac{\Phi_0}{4}, & \text{if } T_A = T_{hot},\ T_B = T_{hot} \\ & \implies T_C = T_{hot}. \end{cases} \tag{5}$$

When $T_A = T_B = T_{cold}$ [input logic state $(A, B) = (0, 0)$], the input coils do not generate any magnetic flux ($\Phi_{AND} = 0$); thereby, the thermal conductance of the SQUIPT is almost zero ($T_C = T_{cold}$) (output logic state 0). If a single actuator is active, i.e., $T_A = T_{hot}$ or $T_B = T_{hot}$ with the other input at T_{cold}, the total magnetic flux driving the SQUIPT is $\Phi_{AND} = \Phi_0/4$. Therefore, the nanovalve is still almost completely closed [24,31] and $T_C = T_{cold}$ (output logic state 0). For $T_A = T_B = T_{hot}$, the total magnetic flux is $\Phi_{AND} = \Phi_0/2$ and the SQUIPT conducts fully. As a consequence, the output logic state is 1 ($T_C = T_{hot}$).

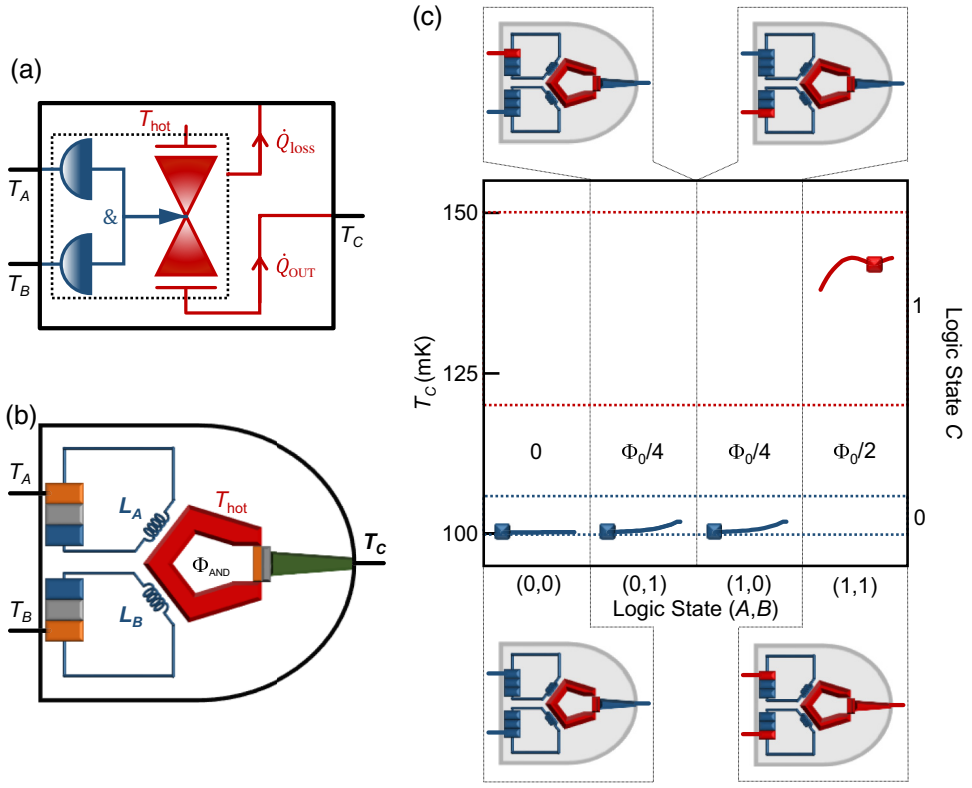

FIG. 3. The AND logic gate. (a) A thermal schematic: two actuators (blue half-circumferences) at input temperature T_A and T_B control, through a valve (red hourglass), the heat flow between the power supply (at temperature T_{hot}) and the output (at temperature T_C). The output ($\dot{Q}_{OUT}$) and loss ($\dot{Q}_{loss}$) thermal currents are shown. (b) A schematic of the coherent caloritronic realization: the thermoelectric elements are constituted of a metal (orange), a ferromagnetic insulator (gray), and a superconductor (blue). The blue spirals depict the superconducting coils L_A and L_B. The SQUIPT is composed of a superconductor ring, kept at temperature T_{hot} (red), interrupted by a metal wire (orange) tunnel-coupled to a metal probe (green) through a thin insulator (gray). (c) The output temperature T_C and output logic state C versus the logic input configuration for $T_{cold} = T_{bath} = 100$ mK and $T_{hot} = 150$ mK. The output temperature T_C for optimum (squares) and fluctuating (lines) input is shown.

For a numerical demonstration of the behavior of the thermal conjunction, we employ the same materials and geometry as used for the NOT gate [31]. Figure 3(c) illustrates the transfer characteristic of the AND logic gate. In the case of a partially conducting SQUIPT [i.e., for $(A,B) = (1,0)$ or $(A,B) = (0,1)$], a small heat current flows from the power supply to the output electrode and the value of T_C is slightly larger than for $(A,B) = (0,0)$. In all cases, the output temperature resides within the range of logic state 0 (100–105 mK), because the electron-phonon coupling is large enough to partially compensate the effect of the heat current reaching the output (see the Appendix).

C. The disjunction logic gate—OR

The working principle of the thermal disjunction logic gate or is summarized in Fig. 4(a), where the parallel connection of two normally closed valves ($T_C = T_{cold}$ when $T_A = T_B = T_{cold}$) allows the heat flow from the power supply at temperature $T_P = T_{hot}$ to a common output electrode. The heating of at least one actuator ($T_A = T_{hot}$ and/or $T_B = T_{hot}$) opens a conduction channel to the output ($T_C = T_{hot}$). A possible practical realization is constituted of two SQUIPTs sharing the same output electrode, as schematized in Fig. 4(b). Each thermal nanovalve is controlled by the magnetic flux (Φ_A or Φ_B) generated by a thermoelectric element connected to the input electrode (at temperature T_A or T_B). The magnetic flux Φ_{OR} effectively controlling the or logic gate can be defined as follows:

$$\begin{aligned}\Phi_{OR}(T_A,T_B) &= \Phi_A(T_A) \vee \Phi_B(T_B)\\ &= M_A I_{T,A}(T_A) \vee M_B I_{T,B}(T_B),\end{aligned} \tag{6}$$

where M_i (with $i = A,B$) is the mutual inductance between the superconducting ring and the input coil L_i, and $I_{T,i}$ are the thermocurrents generated by the input thermoelectric elements. The mutual inductance M_i is chosen in order to have $\Phi_i(T_{hot}) = \Phi_0/2$ (with $i = A,B$). To summarize, the OR thermal-logic gate works as follows:

$$\Phi_{OR}(T_A,T_B) = \begin{cases} 0 \vee 0, & \text{if } T_A = T_{cold},\ T_B = T_{cold} \\ & \implies T_C = T_{cold}, \\ 0 \vee \frac{\Phi_0}{2}, & \text{if } T_A = T_{cold},\ T_B = T_{hot} \\ & \implies T_C = T_{hot}, \\ \frac{\Phi_0}{2} \vee 0, & \text{if } T_A = T_{hot},\ T_B = T_{cold} \\ & \implies T_C = T_{hot}, \\ \frac{\Phi_0}{2} \vee \frac{\Phi_0}{2}, & \text{if } T_A = T_{hot},\ T_B = T_{hot} \\ & \implies T_C = T_{hot}. \end{cases} \tag{7}$$

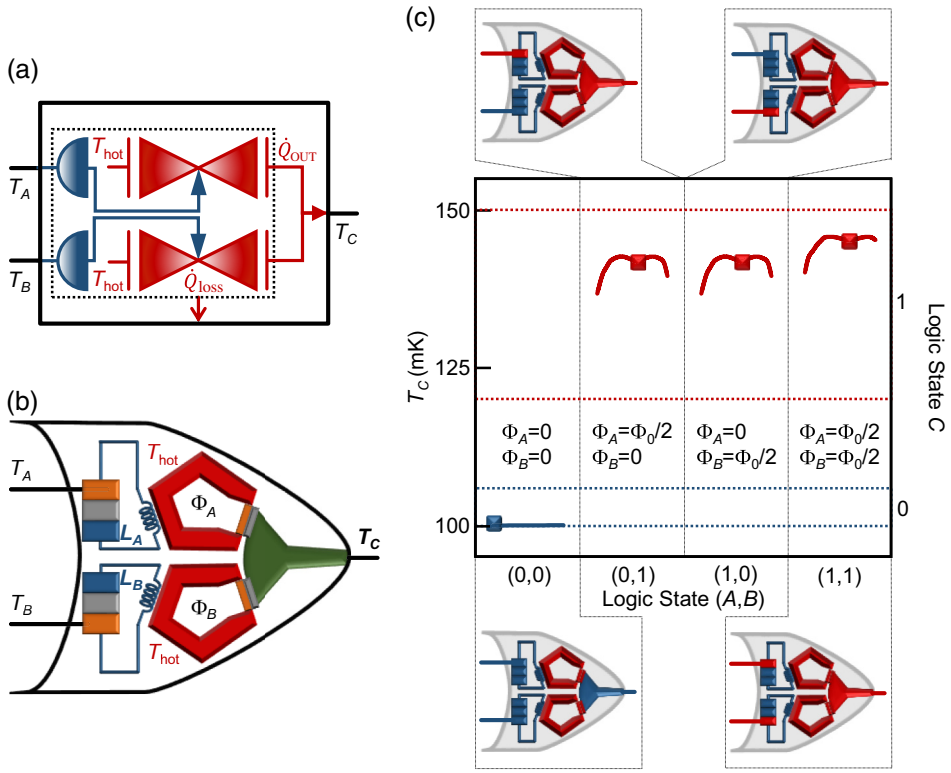

FIG. 4. The OR logic gate. (a) A thermal schematic: two actuators (blue half-circumferences) at input temperature T_A and T_B control, through two valves (red hourglasses), the heat flow from the power supply (at temperature T_{hot}) to the output (at temperature T_C). The output ($\dot{Q}_{OUT}$) and loss ($\dot{Q}_{loss}$) thermal currents are shown. (b) A schematic of the coherent caloritronic realization: the thermoelectric elements are constituted of a metal (orange), a ferromagnetic insulator (gray), and a superconductor (blue). The blue spirals depict the superconducting coils L_A and L_B. The SQUIPTs are composed of a superconductor ring, kept at temperature T_{hot}(red), interrupted by a metal wire (orange) tunnel-coupled to a metal probe (green) through a thin insulator (gray). (c) The output temperature T_C and output logic state C versus the logic input configuration for $T_{cold} = T_{bath} = 100$ mK and $T_{hot} = 150$ mK. The output temperature T_C for optimum (squares) and fluctuating (lines) input is shown.

For $T_A = T_B = T_{cold}$ [input logic state $(A, B) = (0, 0)$], neither of the input coils generate any magnetic flux ($\Phi_{OR} = 0$); therefore, both SQUIPTs are shut ($T_C = T_{cold}$) and the output logic state is 0. When at least one actuator is active, i.e., $T_A = T_{hot}$ or $T_B = T_{hot}$, there is heat flowing to the output electrode and $T_C = T_{hot}$ (output logic state 1).

The behavior of the thermal disjunction is numerically evaluated by employing the same materials and geometry as used for negation and conjunction gates [31]. The transfer characteristic of the or logic gate is summarized in Fig. 4(c). When only one actuator is energized [i.e., for $(A, B) = (1, 0)$ or $(A, B) = (0, 1)$], only the heat current flowing through one valve reaches the output electrode and the optimal output temperature is $T_C = 142$ mK (for further details, see the Appendix). In the case of $(A, B) = (1, 1)$, the thermal currents flowing through both SQUIPTs arrive at the output; as a consequence, the output temperature is higher than in the previous cases ($T_C = 145$ mK).

IV. THE OPERATING TEMPERATURE, SPEED, FAN-OUT, AND COMPATIBILITY

Temperature is the fundamental working parameter for phase-tunable thermal logic, because the grounding physical mechanisms of coherent caloritronics, such as electron-phonon coupling and the superconducting pairing potential, strongly depend on both phonon and electron temperatures. For example, the working speed of such logic gates is limited by the thermalization of the electrons with the lattice phonons, because typically the characteristic time constant of the inductive coupling is much shorter. Therefore, at a first approximation, the logic working speed depends on the threshold temperature $T_{cold} = T_{bath}$ [30]. In the limit of clean metals (employed as output electrodes in our architecture) the electron-phonon relaxation time is given by [30]:

$$\tau_{e\text{-ph}} = \frac{k_B^2 v_F}{0.34 \Sigma T_{bath}^3}, \tag{8}$$

where k_B is the Boltzmann constant, v_F is the Fermi velocity, and Σ is the electron-phonon coupling constant of the metal output lead. Therefore, the maximum operating frequency ($f = 1/\tau_{e\text{-ph}}$) is limited by the phonon temperature, as depicted in Fig. 5(a). For $T_{cold} = 100$ mK (which has been used up to now), the operating frequency f is limited to about 100 KHz. By employing superconductors with a higher critical temperature, such as vanadium ($T_V = 5.38$ K) and niobium ($T_{Nb} = 9.3$ K), the operating temperature can be increased, and f reaches values on the order of a few GHz.

Although we are demonstrating a thermal-logic architecture working at temperatures higher than 1 K [see

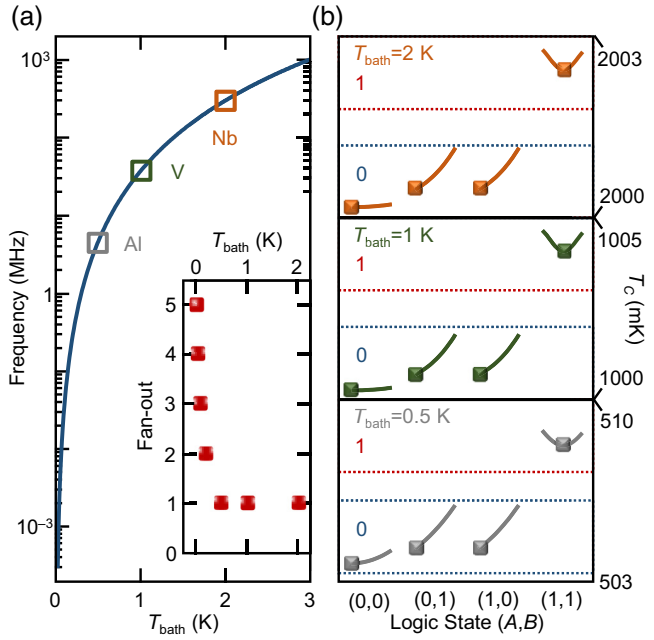

FIG. 5. The temperature dependence of the logic architecture. (a) The maximum operating frequency as a function of the bath temperature T_{bath}. Inset: the FAN-OUT as a function of the phonon temperature T_{bath}. (b) The output temperature T_C versus the input configuration (A, B) of an AND logic gate for $T_{bath} = 0.5, 1, 2$ K. The output signals for optimum (squares) and fluctuating (lines) inputs are shown.

Fig. 5(b)], for logic state 1 the output temperature is drastically suppressed compared to T_{hot}, and the separation between T_{cold} and T_{hot} turns out to be very small (a few mK). We introduce the FAN-OUT, namely the number of series logic gates that are working properly without the necessity of signal amplification. The inset of Fig. 5(a) shows the FAN-OUT of a negation logic gate as a function of the operating temperature. It is calculated by assuming that the output electrode of one device coincides with the input lead of the next one, and then by using the output heat $\dot{Q}_{OUT}$ of a device (in logic state 1) as the input signal for the next logic gate, until T_C resides in the correct temperature range. At high temperature, every logic gate requires an amplification of the output signal; therefore, the temperature amplifier [31] becomes an integral part of the device. On the contrary, at low temperatures the FAN-OUT increases. For example, in the case of $T_{cold} = 100$ mK, it is possible, in principle, to connect three devices before amplification.

Here, we demonstrate the proof of principle of a phase-tunable thermal logic by employing the simplest and most common geometry in hybrid nanostructures. However, the performance of our architecture (speed and FAN-OUT) can be drastically improved by using only superconducting materials, because the thermal losses due electron-phonon coupling decrease drastically [30]. For instance, fully superconducting thermal memories working up to about 10 K at frequencies up to tens of GHz have been proposed [36]. In order to speed up our system and increase the FAN-OUT, thermoelectric elements based on S-FI-S' tunnel junctions (with $\Delta_S > \Delta_{S'}$) [37] and a fully superconducting temperature-biased SQUIPTs [24] could be employed.

Finally, we would like to highlight that phase-tunable thermal logic could be used in synergy with other approaches to computation. It can utilize the unavoidable heat generated by dissipation in other logic architectures in order to increase the total calculating capacity and to decrease the energy consumption. For instance, the materials employed and the geometry are fully compatible with standard low-temperature semiconductor-based technologies and quantum-computation architectures. Therefore, phase-tunable thermal logic could represent a fertile field for the growth of new and more efficient combined computation systems.

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APPENDIX A: THE THERMAL VALVE—THE SQUIPT

The electronic thermal currents flowing from a power supply to an output electrode through a tunnel barrier are given by [30]:

$$\dot{Q}_{OUT}(T_P, T_C) = \frac{2}{e^2 R_T}\int_0^\infty N_P(E)N_C(E)[f_0(E,T_P) - f_0(E,T_C)]EdE, \quad \text{(A1)}$$

where $T_{P/C}$ is the temperature of the power supply or the output lead, e is the electron charge, R_T is the normal-state tunnel resistance, $N_{P/C}$ is the reduced DOS for the power supply or the output lead, and $f_0(E,T) = [1 + \exp(E/k_BT)]^{-1}$ is the Fermi distribution of the quasiparticles.

The thermal valve is a device which controls the flow of a heat current by opening and closing a passageway. The thermal current is modulated by tuning the DOS of (at least) one of the two electrodes [24]. For simplicity, in the following we assume an output electrode made of

a normal metal with $N_C(E) = 1$ and we tune the DOS of the power-supply electrode $N_P(E)$. This can be realized by placing a normal-metal wire (P) in good electrical contact with a superconducting ring (S). The superconducting properties acquired by the wire through the proximity effect [38] can be modulated by a magnetic flux Φ threading the superconducting loop [33–35,39]. The DOS of the wire $N_P = |\Re[g^R]|$ is the real part of the retarded Green's function g^R [40] obtained by solving the one-dimensional Usadel equation [41]. In the limit of a short junction (i.e., when $E_{\rm Th} = \hbar D/l^2 \gg \Delta_{0_S}$, where $E_{\rm Th}$ is the Thouless energy, $\hbar$ is the reduced Planck constant, D is the wire diffusion coefficient, l is the length of the wire, and Δ_{0_S} is the zero-temperature superconducting energy gap of the ring), the proximity effect is maximized, and the DOS can be explicitly written as [24,33]:

$$N_P(E,\Phi) = \left|\Re\left[\frac{E - iE_{\rm Th}\gamma g_s}{\sqrt{(E - iE_{\rm Th}\gamma g_s)^2 + \left[E_{\rm Th}\gamma f_s \cos\left(\frac{\pi\Phi}{\Phi_0}\right)\right]^2}}\right]\right|. \tag{A2}$$

Above, $\gamma = R_P/R_{\rm int}$ is the transmissivity of the clean contact between the superconducting ring (S) and the proximized normal metal wire (P) ($S-P$ contact, where R_P is the resistance of the metal wire and $R_{\rm int}$ the resistance of the $S-P$ interface), $g_S(E) = (E + i\Gamma_S)/\sqrt{(E + i\Gamma_S)^2 - \Delta_S^2}$ and $f_S(E) = \Delta_S/\sqrt{(E + i\Gamma_S)^2 - \Delta_S^2}$ are the coefficients of the phase-independent and phase-dependent parts of the proximized DOS (where Γ_S is the Dynes broadening parameter [42] and Δ_S is the Bardeen-Cooper-Schrieffer (BCS) energy gap [43]), and $\Phi_0 \simeq 2.0678 \times 10^{-15}$ Wb is the magnetic flux quantum. The periodic behavior of $N_C(E,\Phi)$ in the magnetic flux (with periodicity $\Phi = \Phi_0$) results in a heat current $\dot{Q}_{\rm OUT}(T_P, T_C)$ with the same periodic dependence on Φ.

In the quasiequilibrium limit, for a given supply temperature T_P, the steady-state temperature of the output electrode T_C is obtained by solving the following energy-balance equation:

$$-\dot{Q}_{\rm OUT}(T_P, T_C, \Phi) + \dot{Q}_{e\text{-ph},C}(T_C, T_{\rm bath}) = 0. \tag{A3}$$

The electron-phonon coupling takes the form $\dot{Q}_{{\rm loss},C} = \dot{Q}_{e\text{-ph},C}(T_C, T_{\rm bath}) = \Sigma V(T_C^n - T_{\rm bath}^n)$, where Σ is the electron-phonon coupling constant, V is the volume of the output electrode, and the exponent n depends on the disorder of the system [30]. For metals, in the clean limit $n = 5$, while in the dirty limit $n = 4, 6$ [21,24,30]. From Eq. (A3), it follows that the temperature on the right side of the tunnel junction, T_C, inherits the same dependence on Φ of N_C and $\dot{Q}_{\rm OUT}$ (i.e., T_C shows a minimum for $\Phi = 0$ and a maximum around $\Phi = \Phi_0/2$).

APPENDIX B: THE ACTUATION SYSTEM

Since the nanovalve (SQUIPT) is controlled by a magnetic flux, a temperature-to-flux conversion mechanism is necessary in the actuation system. This is realized by a thermoelectric element shorted by a superconducting coil.

The electron-hole asymmetry in the quasiparticle DOS is the key ingredient for thermoelectricity [44]. In superconductors, it can be accomplished by spin-splitting the DOS through an exchange field $h_{\rm ex}$ and by selecting a specific spin species through the coupling of the superconductor to a spin-polarized element [26]. Both requirements are satisfied by a normal-metal–ferromagnetic-insulator–superconductor (N-FI-S) junction, where the ferromagnetic element produces both the exchange field $h_{\rm ex}$ and the polarization $P = (G_\uparrow - G_\downarrow)/(G_\uparrow + G_\downarrow)$ [where $G_\uparrow$ and $G_\downarrow$ are the spin-up and spin-down conductances] [45,46]. For a superconductor thinner than the coherence length ξ_0, the spin-splitted DOS can be assumed to be spatially homogeneous [47] and is written as follows [48]:

$$N_{\uparrow,\downarrow}(E) = \frac{1}{2}\left|\Re\left[\frac{E + i\Gamma \pm h_{\rm ex}}{\sqrt{(E + i\Gamma \pm h_{\rm ex})^2 - \Delta^2}}\right]\right|, \tag{B1}$$

where E is the energy, Γ is the Dynes broadening parameter, and $\Delta(T, h_{\rm ex})$ is the superconducting order parameter, which is calculated self-consistently from the BCS equation [48]:

$$\ln\left(\frac{\Delta_0}{\Delta}\right) = \int_0^{\hbar\omega_D} \frac{f_+(E,T) + f_-(E,T)}{\sqrt{E^2 + \Delta^2}} dE. \tag{B2}$$

Above, Δ_0 is the zero-temperature superconducting gap, ω_D is the Debye frequency of the superconductor, and $f_\pm(E,T) = \{1 + \exp[(\sqrt{E^2 + \Delta^2} \mp h_{\rm ex})/k_BT]\}^{-1}$ is the Fermi distribution of the spin-polarized electrons.

The thermocurrent originated by keeping N (where N is the normal metal of the *N-FI-S* tunnel junction) at a temperature T_A and the other two elements (*FI* and *S*) at the bath temperature $T_{\rm bath}$ takes the following form:

$$I_T(T_A, T_{\rm bath}) = \frac{1}{eR_T}\int_{-\infty}^{\infty} [N_+(E) + PN_-(E)] \times [f_N(E, T_A) - f_S(E, T_{\rm bath})]\, dE, \tag{B3}$$

where R_T is the tunnel resistance in the normal state, $N_\pm(E) = N_\uparrow(E) \pm N_\downarrow(E)$, and $f_{N,S}(E, T_{A,{\rm bath}}) = [1 + \exp(E/k_BT_{A,{\rm bath}})]^{-1}$ is the Fermi distribution of the

metal or the superconductor. The resulting magnetic flux which threads the superconducting ring is

$$\Phi(T_A, T_{\text{bath}}) = MI_T(T_A, T_{\text{bath}}) = k\sqrt{L_A L_S} I_T(T_A, T_{\text{bath}}), \tag{B4}$$

where M is the mutual inductance, $k \leq 1$ is the coupling coefficient, L_A is the inductance of the coil shorting the N-FI-S junction, and L_S is the geometric inductance of the superconducting ring.

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