# Development of solid-state amplifier for accelerator project based on the concept of standardization

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Institute of Modern Physics (IMP), Chinese Academy of Sciences, is the first domestic institute that widely applied solid-state power amplifier (SSPA) to linear accelerator project from the C-ADS project started since 2011. Until now, the same design has already been considered for two large-scale scientific facilities in Guangdong Province of southeast China, China initiative Accelerator Driven System and High Intensity Heavy-ion Accelerator Facility. In a recent decade of accelerator project construction, a large amount of valuable experience in solid-state power source design build and operation was accumulated with the operation and upgrade of several projects. Furthermore, following the successful development of the IMP SSPA, a new "standardization" design concept was put forward after many modifications and improvements, which means all designs meet the stringent system requirements: high performance, low cost, high scalability, high reliability, and ease of maintenance need. The new design and technology can be developed for this accelerator solution, such as the high-performance power amplifier, "hot swap" technology, and special combiners, which are all new methods for long-term stable operation and maintenance on-site, especially the processing failure without rf power interrupting. This paper will detail the development of "standardization" design and its technical characteristics.

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## I. INTRODUCTION

The past few years have seen considerable progress in the performance of semiconductors for high-power cw applications [1]. With the advancement of laterally diffused MOS (LDMOS) technology, the power output of solid-state rf devices has been pushed up to 1000 or even 2000 cw watts at proton or heavy ion accelerator, which is shown in Fig. 1. Although quite innovative and challenging for the required power range, this technology is very attractive and presents significant advantages as compared to the more conventional vacuum tubes, klystron, or tetrodes. The rf system in two accelerator projects at the Institute of Modern Physics (IMP) has been successfully commissioned, and the operational experience is quite satisfactory.

Solid-state power amplifier (SSPA) solution presents significant advantages as compared to the vacuum tubes [2]: (i) High modularity with associated redundancy and flexibility, (ii) elimination of the high voltage handling and the high-power circulator, (iii) simpler start-up procedures and operation control, (iv) no need for periodical replacement, (v) lower operational cost and easier maintenance, and (vi) lower investment cost with a profit of the existing in-house expertise.

So, a solid-state amplifier is very suitable for constructing the accelerator project, especially for large-scaling


FIG. 1. Linear power improvement of the SSPA in a recent decade at IMP.

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linear accelerator projects, due to its low voltage, modularity, the advantages of parallel operation, and robust maintainability. Furthermore, core components such as power amplifier modules and dc supply modules are fixed designs for interchange between the different manufacturers. Most importantly, the new design can meet the requirements of "hot swap," which means any failed module could be replaced immediately even during the time of beam or full reflection operation.

The critical features of SSPAs for accelerator application in IMP are solid-state class AB linear design, suitable for both cw and pulse operation modes, 50-Ω input or output impedance, high reliability and ruggedness, LDMOS technology, water-cooled, high efficiency, and full-performance operation at any load condition (from perfect match to infinite mismatch) [3]. Since the first SSPA was used in the accelerator in 2012, we have gradually gained valuable experiences. Four main problems are greatly improved, namely, the development of a liquid cooling mode based on high power density, the layout of dc power supply, the higher performance of the power amplifier, and the special power combiner.

The development at three frequencies of 24-kW prototypes was launched to validate the performance in the design of standardization, including the 1.2-kW amplifier module at the low- and middle-frequency range and compact combiner scheme. The successful results help us decide to apply this design idea to the current project China initiative Accelerator Driven System (CiADS) and High Intensity Heavy-ion Accelerator Facility (HIAF). The 81.25, 325, and 650 MHz SSPAs are presently under fabrication, and they should be completed in the middle of 2023 for the project construction. The prototypes at all frequencies were completed in 2022. According to the standardization design, the PA module with BLF189XRA at 162.5 MHz has the highest efficiency of 72%, where the efficiency is defined as the ratio of output rf power to dc power. The output power at the 1-dB gain compression point is 1230 W. Similar performance was demonstrated with this MOSFET measured at 325 MHz.

The 650-MHz PA modules were made with two BLF978P transistors due to their small circulators and wavelength. At the −1-dB gain compression point, an output power of 1.915 kW with an efficiency of 63.44% was achieved and more than 2 kW was achieved at saturation with $V_{DS}$ at 50 V. One rack with 32 modules has been completed. The maximum power of the rack exceeded 60 kW, which was higher than initially estimated due to the implementation of specific thermal solutions for the modules. Additionally, the rack demonstrated a drain efficiency of 54.1% and a power output of 57.36 kW, indicating a highly satisfactory performance. Furthermore, the newest PA module prototype from third semiconductor materials has been measured for scientific research, which was estimated to have a 40% increase in power escalation and a 12% increase in efficiency. The detailed information will not be described.

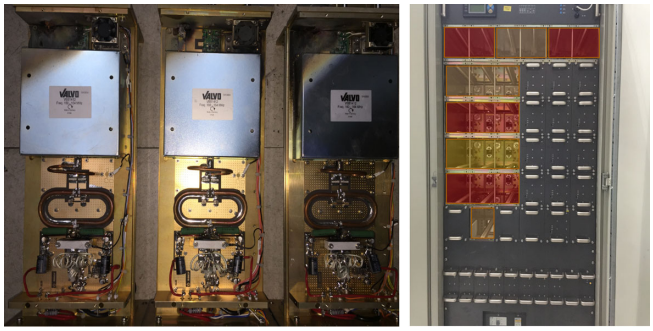

FIG. 2. A serious accident raises a critical problem—port isolation.

## II. STANDARDIZATION DESCRIPTION

In the context of large-scale accelerator projects, the presence of various types of SSPA from different manufacturers can pose challenges in terms of replacement and backup. The availability of an improved design in terms of module size, interfaces, protocols, and performance for interchange purposes could significantly improve the product's appeal in terms of maintenance and cost. The implementation of standardization design is primarily motivated by this objective.

On the other hand, one potential risk associated with SSPAs in the long-term run is the danger posed by the isolation of the power combiner. For instance, in 2018, a serious accident occurred in which a total of 19 modules failed, including burned circulators or transistors, all concentrated on one side as shown in Fig. 2. This phenomenon piqued our interest and ultimately led to the development of a mature isolation theory—hot swap—at IMP, which is the second reason for standardization.

Finally, during the development of standardization, the performance and specific requirements of accelerator construction were gradually improved.

## III. STANDARDIZATION DESIGN

Despite the modular design of SSPAs, mechanical design became a complex technological challenge due to the high power density and the need for interchangeability. Interchangeability refers to the use of a standardized design for PA and dc power supply modules to reduce costs and simplify maintenance. However, achieving this goal proved difficult. Unifying physical dimensions presented significant challenges in coordinating tolerance and multicontact surfaces within a plug-pull structure. Additionally, control logic and protocols varied among manufacturers, requiring each to abandon their previous designs to comply with standardization. Performance differences also resulted in losses of synthesis efficiency, placing high demands on the PA module. Nevertheless, our research at IMP made significant progress in these areas. The first prototype SSPA was completed in 2021, and its structure and performance closely matched the original design. Communication

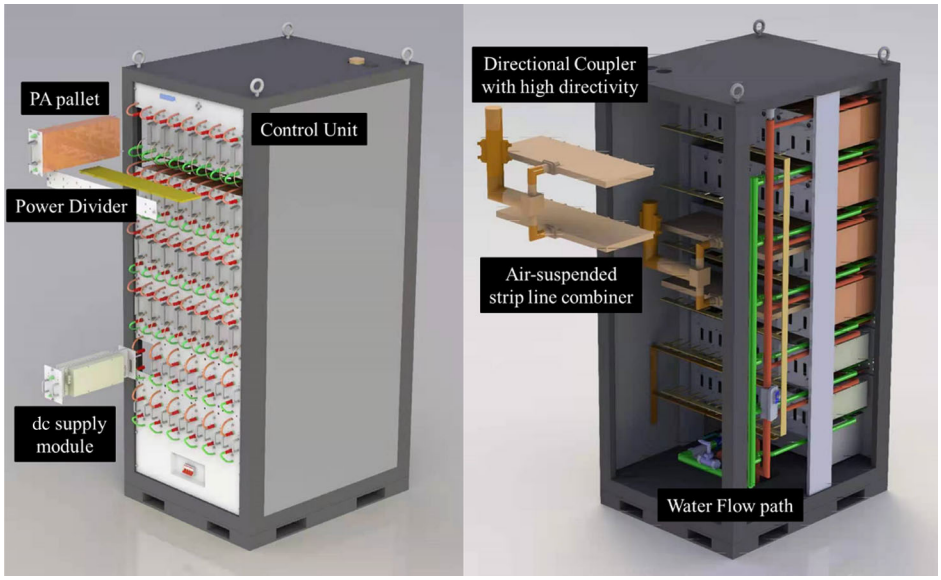


FIG. 3. The structure diagram of solid-state power source.

between different modules became a new research direction to enable monitoring and interlock.

Research has been conducted to enhance performance, including experiments on LDMOS modules with high power density and increased efficiency, specialized power combiners, and dc supply modules.

Hot-swap technology, a critical advancement, was first introduced for SSPA in the CiADS and HIAF projects. The availability requirement for SSPA is ≥0.999, which could not be met by the current system. Hot-swap technology allows for the replacement of faulty modules while the solid-state power source is operating normally or even during full reflection. This significantly improves the availability of solid-state power sources for CiADS projects.

### A. Structure design

The SSPA rack, designed according to standardization principles, primarily comprises power amplifier modules, combiners, distributors, dc power supplies, and cooling components, as shown in Figs. 3 and 4.

To facilitate the convenient upgrade of output power for different cavities, the overall design of the SSPA rack considered the need for hot swapping of PA modules and dc supply components. This required careful consideration of

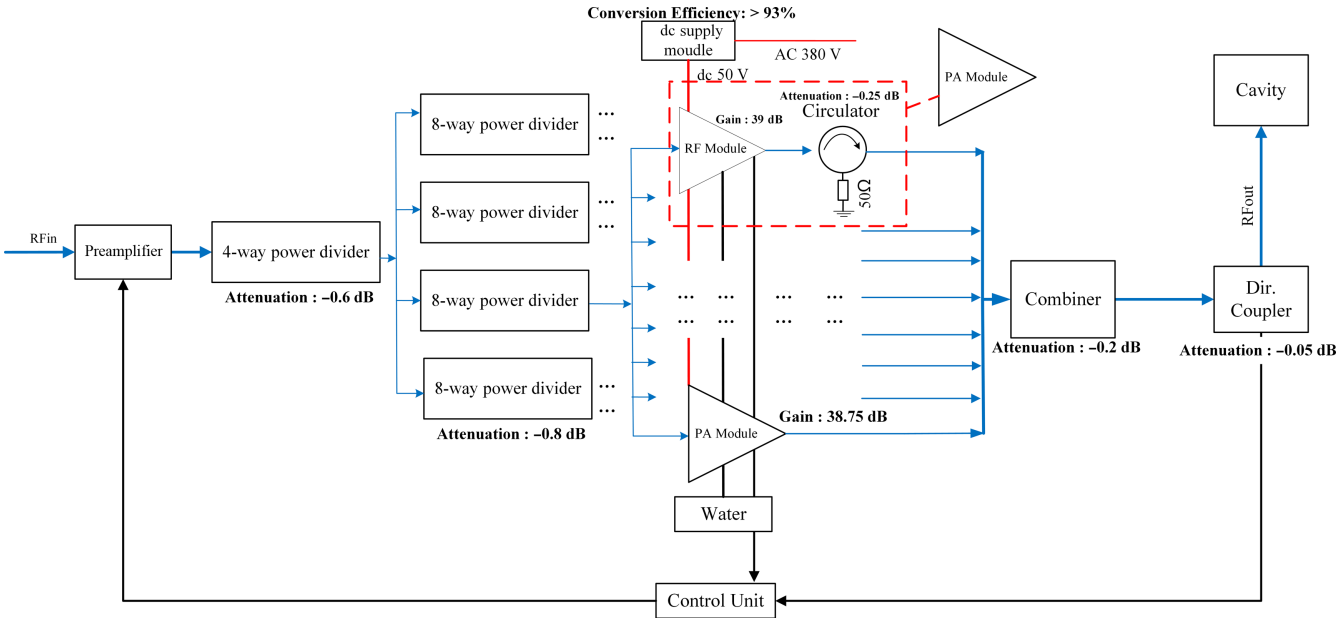


FIG. 4. The block diagram of 162.5-MHz SSPA components: the blue arrows represent the power flow, the red lines represent the power supply system, and the black arrows represent the data flow.

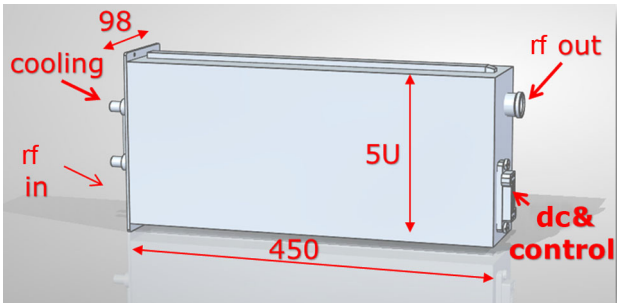


FIG. 5. The universal PA structure from standardization design.

size tolerance, assembly reference, and communication protocols to address process issues arising from different manufacturers.

Communication between the PA module and the dc module was established through the CAN protocol. Furthermore, the sharing of current from the dc power supply was facilitated using this same protocol. This protocol serves as an essential mechanism for the interchange of dc supply components.

The most crucial aspect of the design is universal PA size and interfaces, as shown in Fig. 5. This design strikes a balance between high power density and compact size. All interfaces and connectors were rigorously tested and confirmed through multiple investigations and experiments. For example, the output power can be adjusted according to beam intensity. A four-layer combining structure provides a fourfold range of power, with eight modules in each layer offering power tolerance in the event of failure or hot swap.

Due to energy supply and electromagnetic compatibility (EMC) requirements, the dc supply system is a critical component of the SSPA rack. Its module was designed for hot swapping to enable interchange during operation. Compared to the PA modules, hot swapping of dc supply modules is relatively easy. The primary challenge lies in conducting cooling in a limited area. A tensioner structure was designed to achieve a higher coefficient of heat transfer, as shown in Fig. 6.

The uniformity of interfaces is crucial in designing for reciprocity. After several years of research and measurement, we have determined specific interface types for the PA and dc supply modules, such as the water-cooling connector from STAUBLI and the electrical connector from AVIC. Currently, three prototypes of the SSPA have been completed and are operating on-site for an extended period, with modules from three different manufacturers that can be easily interchanged.

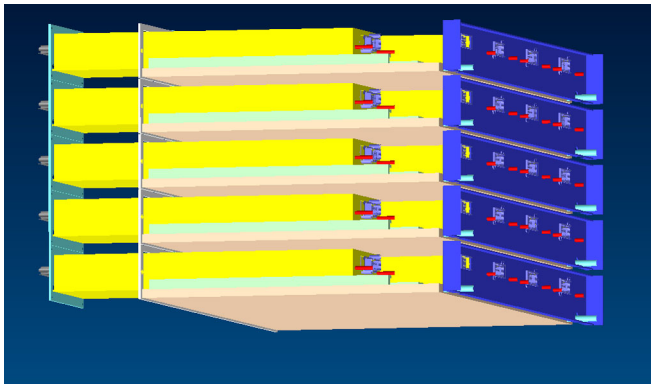

FIG. 6. The current-sharing dc supply structure from standardization design.

In addition, the consistency of the communication protocol and interlocking logic plays a vital role in standardization design. The reliable operation of the monitoring and interlocking system requires underlying hardware support, with communication address and pin feet definition being central to our design in addressing compatibility issues. Detailed communication protocols and hardware interface definitions were completed based on a universal motherboard, which will not be discussed here.

### B. Performance development

The first application of solid-state power sources in the accelerator was from the French SOLEIL and the European light source European Synchrotron Radiation Facility. Later, with the accelerated development of communication, LDMOS, as semiconductor tubes representative of low-frequency applications, are becoming more and more mature and have been more and more widely used in the field of accelerators recently [4]. C-ADS project (Chinese Accelerator Driven System) completed by the Institute of Modern Physics in 2016, which is the first linear accelerator project based entirely on solid-state power sources in China, including 160-kW radio frequency quadrupole (RFQ) and 10-mA superconducting cavities. During the whole project construction, its stability and reliability have been well verified.

After a serious accident involving a single external circulator, the design of high-power large single circulators was replaced with the distributed small-power circulator scheme. The latter has now become the preferred choice due to its better isolation and lower cost from domestic instrument providers. The necessity of combining the two schemes is being evaluated for high-intensity accelerators.

#### *1. Power amplifier module*

Recent advancements in LDMOS technology have enabled the pursuit of higher linear power. For example, the BLF189XRA can achieve up to 1200 W at 162.5 MHz with an efficiency exceeding 70%. At 325 and 650 MHz, the same power has been achieved with an efficiency consumption of 5%–10%, meeting the basic power specification for SSPA in CiADS.

For 81.25 and 162.5 MHz modules, an LDMOS transistor from AMPLEON semiconductor, the BLF189XRA, was selected to design PA modules. This device is designed for push-pull operation with a pair of transistors in a single ceramic package, providing 1200 W cw linear power at 162.5 MHz with an efficiency of 75%. A low-loss

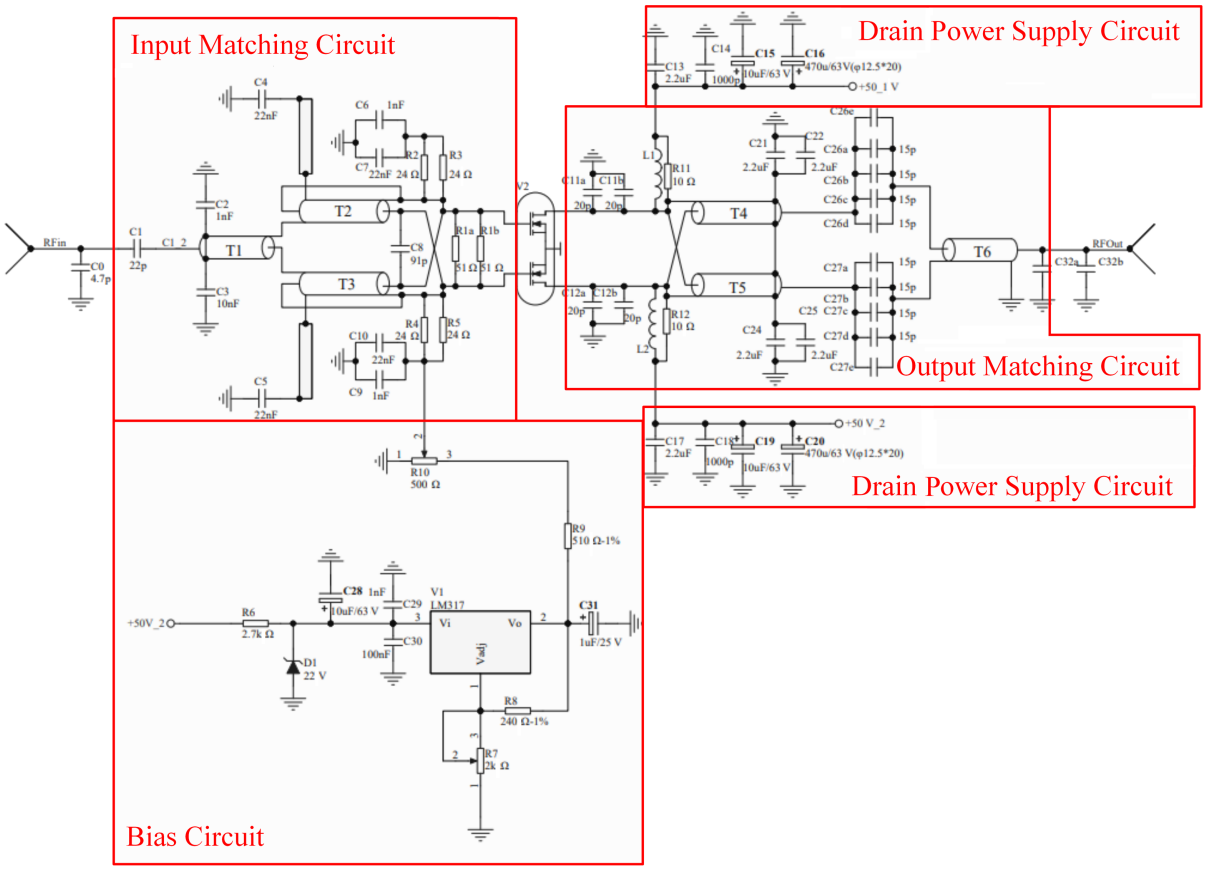


FIG. 7. Schematic of the amplifier module. The circuit mainly includes four parts: bias circuit, drain dc power supply circuit, input matching circuit, and output matching circuit.

circulator was added to the output of the power amplifier to protect the rf amplifiers against reflected signals due to undesired open, short, or mismatched load conditions. The basic circuit is shown in Fig. 7, with some modifications made to meet performance requirements. Specific LDMOS transistors were chosen for use at 325 and 650 MHz, and GaN semiconductor technology was applied at 650 MHz for higher rf conversion efficiency. This design approach was inspired by the European Spallation Source (ESS) project to save energy consumption for inductive output tube (IOT) power source development [5].

The 3D design of the PA was completed after numerous measurements and modifications. In particular, the balun was carefully optimized due to its temperature under strong reflection. The resulting printed circuit board (PCB) design is shown in Fig. 8.

The module was installed in a PA test case, complete with cooling connectors and electrical adaptors. The

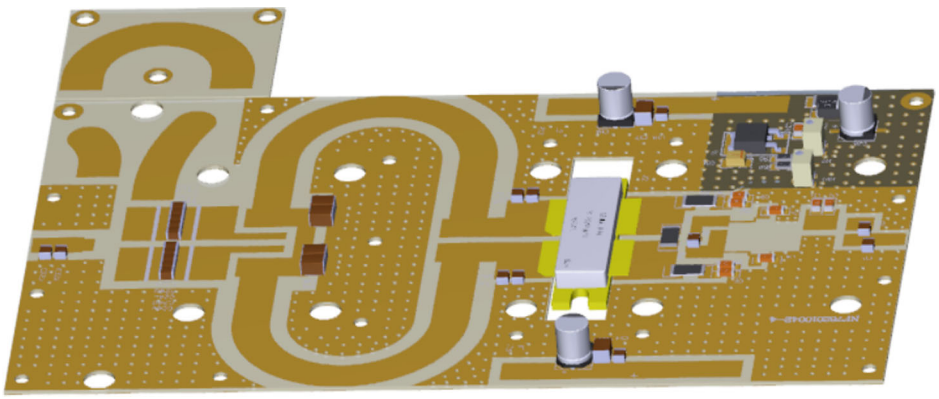

FIG. 8. PCB design of 162.5-MHz PA module.

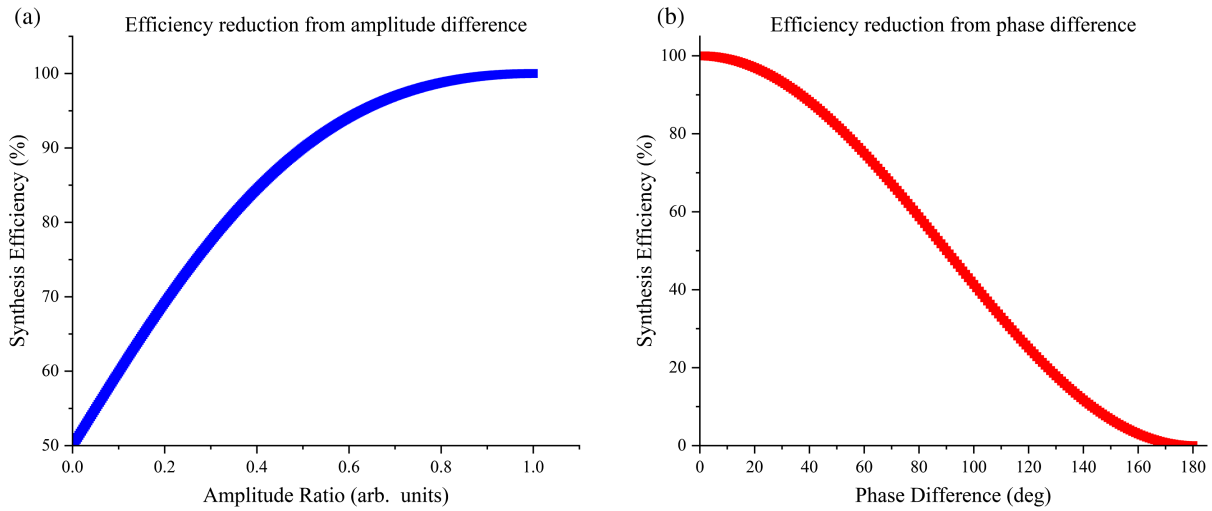


FIG. 9. (a) Efficiency reduction from amplitude difference, where the amplitude ratio is $P_1/P_2$. (b) Efficiency reduction from phase difference, where the phase difference is $\theta_1 - \theta_2$.

circulator and monitoring system were also tested to ensure the stable operation of the superconducting cavity (SC).

The gain of the module was meticulously verified to be below 40 dB to mitigate the risk of self-excited oscillations. An automatic adjustment mechanism for amplitude and phase was implemented to enhance the combining efficiency.

The circulator was specifically optimized to enhance isolation, and the fluctuation current was limited within $\pm 10\%$ from a sliding short during half wavelength.

Performance consistency was deemed crucial as variations in modules from different manufacturers could result in a significant decline in combining efficiency [6]. According to the analysis of the synthesis efficiency given by Eqs. (1) and (2), we calculated the amplitude difference and phase difference separately, which is shown in Fig. 9.

$$P_{\text{out}} = \frac{1}{2}[P_1 + P_2 + 2\sqrt{P_1 P_2}\cos(\theta_1 - \theta_2)], \qquad (1)$$

where $P_{\text{out}}$ is the combined output power in the presence of amplitude and phase inconsistencies, $P$ is the output power of each module, and $\theta$ is the corresponding phase of each module.

$$\eta = \frac{P_1}{P_1 + P_2} = \frac{1}{2} + \frac{\sqrt{P_1 P_2}}{P_1 + P_2}\cos(\theta_2 - \theta_1), \qquad (2)$$

where $\eta$ is the corresponding synthesis efficiency.

To ensure synthesis efficiency, the consistency requirement was limited with $\pm 0.25$ dB gain variation and $\pm 5°$ phase difference, as shown in Fig. 10.

We tested six modules from different manufacturers for a single combiner. All modules were fabricated according to standardized design specifications, and the variation analysis of amplitude and phase met the requirements outlined in Fig. 10. The total power was observed after combining the different modules with varying levels of gain and phase. Our results showed a maximum power loss of 2% in the

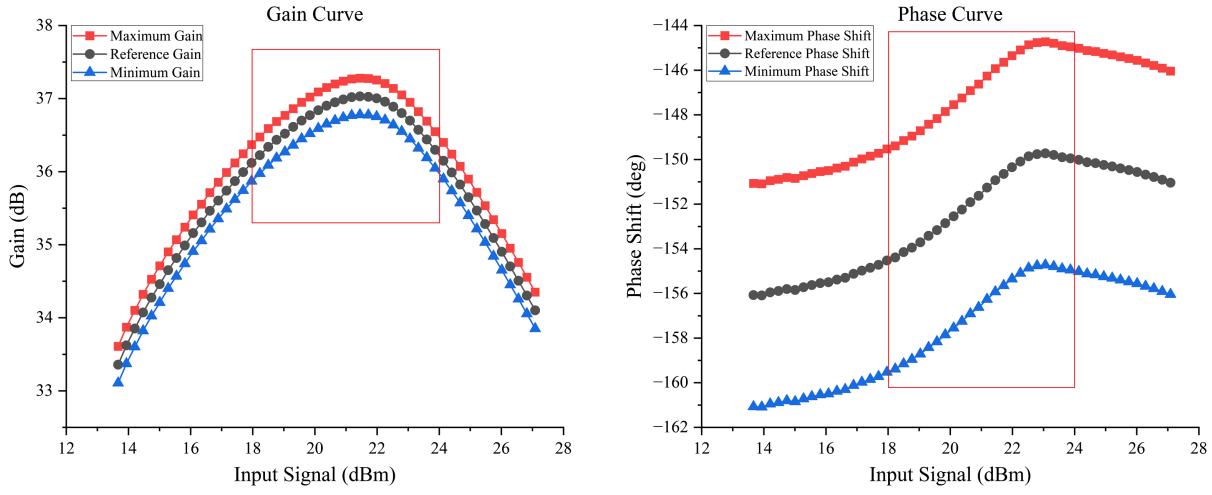


FIG. 10. Consistency requirements of amplitude and phase curves.

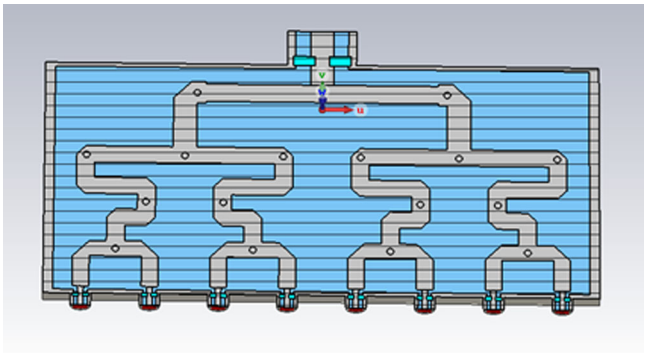

FIG. 11. The internal design of 162.5 MHz 6-and-1 air-suspended stripline combiner.

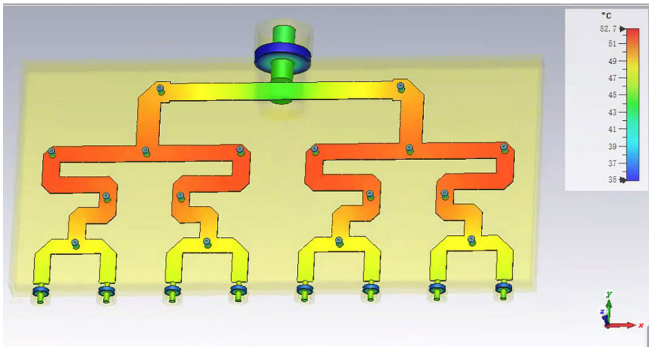

FIG. 12. The multiphysical field analysis of 162.5 MHz combiner to optimize parameters.

most extreme case of 12° phase and 0.5-dB gain difference, which is in excellent agreement with our calculations. This level of difference is easily achievable for manufacturers in terms of mass production.

For a single-layer, eight-in-one combiner, a maximum amplitude/phase difference of 0.5 dB/10° results in an additional efficiency loss of less than 1.13%. Given the difficulty of ensuring that products from different manufacturers fall within the threshold value, this loss is considered acceptable. In cases where very high efficiency is required, special methods such as amplitude and phase adjustment can be implemented automatically to achieve satisfactory results [7], which have already been tested and estimated at IMP.

A study was conducted to accumulate experience in technology and high-power density for high-performance modules. The ART2K0FE, a new AMPLEON LDMOS, can achieve up to 2 kW with 65 V $V_{DS}$. Two types of baluns, PCB and coaxial, were measured under high-power density conditions. The PCB balun was found to have higher linear power and a smaller size than the coaxial balun but at the cost of cooling and harmonic suppression. With a 60-V $V_{DS}$ and a PCB balun, the ART2K0FE transistor was able to stably achieve 1.4-kW linear power. The efficiency at the $P_{-1\,\mathrm{dB}}$ point was 73.5%, and the harmonic suppression was −45 dBc, both of which were in good agreement with the requirements.

In ongoing research, new semiconducting materials from civil technologies have demonstrated excellent performance in laboratory experiments, achieving higher efficiency and power. These results suggest that the performance of PA can be greatly improved soon.

### 2. High power combiner

In the initial design of the power source, all-in-one combiners employed a simple coaxial structure, with each amplifier connected by a long cable. However, due to the high-power density and standing wave operation, cables with diameters of up to 10–20 mm risked reducing rf heat performance and significantly impacting the layout of the rear machine during maintenance.

After careful analysis, the design of the "standardized" combiner was modified to incorporate an air-suspended stripline structure, as shown in Fig. 11. The connection between the PA modules and combiners was reconfigured for direct insertion, enabling hot swapping. This design effectively mitigates the impact of heat and bending stress along the cable, streamlining the rear structure, and enhancing the maintainability and reliability of the entire rack. Through multiple simulations and experiments, a combination efficiency of 98% and port isolation in the event of a single port failure were achieved.

As passive devices, all combiners, including splitters and couplers, were designed in-house using the CST computer code to simulate all parameters, as shown in Fig. 12. For standardization assessment, the first batch of prototypes was contracted to five different manufacturers, with assembly and testing performed in-house. Specific simulation details and mechanical processes were negotiated and rechecked collaboratively. Table I presents a measured

TABLE I. The design example of 8 − 1 combiner at 162.5 MHz.

| Parameters | Measured results | Simulated results | |
|---|---|---|---|
| Output port | Log (dB) | −28.968 | −29.157 |
| Input port 1 | Log (dB) | −9.033 | −9.06 |
| | Phase (°) | 163.007 | 148.32 |
| Input port 2 | Log (dB) | −9.025 | −9.03 |
| | Phase (°) | 163.240 | 147.70 |
| Input port 3 | Log (dB) | −8.993 | −9.03 |
| | Phase (°) | 164.201 | 147.65 |
| Input port 4 | Log (dB) | −9.011 | −9.07 |
| | Phase (°) | 163.338 | 148.40 |
| Input port 5 | Log (dB) | −9.095 | −9.07 |
| | Phase (°) | 163.199 | 148.40 |
| Input port 6 | Log (dB) | −9.082 | −9.04 |
| | Phase (°) | 163.940 | 147.65 |
| Input port 7 | Log (dB) | −9.067 | −9.04 |
| | Phase (°) | 163.785 | 147.71 |
| Input port 8 | Log (dB) | −9.108 | −9.06 |
| | Phase (°) | 162.830 | 147.43 |

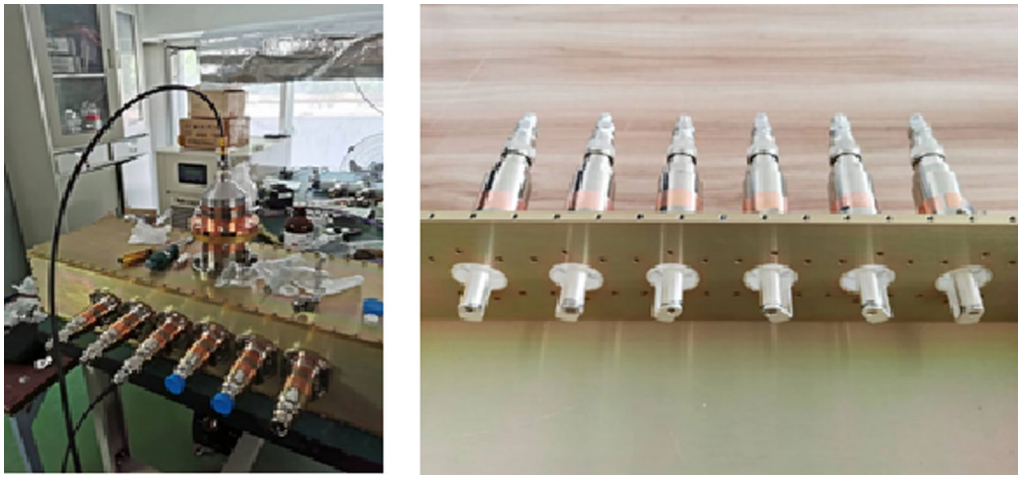

FIG. 13. The resonator combiner prototype and its coupling loops.

example of a combiner. The combining loss is less than −0.05 dB.

For superconducting cavities, strong reflection must be carefully considered in the design of power combining.

The isolation is complex for high-power combiners due to the issue of balancing resistance. During full reflection operation, rf power flow is rearranged according to the phase from the reflected surface due to a failed PA module, which will be described in detail in the next chapter.

A new combiner based on an empty resonator was developed for the new SSPA rack, and its prototype has been carefully measured using a four-port vector network analyzer. Rotating one coupling loop can isolate the corresponding port from the entire system, with a worsening S parameter of the remaining ports. For a 12-in-1 or 16-in-1 combiner system, the mismatch can be compensated by adjusting the remaining loops. The specific structure is shown in Fig. 13.

Another combiner for the high-intensity accelerator was designed and measured. The chain combining structure at 650 MHz was researched due to the compact size and higher frequency. The 150-kW cw power experiment in Fig. 14 shows good agreement with the combining simulation.

### *3. DC supply module*

The development of the dc power supply has undergone several iterations. The initial design featured a large heat sink with PA and dc supply modules placed on opposite sides at the shortest distance. However, the issue of thermal grease during maintenance proved inconvenient. Subsequently, a smaller heat sink with a double-sided design and a modular pluggable structure was implemented, greatly improving maintenance efficiency.

The current standardized design positions the dc supply modules away from PA modules for better redundancy. This configuration allows for current-sharing control of the relatively independent dc supply, ensuring that the failure of individual modules does not impact the rated output power. This design offers significant advantages in terms of high-power operation and long-term stability. The development process is illustrated in Fig. 15.

The dc supply module was designed to deliver an output of 5 kW at 50 V, with dimensions of $185 \times 60 \times 520$ mm$^3$ (width × height × depth), as shown in Fig. 16.

Due to the requirements of pulsed operation and EMC, particular attention was paid to specifications such as power factor, total harmonic distortion (THD), and three-phase

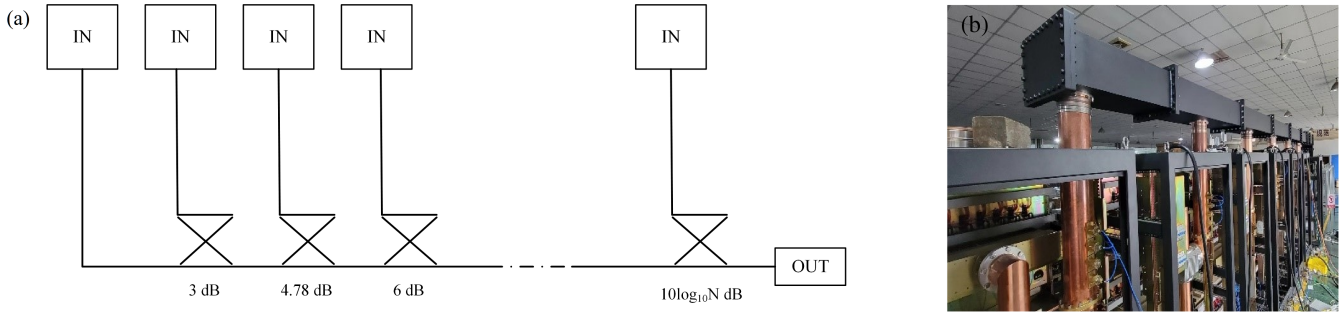


FIG. 14. (a) Principle of the chain combiner. (b) High-power experiment of chain combiner.

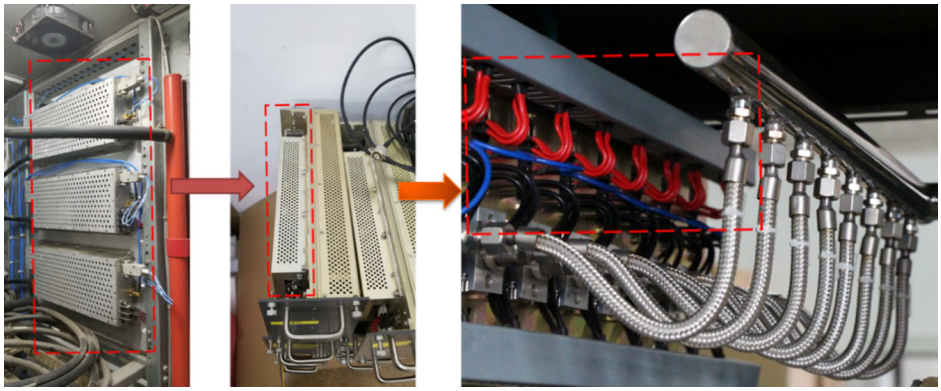

FIG. 15. Development of the supply form of dc power supply.

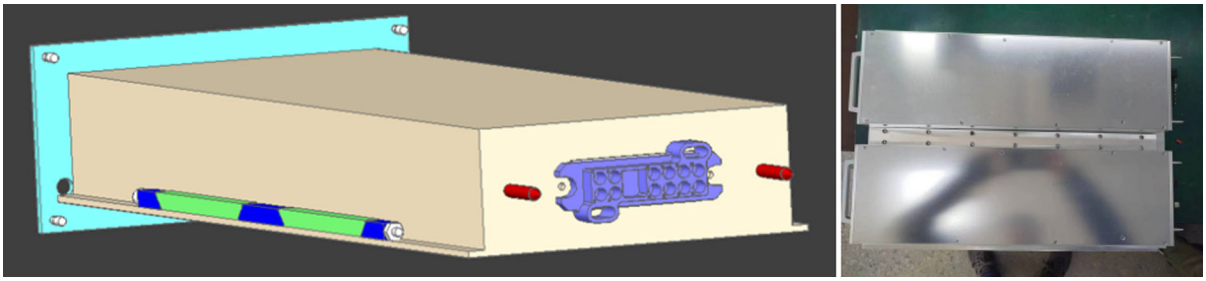

FIG. 16. The structure of dc module with two fastening strips.

equilibrium, as detailed in Table II. Special methods for contact cooling are currently being tested.

### C. Key technology-hot swap

The failure of an individual PA module in a solid-state power source can result in the breakdown of the entire rf system [8]. This typically affects all operating conditions and can only be repaired during a scheduled machine shutdown, significantly increasing failure time and reducing beam efficiency. When an individual power amplifier module fails, the working state of other parallel modules may change drastically, potentially leading to port damage or even serious accidents during long-term operation. Additionally, the failure of a single power amplifier module can result in a decrease in overall synthesis power greater than the normal output power from the modules, affecting overall synthesis efficiency. Implementing hot-swap

TABLE II. The specifications of dc supply module.

| Input | ac 380 ± 15% VAC, TN-S |
|---|---|
| ac frequency | 50 Hz |
| Max output current | ≤100 A |
| Power actor | >0.95 at full power |
| Outputs | dc 48–65 V |
| Output power | 5 kW maximum |
| Efficiency | >93% |
| Ripple/noise | ≤300 $mV_{pk\text{-}pk}$ with 20 MHz bandwidth |
| Line regulation/load regulation | ≤1% of output voltage |
| THD | ≤10% of harmonic voltage and current |
| Three-phase equilibrium | ≤1% of rated power |
| Operating Temp. | +5 to +50 °C |
| Storage Temp. | −40 to +85°C |
| Humidity | 0% to 95% noncondensing |
| Cooling | Liquid cooling |

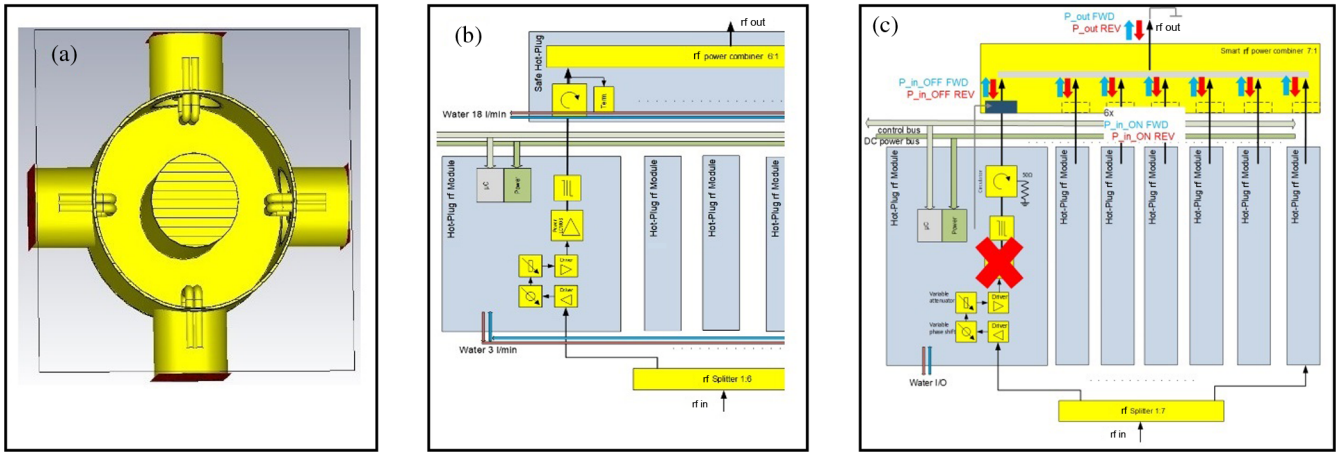


FIG. 17. Three solutions to hot swap developed in IMP: (a) cavity combiner type, (b) load separation type, and (c) fixed open-circuit type.

technology can significantly simplify SSPA maintenance, increase synthesis efficiency, and improve the availability of the entire machine.

There are three methods for implementing hot-swap technology, as depicted in Fig. 17. Mode (a) of the resonator combiner involves adjusting the coupling power of each branch by rotating the joint to fully isolate it from the combiner. When hot swapping is required, the coupling degree is adjusted to 0, decoupling the branch from the combiner and allowing it to be removed. However, slight fine-tuning of the coupling degree of other branches may also be necessary. Mode (b) involves placing a circulator and load on the combiner side to ensure that the corresponding port of the combiner is in a matched state when the module is removed. However, replacing the circulator and load in the event of a fault can be difficult. Mode (c) realizes hot swap mainly by designing the input port reflection phase of the combiner. When a module is pulled out, the combiner port is OPEN and has a reflection coefficient of 1. If the synthesis node's reflection coefficient is also designed to be 1, the combiner can continue to operate normally.

Currently, cavity combiner and load separation types are in the experimental stage, while the fixed open-circuit type has been designed and is in the prototype processing and experimental testing phase.

### *1. The theory of single-port failure*

When a PA module is removed from a fixed open-circuit combiner, the corresponding port then transitions to the open state and the power state in this open arm can be represented by Fig. 18. As a result, when viewed from the combiner synthesis node, the impedance at the port is infinite. Since the synthetic node and the open circuit point are connected through a microstrip line or other rf cable which insert phase is $\varphi_i$. If the study plane is chosen to be close to the combiner node, the reflection coefficient looking toward the open circuit point can be expressed as $\Gamma_i e^{-j2\varphi_i}$. Assuming that the load at the synthesized port also has reflection, the reflection coefficient of the synthetic node looking at the load can be expressed as $\Gamma_{n+1} e^{-j\varphi_{n+1}}$, and its phase includes the reflection phase of the load and the twofold transmission phase shift from the synthetic node to the load.

Based on the conservation relation, the power of the synthesized port can be obtained as Eq. (3). In the load separation formula, the reflected power of each port is absorbed by the load, and the output power can be expressed as Eq. (4). In the adjustable coupling mode, the combiner will become an ideal $(N-1)$ channel combiner because the unplugged port is decoupled, and the output power can be expressed as Eq. (5).

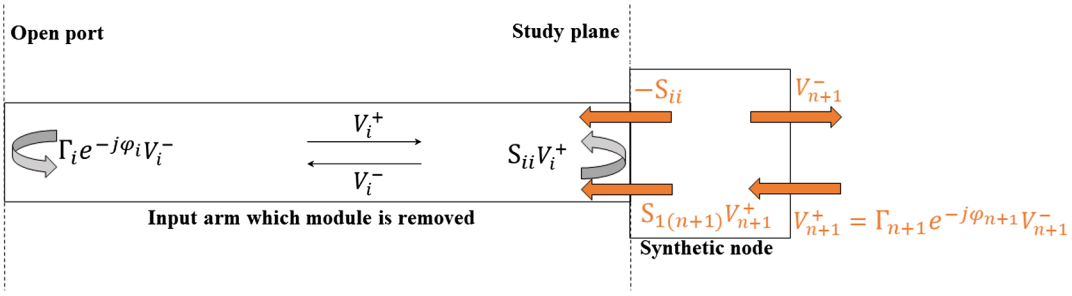


FIG. 18. Power flow in open port combiner: $S_{ii}$ is the reflection coefficient of input port $i$, $S_{1(n+1)}$ is the transition coefficient between input port and synthesized port, and $V$ is the voltage in the corresponding direction.

TABLE III. Theoretical power drop caused by single module pulling out.

| | Adjustable coupling type | Load separating type | Fixed open circuit |
|---|---|---|---|
| 6 and 1 | −16.67% | −30.56% | −0.5% to 30.48% |
| 32 in 1 | −3.13% | −6.15% | −0.1% to 6.13% |
| 100 in 1 | −1% | −1.99% | −0% to 1.98% |

TABLE IV. Power reduction measurement when a single module is removed.

| | Test power | Power change | The phase change |
|---|---|---|---|
| 6 and −1 | A closed-loop 4.5 kW | −31.7% | 1° |
| | A closed-loop 5 kW | −30.8% | 2.18° |
| | Open loop 6 kW | −32.4% | 2.11° |
| 32 in 1 | Open loop 7.5 kW | −8% | 0 |
| | Open loop 13.4 kW | −7.5% | 0 |
| | Open loop 21.3 kW | −6.1% | 0 |
| | Open loop 29.6 kW | −5.1% | 0 |

$$P_{n+1}^{-} = \left( \frac{(n - n\vec{\Gamma}_i S_{ii} - 1) S_{1(n+1)}}{1 - \vec{\Gamma}_i S_{ii} - \vec{\Gamma}_i \overrightarrow{\Gamma_{n+1}} S_{1(n+1)}^2} \right)^2 \tag{3}$$

$$P_{n+1}^{-} = \frac{(n-1)^2}{n} \tag{4}$$

$$P_{n+1}^{-} = n - 1. \tag{5}$$

These three types of hot-swap methods do not affect the synthesis phase, mainly reflected in the different degrees of output power decline. Table III lists theoretical power decline for three types of one-stage combiner when the reflection coefficient of the load is $0.98e^{-j\varphi_{n+1}}$ and the reflection coefficient of the open circuit point is 0.98.

When the number of synthetic routes is large, the power decrease caused by the hot-swappable module is small. However, when the number of synthetic routes is small, the power decrease caused by the module is obvious. The power decrease level in the fixed open-circuit scheme is related to the reflection phase $\varphi_{n+1}$, the power decrease level close to 0% under $\varphi_{n+1} = 0$, if $\varphi_{n+1} = \pi$, the power decrease level reaches the maximum value.

### 2. The measurement of hot swap

For the hot-swap experiment, we selected a 32-kW power source rack from manufacturer 1 and a 6-kW power source (single layer) from manufacturer 2. The results are shown in Table IV.

The measured results of hot swap are consistent with the theoretical values in Table III. In the 32-in-1 power synthesis, the variation in power decrease levels can be attributed to changes in the insertion phase shift of the entire machine during power increase, resulting in changes in the load reflection phase.

In the experiment to assess the impact of hot swap on the low-level rf (LLRF) control loop, depicted in Fig. 19, a resonator cavity was prepared as a 6-kW load to measure changes in amplitude and phase. The results are shown in Fig. 20.

During the test, it was observed that the cavity voltage experienced a sudden drop with pulling out. The phase and amplitude of the cavity voltage reached the closed-loop set value after approximately 100 ms, and the LLRF closed loop did not break. During the insertion process, the phase and amplitude of the cavity voltage were effectively controlled after approximately 50 ms, indicating that the LLRF was able to effectively control the loop during insertion. Additionally, during hot swapping, the forward and reverse power of SSPA

FIG. 19. The special measured test for hot-swappable function.

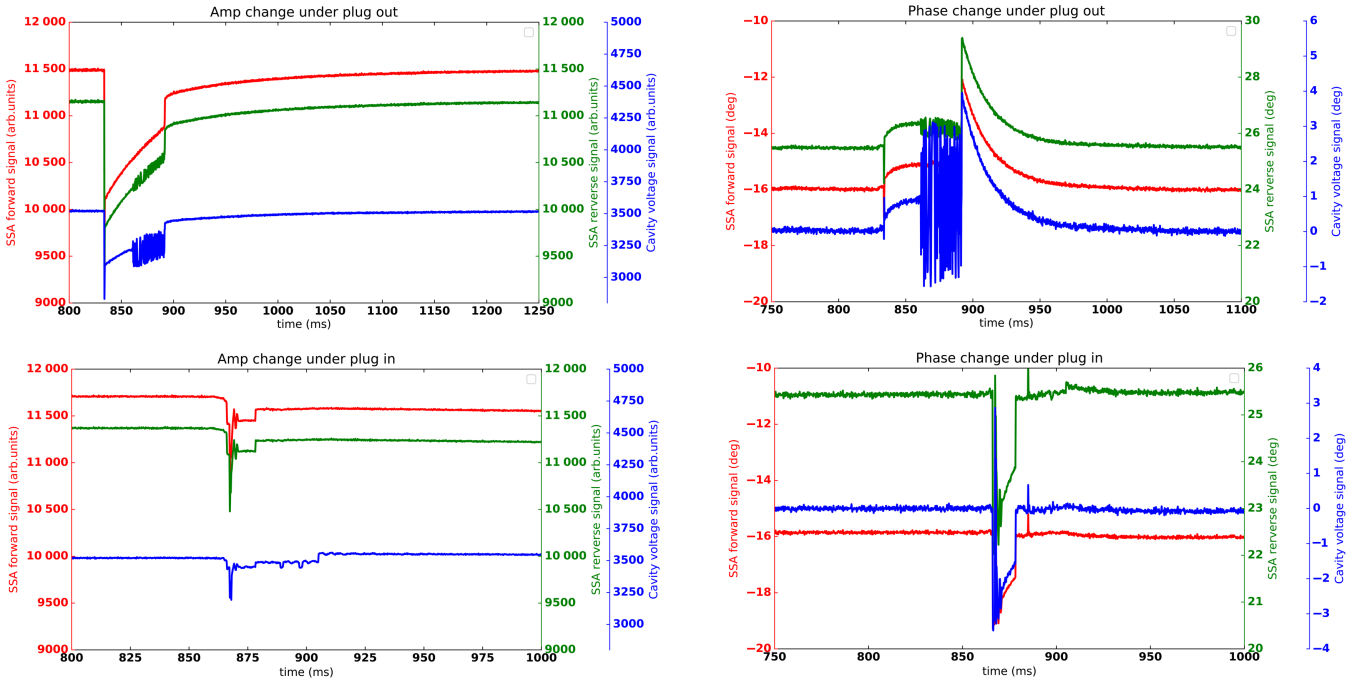


FIG. 20. Amplitude and phase change during the hot swap when 4.5 kW closed loop.

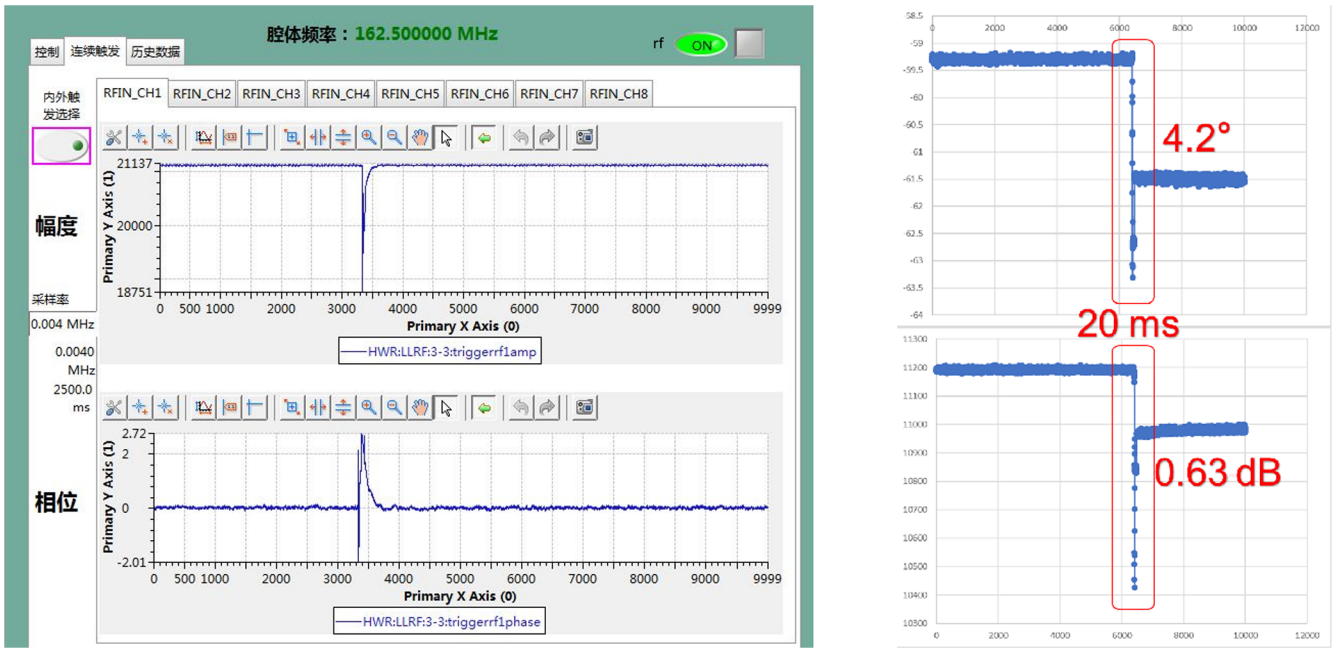


FIG. 21. Hot swap on-load experiment under LLRF closed loop in IMP.

remained stable and did not run out of control. The power drop level is presented in Table III under plug-out. When the LLRF loop was opened, fluctuations of 0.63 dB and 4.2° in amplitude and phase were observed, as shown in Fig. 21.

With adjustable coupling and the fixed open circuit, the synthesis efficiency of SSPAs can be improved, thereby enhancing rf power availability. When the amplitude-phase loop is closed, the amplitude and phase fluctuations caused by hot swapping are less than or equal to 100 ms, and the control loop remains closed. This indicates that the system is capable of effectively managing fluctuations during hot swapping.

## IV. MEASUREMENTS OF PROTOTYPE MACHINE

Three new SSPA prototypes were tested, including one set of RFQ power sources comprising eight racks that combined to produce 200 kW of cw power (four sets of

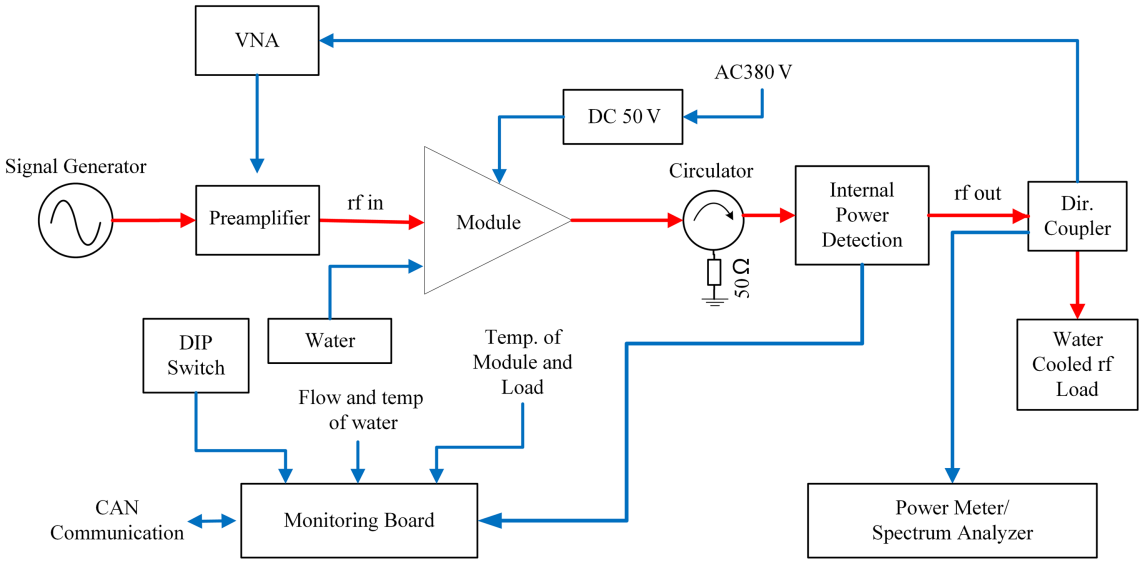


FIG. 22. The measurement block diagram of single module.

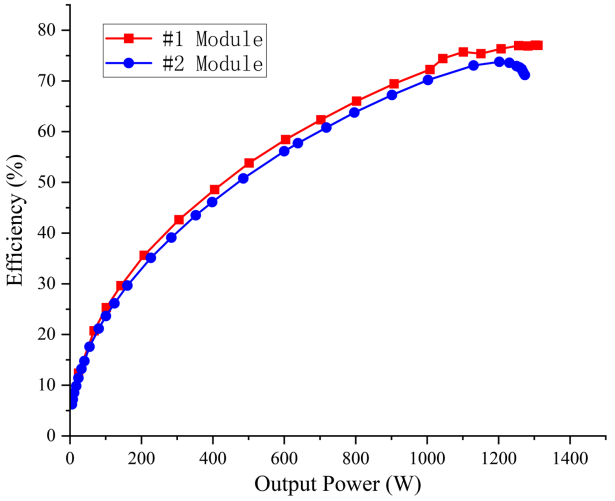


FIG. 23. Measured efficiency of single module at 162.5 MHz.

50-kW amplifiers), and two sets of 24-kW amplifiers for the SC. Of the 304 modules tested, only three exhibited minor issues that were quickly resolved. Measurements of cw-rated power were conducted on a dummy load and customized sliding short.

The complete rf system, including the power source, cavity, control, and LLRF system, was installed in the machine in the spring of 2021 and commissioned the following summer. The system has operated for approximately 4000 h and has proven to be highly reliable, without beam time loss attributed to SSPA. Additionally, the system is easy and flexible to operate.

### A. Test of standardized module

The measurement block diagram is presented in Fig. 22 and comprises a signal generator (R&S SMB 100A), preamplifier (Mini-Circuits ZHL-03-5WF+), directional

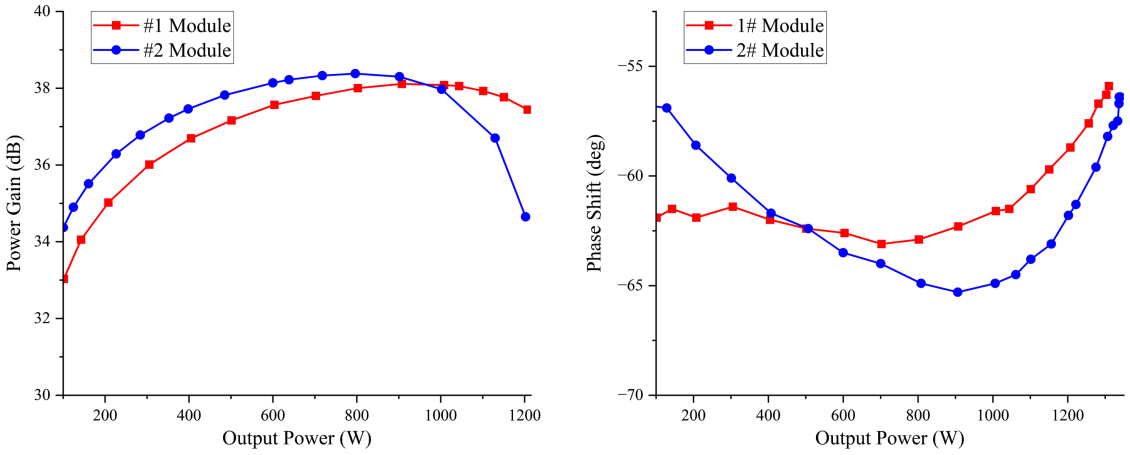


FIG. 24. Measured results of gain and phase curve at 162.5 MHz.

TABLE V. Measured harmonics and spurious power of single module.

| Power output | Results | Power rating (W) |
|---|---|---|
| Harmonics (dBc) | −35.61 | 100 |
| | −32.87 | 600 |
| | −31.95 | 1200 |
| Spurious (dBc) | −68.51 | 100 |
| | −66.99 | 600 |
| | −72.65 | 1200 |

coupler (Exir MDIR-2039-11-A), 50V dc power supply, power meter (Agilent N1914A power sensor), Vector Network Analyzer (R&S ZND), and a water-cooled rf load. The preamplifier is a broadband amplifier with a power gain of 30 dB and gain flatness of ±1.0 dB over a frequency range of 60–300 MHz. The output directional coupler, manufactured by Exir, has a coupling coefficient of 60 dB and a directivity of 42 dB.

The two-port vector network analyzer (R&S ZND) is used to measure the gain and phase characteristics of the standardized module through power and frequency sweeps. The power meter and spectrum analyzer are also employed to measure the rf efficiency, harmonics, and spurious spectrum.

The performance results are shown in Fig. 23. The rf efficiency of the No. 1 and No. 2 module are 75.3% and 73.2%, respectively, at 1-dB compression point. The maximum power of a single module is up to 1.3 kW.

The module gain is approximately 37 dB at an output power of 1.1 kW. Figure 24 shows the relationship between the phase shift and output power at 162.5 MHz.

The single module has a maximum phase deviation of 10°. The measured harmonics and spurious power is shown in Table V.

The harmonic is well below −30 dBc, while the spurious is below −70 dBc when the output power is 1.2 kW. The temperature of the transistor and balun was measured using an infrared thermal camera (FLIR E40), with all components exhibiting a surface temperature of less than 100 °C, as shown in Fig. 25. Multiphysics simulations may analyze the surface temperature resulting from thermal simulation according to the structure and cooling liquid, with results expected to be consistent with the measured cloud map.


FIG. 25. Measured surface temperature of the module at 1.2-kW output power.

FIG. 26. Test setup of the 50-kW power amplifier.

### B. High power test of 162.5 MHz/50-kW SSPA

Two 26-kW amplifier racks were developed to create a 50-kW amplifier with an additional two-port coaxial

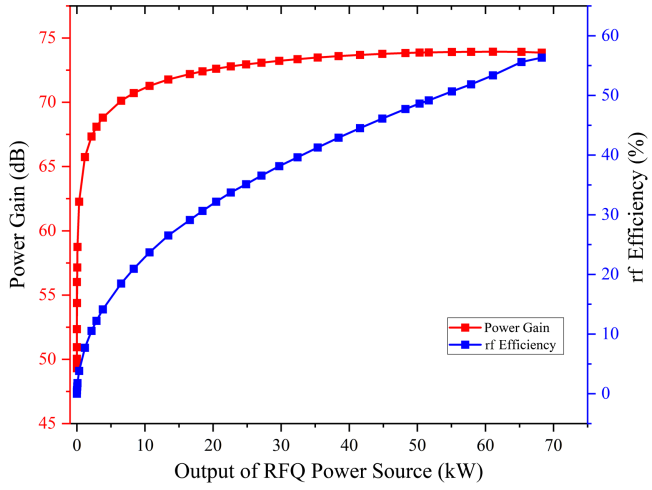


FIG. 27. Measured power gain and rf efficiency of integrated power amplifier.

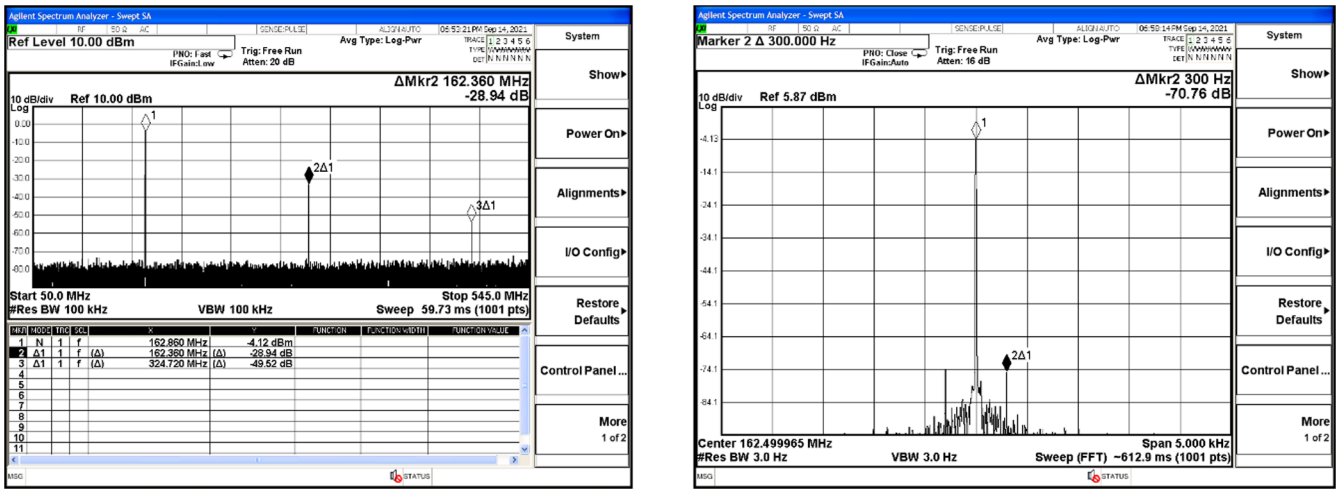


FIG. 28. Measured harmonics and spurious spectrum with the output power of 50 kW.

combiner, as shown in Fig. 26. The integrated power amplifier was tested using a $6-1/8$-inch directional coupler to monitor the output power, and a water-cooled 100 kW/50 Ω load was used to dissipate the output rf power.

As depicted in Fig. 27, the power gain and rf efficiency of this 50-kW amplifier were measured. The peak gain was observed at an output power of 65 kW, with the maximum measured output power reaching 68 kW. The dc to rf conversion efficiency demonstrated an upward trend with increasing output power, reaching an efficiency of 56% at the maximum output power of 68 kW. Operating the integrated amplifier at this power corresponds to each PA module functioning at 1250 W (64 modules). The efficiency of an individual PA module is almost 71% at an output power of 1250 W, which means the efficiency of this amplifier is finally reduced by 15%.

The suppression of harmonics and spurious signals was measured using a spectrum analyzer. The second harmonic frequencies were suppressed to −34.94 dBc (with a −6 and −9 dB correction for second and third harmonic suppression, respectively, based on the measured signal from the directional coupler), while the suppression of spurious signals was measured to be better than −70 dB, as shown in Fig. 28.

A 24-h long-term test was conducted to assess the performance of the 50-kW amplifier in terms of output power and phase stability. As shown in Fig. 29, the fluctuations of the open-loop output power and phase were 0.06 dB and 1°.

In the end, a 1-h full reflection test was conducted to verify the capability of withstanding full reflection power without the external circulator. A coaxial $6-1/8$-inch short terminal was used in place of the 50-kW load to generate a standing wave.

The open loop output power stability was 0.06 dB, and the phase dropped by 2.5° during the test, as shown in Fig. 30. The rf field intensity measurement was performed,

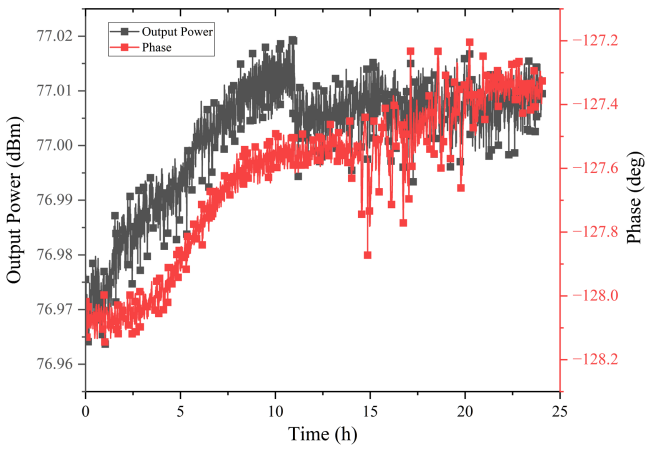


FIG. 29. Output power and phase stability test at 162.5 MHz with the output power of 50 kW.

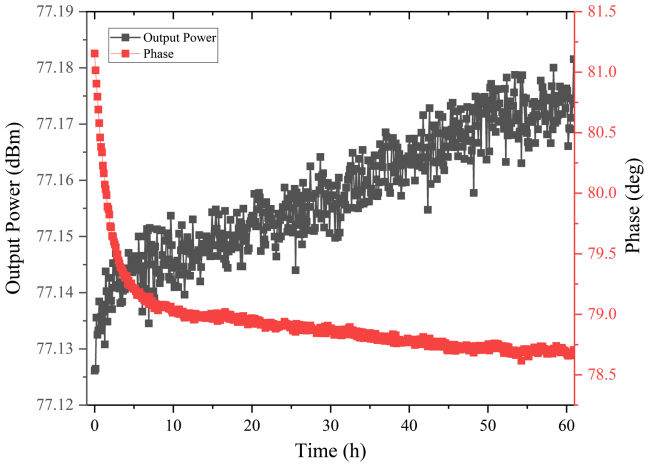


FIG. 30. Output power and phase stability under full mismatch at 162.5 MHz with the output power of 50 kW.

TABLE VI. Performance of 50-kW amplifier.

| Parameter | Measured value |
|---|---|
| Operating frequency | 162.5 MHz |
| Bandwidth | ±2 MHz |
| Max output power | 68 kW |
| Gain | 73.92 dB at 50 kW |
| Harmonics level | −34.94 dBc at 50 kW |
| Spurious level | −70.76 dBc at 50 kW |
| Power factor | >0.98 at full power |
| RF Efficiency | 55.0% at 50 kW, 56.3% at 68 kW |
| Amplitude stability | −0.88% to + 0.40%/24 h |
| Phase stability | −0.5° to + 0.4°/24 h |

revealing a maximum rf emission level was 28.3 $\mu W/cm^2$ at the distance of 1 m from the amplifier. This value is significantly lower than the allowed exposure limit (200 $\mu W/cm^2$ at 162.5 MHz).

An RFQ cavity at 162.5 MHz needs almost 200-kW power to accelerate the protons to 2.1 MeV. Its four couplers were designed at two sides of the cavity. According to the rf design, eight standardization racks were divided into four groups, with each group corresponding to a coupler. The main specifications of a 50-kW amplifier, comprising two identical racks, are measured and listed in Table VI.

The entire rf system was installed and put into operation in August 2021. Over a period of more than 12 months, no significant deterioration in gain or PA failure was observed.

## V. CONCLUSION

The design and improvement of the SSPA application in IMP were researched and summarized, with high power density and strong standing wave identified as two key requirements. For future large-scale accelerator development, stability, availability, and maintainability were carefully considered to create a new SSPA design standard, "standardization," which provides new design ideas for critical components according to the accelerator application and introduces new characteristics—reciprocity and hot swap. This represents a significant step forward in terms of convenience and usability for maintenance.

To date, three new prototype SSPAs by different manufacturers following the standardization have been completed and are operating on-site. Their specifications and performance are entirely satisfactory, demonstrating high levels of reliability, accessibility, and flexibility in operation. All PA modules can be easily interchanged and support essential hot-swap functions.

The logical control and port full isolation on the combiner will be measured and tested for all machines. Special designs and experiments, such as a prototype of the resonator combiner, will be implemented. An improved version, which meets the requirements of hot swap, by realizing full isolation on a single port through tuning the loop slightly, is expected to be completed within 2 months.

Investigations into suitable transistors for frequencies from 325 MHz to 1.3 GHz are ongoing. At 162.5 MHz, ART2K0FE was researched deeply for power density, efficiency, and linearity. Some SSPA standards are going to be applied as accelerators or industry applications. Several manufacturers have expressed their intention to adopt the SSPA technology and collaborations both domestically and internationally are underway.

## ACKNOWLEDGMENTS

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[1] A. V. Smirnov, Combiner-based method for efficiency enhancement of power amplifiers operating in a broad dynamic range, Nucl. Instrum. Methods Phys. Res., Sect. A **931**, 207 (2019).

[2] P. Marchand, T. Ruan, F. Ribeiro, and R. Lopoes, High power 352 MHz solid state amplifiers developed at the Synchrotron SOLEIL, Phys. Rev. ST Accel. Beams **10**, 112001 (2007).

[3] B. Kaizer, I. Fishman, A. Perry, L. Weissman, T. Zchut, J. Luner, E. Farber, A. Azoulay, and S. Robin, High power solid state RF amplifiers for SARAF Phase II Linac, Nucl. Instrum. Methods Phys. Res., Sect. A **1039**, 167001 (2022).

[4] B. V. Ramarao, S. Sonal, J. K. Mishra, M. Pande, P. Singh, G. Kumar, and J. Mukherjee, Development of 3 kW at 325 MHz solid-state RF power amplifier using four power amplifier modules, Nucl. Instrum. Methods Phys. Res., Sect. A **735**, 283 (2014).

[5] M. Jensen *et al.*, Testing of the ESS MB-IOT prototypes, in *Proceedings of 9th International Particle Accelerator Conference, IPAC-2018 Vancouver, BC, Canada* (JACoW, Geneva, Switzerland, 2018), pp. 1759–1764, https://doi.org/10.18429/JACoW-IPAC2018-WEXGBF1.

[6] M. Gaspar, M. Pedrozzi, L. F. R. Ferreira, and T. Garvey, A compact 500 MHz 4 kW solid-state power amplifier for

accelerator application, Nucl. Instrum. Methods Phys. Res., Sect. A **637**, 18 (2011).

[7] H. Büttig, A. Arnold, A. Büchner, M. Justus, M. Kuntsch, U. Lehnert, P. Michel, R. Schurig, G. Staats, and J. Teichert, RF power upgrade at the superconducting 1.3 GHz CW LINAC "ELBE" with solid state amplifier, Nucl. Instrum. Methods Phys. Res., Sect. A **704**, 7 (2013).

[8] S. Liepeng, Y. Zhenyu, Z. Cheng *et al.*, Analysis of modules failure in solid-state amplifier for high current RFQ, High Power Laser Part. Beams **31**, 065103 (2019).