

Proposal of a free-space-to-chip pipeline for transporting single atomsAiping Liu ^{1,2}, Jiawei Liu,^{1,2} Zhanfei Kang,^{1,2} Guang-Jie Chen,^{3,4} Xin-Biao Xu,^{3,4} Xifeng Ren ^{3,4}, Guang-Can Guo,^{3,4} Qin Wang,^{1,2,*} and Chang-Ling Zou^{3,4,†}¹*Institute of Quantum Information and Technology, Nanjing University of Posts and Telecommunications, Nanjing 210003, China*²*Broadband Wireless Communication and Sensor Network Technology, Key Lab of Ministry of Education, Nanjing University of Posts and Telecommunications, Nanjing 210003, China*³*CAS Key Laboratory of Quantum Information, University of Science and Technology of China, Hefei 230026, China*⁴*CAS Center for Excellence in Quantum Information and Quantum Physics, University of Science and Technology of China, Hefei 230026, China*

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A free-space-to-chip pipeline is proposed for the efficient transportation of single atoms from a magneto-optical trap to an on-chip evanescent-field trap. Due to the reflection of the dipole laser on the chip surface, the conventional conveyor-belt approach can transport only atoms in close proximity to the chip surface, with a distance of about one wavelength. This limitation hinders the efficient interaction between the atom and the on-chip waveguide devices. Here, a two-layer photonic chip architecture is proposed to realize a free-space-to-chip atom pipeline. By employing a diffraction beam of the integrated grating with an incident angle of the Brewster angle, the reflection of the dipole laser is suppressed, allowing the atoms to be brought to the chip surface with a distance of only 100 nm. The pipeline is verified numerically and provides a reliable atom source for a hybrid photonic-atom chip.

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In recent decades, neutral atoms have emerged as one of the most important systems for quantum information processing and have attracted increasing attention due to their potential applications [1–3]. Quantum systems based on single atoms can demonstrate nonclassical effects and verify quantum theory [4] and have been extended to quantum computing and quantum communication [5–9]. For these applications, optical dipole traps have become a common tool for trapping and manipulating neutral cold atoms because atoms can have long trapping times, especially for far-detuned frequencies [10,11]. Various configurations of optical dipole traps have been proposed and investigated in recent decades [12–16]. Additionally, optical cavities have been introduced to enhance the interaction between atoms and photons [17,18]. Recently, strong coupling between arrays of atoms [19–21] and multiple cavities [22,23] was demonstrated. With these advantages, optical dipole traps and optical cavities have become the main platforms for realizing atom-based quantum optical devices.

With the rapid development and maturity of integrated optical technology, there is a demand for integrating atoms into photonic chips [3,24–28]. Compared with conventional atom and cavity systems, a hybrid-photonic-atom-chip system offers many advantages, including high stability and robustness, strongly enhanced light-matter interaction, flexibility in

engineering long-range atom-atom interaction, and great extensibility of devices on a single chip. In addition, the photonic chip also provides a potential solution to realize an efficient and compact magneto-optical trap (MOT) for atom cooling [29–31]. Therefore, the hybrid photonic-atom chip enables cooling, transport, stable on-chip trapping, and manipulation of single atoms, offering a scalable solution for quantum optical devices.

However, it is very challenging to bring cold atoms from the free-space MOT to the surface of the chip at a subwavelength distance [12,32,33]. The evanescent field of confined optical modes on a photonic chip decays significantly in vacuum, requiring an atom-surface distance of around 100 nm for stable on-chip atom trapping. Nonetheless, the reflection and scattering of the dipole laser on the chip surface distort the distribution of the trap potential and prevent the atoms from approaching the chip. Several methods have been proposed to transport cold atoms from free space to photonic chips [34–37]. However, achieving efficient and precise atom delivery beyond the limit of the “last 1 μm ” remains a critical area of exploration for the advancement of atomic chips. One potential approach to circumvent this problem is to introduce an antireflection coating and the Brewster angle [38–40] on the surface of the photonics chip to prevent light reflection.

In this work, an efficient free-space-to-chip pipeline is proposed for a hybrid-photonic-atom-chip platform, enabling the transport of single atoms to an on-chip evanescent-field trap. A free-space optical conveyor belt can be realized by the interference of a diffracted beam from the integrated apodized grating and a free-space Gaussian beam, which intersects with

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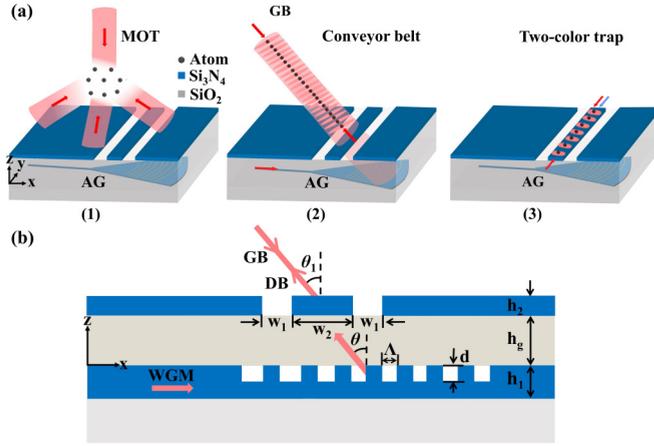


FIG. 1. (a) Flow chart of the operation procedure for the hybrid-photonic-atom-chip architecture: (1) the preparation of a cold-atom ensemble via a MOT, (2) the transportation of atoms from free space to the chip, and (3) the trapping and conveying of single atoms by the on-chip waveguides. (b) The cross-sectional geometry of the atom pipeline. GB: Gaussian beam, AG: apodized grating, WGM: waveguide mode, DB: diffraction beam.

a waveguide-based on-chip optical conveyor belt. By utilizing the antireflection property of the Brewster angle, the reflection of the free-space dipole laser on the waveguide surface is efficiently suppressed, allowing for continuous atom delivery from the free space to the integrated waveguide surface with a distance of around 100 nm. This pipeline provides a potential solution for reliable and efficient single-atom sources on the chip, which is essential for future atom-based quantum optics devices.

This paper is organized as follows. Section II provides an overview of the operation procedure for the hybrid-photonic-atom-chip architecture. Section III covers the structure design of the atom pipeline and the impact of reflection. In Sec. IV, the reflection on the dielectric surface is analyzed, and it can be suppressed by the Brewster angle. Finally, Sec. V demonstrates the performance of the atom pipeline with antireflection based on the Brewster angle.

II. OVERVIEW

Figure 1 sketches the two-layer chip architecture to realize free-space-to-chip atom transportation. On the top layer, photonic structures are fabricated with vacuum cladding, so cold atoms can be transported and trapped on top of them. As demonstrated in previous works [41–44], the blue- and red-detuned lasers in the waveguide can create a dipole trap using evanescent fields with a trap depth of ~ 1 mK. The integrated waveguides and microring resonators not only enable the manipulation of individual atoms through the trap potential but also enhance the photon-atom interaction due to the strongly confined optical fields on the chip. Therefore, there is potential to realize hybrid photonic-atomic quantum circuits [24–28]. The bottom layer of the chip provides the essential optical components responsible for converting the guided laser light in the waveguide into free-space beams.

Additionally, it facilitates the preparation and transportation of cold atoms to the top layer.

This architecture operates as follows:

(i) A cold-atom cloud with a distance of around 0.1–1 mm above the chip is prepared, as illustrated in Fig. 1(a), panel 1. In most cold-atom experiments, a cold-atom ensemble can be efficiently prepared by a standard MOT [45]. By employing a photonic chip with transparent substrates [27], we can achieve a conventional six-beam MOT configuration, with the MOT center positioned close to the chip surface [12,46]. Moreover, MOTs can be realized using on-chip optical devices. For instance, using gratings, bottom-layer photonic circuits can generate three cooling laser beams. Then, the MOT can be achieved by introducing an additional off-chip free-space cooling laser and a printed circuit for the magnetic field gradient [29–31].

(ii) An optical conveyor belt is used to transport cold atoms to the chip surface. An apodized grating on the bottom layer can generate a focusing Gaussian laser beam. The waveguide mode on the bottom layer is diffracted from the apodized grating, resulting in an output beam with a diffraction angle θ in the substrate and a refraction angle θ_1 in the air at wavelength λ , as shown in Fig. 1(a), panel 2. In the opposite direction, a Gaussian beam with the same wavelength λ propagates and interferes with the diffraction beam, forming an optical lattice above the chip. This lattice enables the transport of atoms using the atomic conveyor-belt technique [47]. By intersecting the free-space standing-wave conveyor belt with the on-chip evanescent-field-based conveyor belt [48], atoms can be transported between the two dipole traps [49], thus realizing an atom pipeline.

(iii) Single atoms are trapped and guided using the top-layer waveguide structures, as depicted in Fig. 1(a), panel 3. When the trapped atoms approach the chip surface (top layer) at a distance of about 100 nm, the van der Waals (vdW) force increases drastically [50]. This force causes the atoms to adhere to the chip surface, preventing them from further manipulation on the chip. Both the blue-detuned TM mode and the red-detuned TE mode are excited in the waveguide. The evanescent field of the blue-detuned TM mode generates a repulsive force that overcomes the vdW force, thereby preventing the atom from attaching to the chip surface. Conversely, the evanescent field of the red-detuned TE mode exerts an attractive force on the atom. The combination of the evanescent field of the waveguide modes and the vdW potential creates an optical trap well, with its center located approximately 100 nm from the waveguide surface [16,24,27,48].

The above procedure provides a potential method for transporting atoms from the MOT to the integrated photonic structures. However, as mentioned above, due to the potential diffraction and reflection of optical lasers around the surface, it is very challenging to realize seamless conversion between the optical conveyor belt and the on-chip evanescent-field traps. In this work, we focus on addressing this issue and present a practical solution of atom pipeline for connecting the free space and the chip. As an example, we consider ^{87}Rb atoms, which have a transition wavelength of 780 nm for the D_2 line. For the optical conveyor belt, we utilize a red-detuned laser with a wavelength of 850 nm to form a standing-wave

optical trap. For the evanescent-field trap, we employ the blue-detuned TM mode with a wavelength of $\lambda_b = 760$ nm and the red-detuned TE mode with a wavelength of $\lambda_r = 852$ nm to propagate unidirectionally and bidirectionally in the waveguide, respectively.

III. STRUCTURE DESIGN FOR THE PIPELINE

The detailed design parameters for realizing the pipeline are illustrated in Fig. 1(b). The chip architecture employs Si_3N_4 for the two layers of photonic structures, with thicknesses $h_1 = 300$ nm and $h_2 = 240$ nm. Notably, we utilize the $\lambda/4$ condition as the antireflection condition for the 850-nm laser in the top Si_3N_4 layer. The thickness of the top Si_3N_4 layer for antireflection is optimized through numerical simulations, as the optical path length of light in the Si_3N_4 layer depends on the incident angle. The bottom layer is buried in SiO_2 , with a distance of $h_g = 5$ μm from the top layer.

The apodized grating is etched on a tapered waveguide with a taper angle of 50° , and the apex of the taper upper surface serves as the origin of the coordinate system. The etching depth d of the grating is set to 200 nm. The length of the grating part is about 8 μm , and the width of the input waveguide is 0.55 μm . More details about the design of the apodized grating can be found in Ref. [14]. The diffraction angle of the apodized grating is related to the grating period Λ . To form a Gaussian-like beam, the grating period Λ of the apodized grating gradually changes from 365 to 332 nm, while the duty cycle η increases from 0.5 to 0.3 along the grating.

On the top layer, a waveguide intersects with the output Gaussian-like beam to transport the atoms from the optical conveyor belt to the waveguide evanescent-field trap. In order to suppress the diffraction of the free-space beam, the top layer of Si_3N_4 is nearly uniform, with only two grooves (width w_1) etched out to form a waveguide (width w_2) in the center.

We used the three-dimensional finite-difference time-domain method to simulate the electromagnetic field distribution and investigate the performance of the pipeline, as shown in Fig. 2. To analyze the effect of the reflection on the chip surface, a simplified model without etched grooves on the top Si_3N_4 layer is considered first. A TE Gaussian beam with a waist diameter of 3 μm is incident on the chip surface at an angle of 51.525° (not the Brewster angle). To form the standing-wave fields for the optical conveyor belt, a counterpropagating beam from the apodized grating on the bottom layer is generated at the same time. The intensity distributions of the Gaussian beam and the diffraction beam on the x - z plane above the chip are shown in Figs. 2(a) and 2(b), respectively. Although the antireflection condition of the waveguide thickness is used in our design to suppress the reflection, we can still find non-negligible reflection of optical fields, which induces the interference field distribution close to the surface of the chip. As shown in the insets of Figs. 2(a) and 2(b), the field distributions of both beams have similar Gaussian-like beam profiles. When the laser is input from both free space and the bottom layer, the interference of the beams gives rise to the standing-wave optical lattice, as shown in Fig. 2(c). The antinodes of the standing wave are labeled

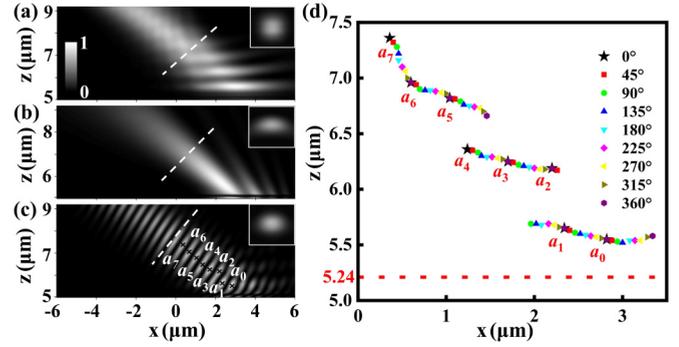


FIG. 2. The intensity distributions of the optical field on the x - z plane above the platform without etching grooves. (a) The intensity distribution of the Gaussian beam. (b) The intensity distribution of the diffraction beam from the integrated apodized grating. (c) The intensity distribution of the optical lattice. The insets in (a), (b), and (c) are the intensity distributions on the cross section denoted by the dotted lines. (d) The antinode position of the standing wave for different incident phase differences $\Delta\varphi$.

$a_0, a_1, a_2, \dots, a_i$, with the location becoming farther away from the chip surface as index i increases.

The red-detuned optical lattice can trap cold ^{87}Rb atoms at the antinodes. Consequently, by controlling the phase difference $\Delta\varphi$ between the two inputs for the Gaussian beam and the diffraction beam, we anticipate that the atoms trapped in the antinodes can move toward the chip [12,47,49]. In practical experiments, the two inputs are generated from the same laser, with phase control achieved using an acousto-optics modulator and a radio-frequency signal generator [46]. Figure 2(d) displays the progression of the antinode locations from a_0 to a_7 with varying $\Delta\varphi$, and the stars are the reference points that represent the positions of a_i when $\Delta\varphi$ is set to zero. By adjusting the phase difference $\Delta\varphi$ by 2π , the trapped atoms at star location a_i can be transported to the adjacent star location a_{i-1} . Thus, atoms in the optical lattice can be continuously transported to a_0 to realize a desired atom pipeline. However, we found that the traces of the antinodes are not continuous and are separated into three sections. As a result, atoms initially located at a_7 in the free-space optical lattice could be transported to only a minimum height of about 1.5 μm above the chip, and the transportation from a_3 to a_0 was impeded. The observed discontinuity in the antinode traces can be attributed to the formation of an additional standing wave caused by the reflection of the Gaussian beam on the top layer [Fig. 2(a)], preventing the transport of atoms toward the chip surface.

IV. THE SUPPRESSION OF REFLECTION

The results presented above confirm that the application of optical conveyor belts in the hybrid photonic-atom chip is limited to a distance of about 1 μm because there is considerable reflection of laser power even when the top-layer thickness meets the antireflection condition. To circumvent this issue, we propose using the Brewster angle to further suppress reflection. In this approach, a TM-polarized Gaussian beam is incident on the chip surface at an input angle θ_1 equal to the

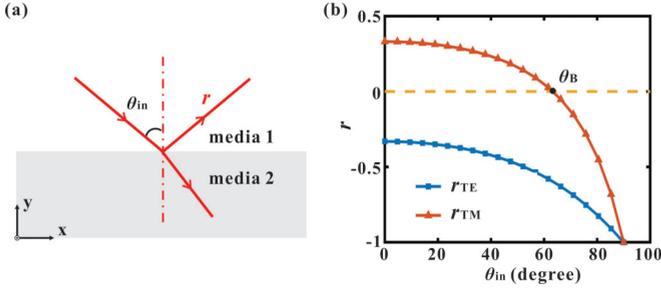


FIG. 3. The reflection and refraction of light at the interface of two media. (a) Illustration of light on the interface. (b) The reflection coefficients of TM- and TE-polarized light at 850 nm vary as a function of the incident angle θ_{in} on the air-to-Si₃N₄ interface.

Brewster angle of the top layer. As shown in Fig. 3(a), the reflection coefficients of optical fields on a flat surface for two polarizations follow [51]

$$r_{TM} = \frac{n_1 \cos \theta_{in} - \sqrt{n_2^2 - n_1^2 \sin^2 \theta_{in}}}{n_1 \cos \theta_{in} + \sqrt{n_2^2 - n_1^2 \sin^2 \theta_{in}}}, \quad (1)$$

$$r_{TE} = \frac{n_2 \cos \theta_{in} - \sqrt{n_1^2 - n_1^4 \sin^2 \theta_{in} / n_2^2}}{n_2 \cos \theta_{in} + \sqrt{n_1^2 - n_1^4 \sin^2 \theta_{in} / n_2^2}}, \quad (2)$$

where n_1 and n_2 are the refractive indices of media 1 and media 2, respectively. For our specific case, where light with a wavelength of 850 nm is incident from air ($n_1 = 1$) to Si₃N₄ ($n_2 = 1.999$) [52], the reflectivities r_{TM} and r_{TE} as a function of the incident angle θ_{in} are shown by the red line with triangles and the blue line with squares in Fig. 3(b), respectively. We find that at the Brewster angle $\theta_B = 63.4^\circ$, the reflection coefficient r_{TM} vanishes, resulting in a significantly suppressed reflection.

According to Eq. (1), the reflection of the TM-polarized Gaussian beam vanishes when incident on the chip surface at the Brewster angle θ_B . Compared with Fig. 2(a), the reflection of the Gaussian beam on the chip surface shown in Fig. 4(a) is suppressed in both the near field and the far field. The diffracted TM-polarized beam is output from the top layer at the same Brewster angle θ_B , when the TM mode is incident on the apodized grating with grating periods Λ ranging from 365 to 332 nm. The intensity distribution of the diffraction beam on the x - z plane is shown in Fig. 4(b), with the inset showing the intensity distribution on the cross section, denoted by the white dashed line. The counterpropagating Gaussian beam and the diffracted beam interfere to form an optical lattice, as shown in Fig. 4(c). The relation between the antinode locations (a_0 to a_7) and the phase difference $\Delta\varphi$ is given in Fig. 4(d). In contrast to the discontinuous traces of antinodes, the proposed scheme employing the Brewster angle generates a continuous trace of antinodes towards the interface, where all the antinodes a_i with $\Delta\varphi = 2\pi$ move and connect to a_{i-1} with $\Delta\varphi = 0$. As a result, the trapped atoms can be transported from free space to very close to the chip surface. After the atoms are delivered to the chip surface, they can be trapped and further transported by the evanescent optical trap on the waveguide surface [32], and thus, the pipeline is realized.

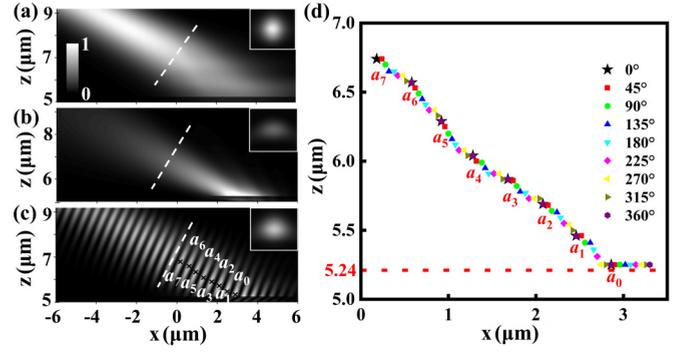


FIG. 4. The intensity distributions of the optical field on the x - z plane above the platform without etching grooves. (a) The intensity distribution of the Gaussian beam incident with the Brewster angle from free space. (b) The intensity distribution of the diffraction beam output with the Brewster angle from the integrated apodized grating. (c) The standing wave formed by the interference of the diffraction beam and the Gaussian beam. (d) The antinode position of the standing wave for different incident phase differences $\Delta\varphi$.

V. THE PERFORMANCE OF THE ATOM PIPELINE

In practice, waveguides must be fabricated to generate the on-chip evanescent-field atom trap potential. Two grooves should be etched on the top layer of the chip to create a waveguide that intersects with the optical lattice at a right angle. On the one hand, a small cross section of the waveguide is required to effectively enhance the electric-field intensity of the waveguide mode, thus reducing the required laser power for the evanescent-field trap. On the other hand, the scattering influence of the etched grooves on the optical trap laser should be minimized, which requires a wider waveguide and narrower etched grooves. Considering this trade-off relation, we have chosen $w_1 = 0.15 \mu\text{m}$ and $w_2 = 3 \mu\text{m}$ for the widths of the waveguide and etched grooves, respectively. Figure 5(a) illustrates the cross-section structure of the waveguide and the corresponding electric-field distribution of the TE and TM modes for red- and blue-detuned trap lasers. It shows confined modes in the waveguide region. Due to the leakage loss to the unetched slab with a finite groove width, the intensity of the waveguide mode will decay with propagation z as $\propto \exp(-z/L)$, where L represents the mode propagation length in the waveguide. Figure 5(b) numerically investigates the dependence of the propagation length on w_1 , and both modes exhibit propagation length $L > 1 \text{ mm}$. This indicates an energy loss of less than 1% in the waveguide with a length less than $10 \mu\text{m}$ for realizing the pipeline. In the area of the chip surface covered by the free-space dipole laser beam, which has a diameter of several micrometers, the widths of etched grooves around the waveguide are minimized to reduce diffraction loss. Simultaneously, the width of the waveguide is increased. The length of this narrow groove region is about $10 \mu\text{m}$ to minimize the leakage of waveguide modes into the slab. Outside the laser spot area, a tapered waveguide can be employed to narrow the waveguide, resulting in stronger coupling between the atom and the waveguide mode. Additionally, increasing the width of the groove can help reduce leakage loss. The different leakage losses between the TE and TM modes can be attributed to the distinct

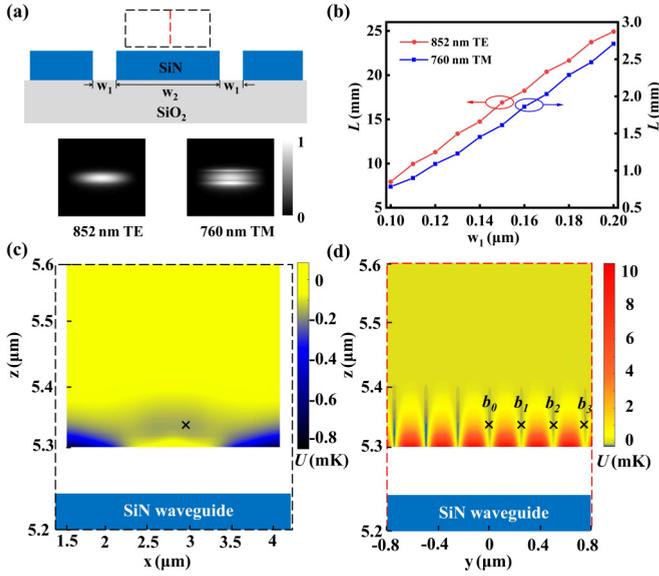


FIG. 5. The distribution of the optical trap depth. (a) The cross section of the waveguide and the optical field distributions of the TE and TM modes. (b) The propagation lengths of the waveguide modes vary with the gap width. Optical trap depth formed by the evanescent field of the waveguide modes and the vdW potential (c) on the x - z plane and (d) on the y - z plane, corresponding to the black dashed rectangle and the red line in (a).

electric-field boundary conditions for the two orthogonal optical polarizations.

The optical trap depth is analyzed in the following. By disregarding the Zeeman sublevels, we can estimate the optical dipole potential formed by linearly polarized light as [53]

$$U = \frac{\hbar\gamma I_0}{24I_S} \left(\frac{1}{\delta_{1/2}} + \frac{2}{\delta_{3/2}} \right). \quad (3)$$

Here, $\gamma/2\pi \approx 6.1$ MHz represents the natural linewidth of the ^{87}Rb D_2 transition, I_S denotes the saturation intensity, I_0 represents the intensity of the optical field, and $\delta_{1/2}$ and $\delta_{3/2}$ represent the detunings between the light frequency and the D_1 and D_2 transitions, respectively. These detuning are much larger than the hyperfine splitting of the excited state. For ^{87}Rb atoms with a resonant wavelength of about 780 nm, a red-detuned optical field (850 or 852 nm) generates an attractive gradient force, while a blue-detuned optical field (760 nm) produces a repulsive force. When calculating the optical dipole potential, we set the reference point at infinity with $U = 0$.

When the atom approaches the surface of the chip at a small distance, both the Casimir-Polder (CP) and vdW potentials are significant [50,54,55], attracting the atom to the surface. In pioneering studies on the near-field atom-surface interactions, the CP potential was theoretically investigated with Si_3N_4 [56]. In our case, the vdW force dominates because the distance between the trap center and the surface is much less than a wavelength. On the surface of the Si_3N_4 waveguide, the vdW potential of the ^{87}Rb atom can be estimated as $U_{\text{vdW}} = -0.12\hbar\gamma\lambda^3/8\pi^3d^3$, where d represents the distance from the surface [50,57]. The combination of the two-color evanescent field of the waveguide modes and the

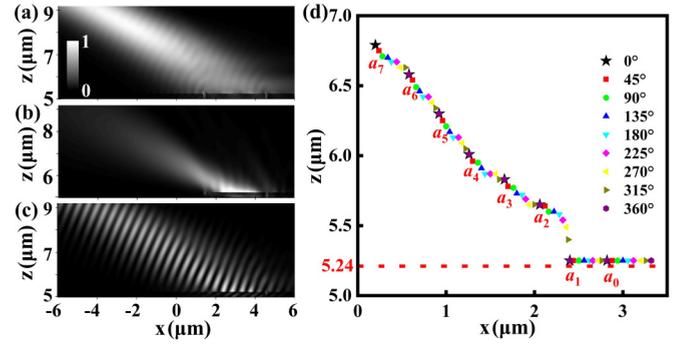


FIG. 6. The free-space optical conveyor belt formed by the platform with etching grooves. (a)–(c) The intensity distributions of the optical potential in the x - z plane. (d) The antinode positions against the phase differences $\Delta\phi$.

vdW potential results in an optical trap well above the surface of the waveguide. Figures 5(c) and 5(d) show the optical trap depths on the x - z plane and x - y plane above the waveguide surface, corresponding to the black dashed rectangle and the red dashed line in Fig. 5(a), respectively, where the powers of the blue- and red-detuned modes are 100 and 77.7 mW, respectively. The optical trap depth is about 0.162 mK, with trap centers about 100 nm away from the waveguide surface, as shown in Fig. 5(c). It is worth noting that the vdW potential is estimated by approximating the Si_3N_4 layer as an infinitely large uniform film, and the potential edge effect of the grooves is neglected since the atoms are trapped in a region away from the edge by about $1.5 \mu\text{m}$. A lattice of the trap well denoted as b_0, b_1, \dots, b_i along the waveguide is generated, as shown in Fig. 5(d). By manipulating the phase difference $\Delta\phi$ of the bidirectionally input red-detuned TE modes, the trap wells will move along the waveguide, which will transport the trapped atom to other positions on the chip. As a trade-off for the reduced perturbations of the waveguide structure to the free-space beams, the relatively wide waveguide requires a higher laser power for the near-field optical dipole trap. A high power up to 10 W was experimentally demonstrated for a waveguide mode on optical chips [58], making it realistic for the laser power required in our designed waveguide. Although the tightly confined optical modes in the waveguide can induce the out-of-phase longitudinal polarization component, which may have an impact on the potential of the atoms trapped in the evanescent field of a waveguide [59,60], this impact on the potential is left for future study since this paper mainly focuses on the transport of atoms from free space to the chip surface.

The intensity distributions of the free-space conveyor belt, with etched grooves, are depicted in Figs. 6(a)–6(c). Compared with Figs. 4(a)–4(c), the scattering from the grooves induces a minor perturbation on the optical lattice's intensity distribution, resulting in a significant drop in the antinode position close to a_1 . When the atom approaches the waveguide surface within hundreds of nanometers, the blue-detuned evanescent optical field of the waveguide modes can be employed to prevent the atom from attaching to the chip surface and to ensure a separation between the trap center and the surface of about 100 nm for efficient atom-waveguide coupling.

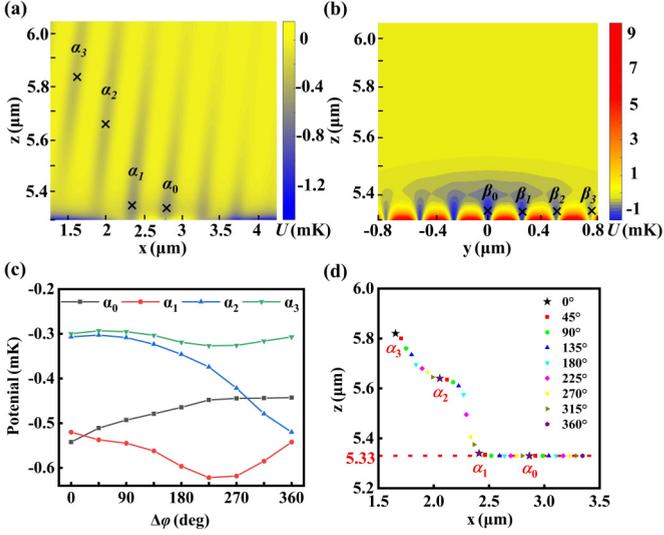


FIG. 7. The distribution of the total optical trap depth. (a) The total optical trap potential distribution on the x - z plane. (b) The total optical trap depth potential distribution in the x - y plane. (c) The effective optical trap depths of trap wells α_0 to α_3 as a function of the phase difference $\Delta\phi$. (d) The positions of the trap centers against the phase difference $\Delta\phi$.

Therefore, the sharp drop caused by the etched grooves does not hinder atom delivery from the free space to the near field of the waveguide surface.

Last, when the atom pipeline is implemented, the optical trap potential at the intersection is a superposition of potentials from the waveguide modes, the free-space standing wave, and the vdW potential. The distributions of the total optical trap potential in the intersection region with $\Delta\phi = 0$ and $\Delta\phi = 0$ for both free-space and on-chip optical fields on the x - z plane are shown in Fig. 7(a), and those on the x - y plane are shown in Fig. 7(b). The powers of the Gaussian beam and the propagating waveguide mode are 1.69 and 100 mW, respectively. The locations of trap wells are denoted by α_i ($i \in 0, 1, 2, \dots$) along the free-space standing wave and by β_i ($i \in 0, \pm 1, \pm 2, \dots$) along the waveguide. When the phase difference $\Delta\phi$ of the free-space standing wave is manipulated, the trap wells move, and the effective trap depths vary. For example, Fig. 7(c) shows the results for α_0 to α_3 with the optical fields in the waveguide fixed ($\Delta\phi = 0$). To ensure a stable atom trap during atom delivery, trap depths deeper than 0.3 mK are maintained. The trap centers of the wells vary with the phase difference $\Delta\phi$, demonstrating continuous movement between the adjacent trap wells. Near the waveguide surface, trap well α_0 is connected to trap well β_0 . The position of trap well β_0 will move horizontally to the adjacent trap well with the manipulation of the phase difference $\Delta\phi$ of the two red-detuned TM modes, which transports the atoms along the waveguide surface. In practice, manipulating atoms in the vicinity of the chip would be very challenging. In particular, the vibrations of the solid substrates and the charge fluctuations on the surface might heat atoms [61], and thus, the lifetime of atoms in the dipole trap may be short. In this study, we present only a simple scheme for atom transport on the waveguide, while a more detailed study of the near-field

dipole trap will be carried out in future work. While the analysis above considers only an atom delivery distance of several micrometers above the chip surface, it is also possible to achieve atom delivery farther away from the chip surface, where a stable standing wave can be established without the influence of reflections. Thus, a continuous free-space-to-chip pipeline for single atoms is realized on the integrated chip.

VI. CONCLUSION

A two-layer photonic chip architecture was proposed for the realization of a compact hybrid photonic-atom chip. In particular, a key ingredient of the architecture for realizing the efficient transport of cold atoms from the free-space MOT to the integrated waveguide evanescent-field trap was proposed and numerically validated. A free-space optical conveyor belt is formed by the interference of an on-chip diffracted laser beam and a free-space Gaussian beam. However, the diffraction and reflection of the dipole laser on the chip surface limit the transportation of atoms to a distance of about one wavelength above the chip surface. To address this issue, a free-space-to-chip pipeline for the smooth delivery of single atoms was proposed by employing the Brewster angle, which enables the elimination of dipole laser reflection on the surface of the chip. This continuous delivery of cold atoms from free space to the chip surface within a distance of less than 100 nm enables efficient interaction between the atoms and the evanescent field of the guided mode in the waveguides. Therefore, our proposal provides a reliable atom source for constructing on-chip hybrid atom-photonic devices, including single-photon sources, high-fidelity single-photon quantum gates, and quantum memories. Furthermore, this platform promises a different type of integrated circuit for matter waves of single atoms [62].

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