Characterization, synthesis, and optimization of quantum circuits over multiple-control *Z*-rotation gates: A systematic study

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We conduct a systematic study of quantum circuits composed of multiple-control *Z*-rotation (MCZR) gates as primitives, since they are widely used components in quantum algorithms and also have attracted much experimental interest in recent years. We establish a circuit-polynomial correspondence to characterize the functionality of quantum circuits over the MCZR gate set with continuous parameters. An analytic method for exactly synthesizing such quantum circuit to implement any given diagonal unitary matrix with an optimal gate count is proposed, which also enables the circuit depth optimal for specific cases with pairs of complementary gates. Furthermore, we present a gate-exchange strategy together with a flexible iterative algorithm for effectively optimizing the depth of any MCZR circuit, which can also be applied to quantum circuits over any other commuting gate set. Besides the theoretical investigation, the practical performance of our circuit synthesis and optimization techniques is further evaluated numerically on two typical examples in quantum computing, including diagonal Hermitian operators and quantum approximate optimization algorithm circuits with tens of qubits, which can demonstrate a reduction in circuit depth by 33.40% and 15.55% on average over relevant prior works, respectively. Therefore, our methods and results provide a pathway for implementing quantum circuits and algorithms on recently developed devices.

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I. INTRODUCTION

With the arrival of the noisy intermediate-scale quantum era [1], the synthesis and optimization of quantum gate circuits have become crucial steps towards harnessing the power of quantum computing on realistic devices [2,3]. While single-qubit rotation and two-qubit controlled-NOT gates have been subjects of long-term investigations as they constitute an elementary gate set capable of universal quantum computation [4,5], the multiple-control rotation (MCR) gates defined to act on more qubits have also attracted a great deal of interest in terms of both fundamental and practical aspects.

(i) Theoretically, MCR operations often serve as important components in many quantum algorithms or quantum computing models such as preparing quantum hypergraph states [6,7], building a circuit-based quantum random access memory [8,9], participating in Shor's factoring algorithm [10] and different types of quantum search algorithms [11–13], the quantum walk [14], and fault-tolerant quantum computation [15,16]. Therefore, a good understanding of MCR circuits can facilitate the design and analysis of new quantum information processing schemes. In fact, MCR gates have been included as basic building blocks in some popular quantum computing software frameworks such as Qiskit [17] and PennyLane [18].

(ii) Instead of performing concatenated single- and two-qubit gates in conventional experiments [11,19,20], recent experimental progress has also been made in direct implementations of MCR gates in a variety of physical systems, including ion traps [21], neutral atoms [22,23], linear and nonlinear quantum optics [24–26], and superconducting circuit systems [27–29]. In particular, MCR gates have been used as native quantum gates in practical experiments for demonstrating quantum algorithms [30,31] and quantum error correction [32]. Therefore, quantum circuits over suitable MCR gates for benchmarking and exploiting these ongoing quantum hardware need to be specifically considered.

Several notable works have investigated quantum circuit models at the level of MCR gates with various techniques and results. For example, discussions about the use of multiple-control Toffoli gates as basic building blocks in circuit synthesis were presented early on, including the use of Reed-Muller spectra [33], Boolean satisfiability techniques [34], and NCV-$|v_1\rangle$ libraries [35]. Typically, the issue of decomposing diagonal Hermitian quantum gates into a set consisting of solely multiple-controlled Pauli Z operators had been studied [36] by introducing a binary representation of these gates. Subsequently, different circuit identities that can replace certain configurations of the multiple-control Toffoli gates with their simpler multiple-control relative-phase implementations were reported [37], showing the optimized resource counts. Given these promising results, quantum circuits based on a wider range of multiple-control quantum gates and their applications are worthy of more in-depth exploration as well.

In this paper we develop a systematic characterization, synthesis, and optimization of quantum circuits over multiple-control Z-rotation (MCZR) gates with continuous parameters, each of which would apply a Z-axis rotation gate $R_Z(\theta) = \mathrm{diag}\{1, e^{i\theta}\}$ with a real-valued θ to the target qubit only when all its control qubits are set to 1. In fact, such quantum gates

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play a prominent role in quantum state generation [6,38–40], quantum circuit construction [41–43], and fault-tolerant quantum computation [15,16]. Accordingly, schemes aimed at realizing fast and high-fidelity special or general MCZR gates are constantly being proposed [44–49] as well as experimentally demonstrated [22,23,28,30–32] in recent years. One-step implementation of the two-qubit controlled-Z (CZ), three-qubit CCZ, and four-qubit CCCZ gates has been realized with experimental fidelities of about 0.94, 0.868, and 0.817, respectively, based on the continuous-variable geometric phase in a superconducting circuit [28]. Then a multimode superconducting processor circuit with all-to-all connectivity that can implement the near-perfect generalized CCZ(θ) gates with an arbitrary angle θ as the native three-qubit controlled operations was presented [30] and a three-qubit Grover search algorithm and the quantum Fourier transform were demonstrated experimentally. Hence, how to perform quantum computing tasks over such gates with a low gate count and circuit depth is of practical significance, motivating us to conduct a systematic study in this work. For a general consideration, the number of control qubits, the set of acting qubits, and the angle parameters θ of MCZR gates are all unrestricted in our discussion.

The rest of this paper is organized as follows. In Sec. II we put forward a convenient polynomial representation to describe the functionality of the MCZR circuits, indicating that any realizable unitary matrix must be a diagonal one. In Sec. III we analytically derive a circuit synthesis method that can provide an optimal gate count for implementing any given diagonal unitary matrix, which also achieves an optimal circuit depth for cases consisting of well-defined pairs of complementary gates. In Sec. IV we consider how to reduce the circuit depth of any given MCZR circuit by proposing a gate-exchange strategy together with a flexible iterative depth-optimization algorithm, which can yield better optimization results at the cost of more execution time. In Sec. V we validate the performance of our synthesis and depth-optimization methods for MCZR circuits by numerical evaluations on two typical examples, including the diagonal Hermitian quantum operators and quantum approximate optimization algorithm (QAOA) circuits, both of which show improvements over previous results. For the former, our constructed circuits on average can achieve a 33.40% depth reduction over the prior work [36] for the circuit size $n \in [2, 12]$. For the latter, our optimized circuit depth ranges from 3.00 to 4.05 for $n \in [6, 50]$ and on average can reduce the circuit depth up to 58.88% over randomly selected circuits and 15.55% over the results from Ref. [50], respectively. Notably, here we achieve a nearly constant depth for moderate-size QAOA circuits on 3-regular graphs. We expect the methods and results of this paper to be beneficial to the study of implementing quantum circuits and algorithms on specific quantum systems, and several directions for future work are discussed in Sec. VI.

II. CHARACTERIZATION OF MCZR CIRCUITS

To characterize the functionality of the MCZR circuit, we first establish a useful circuit-polynomial correspondence and then illustrate its unitary matrix representation. For convenience, here we introduce some of the notation used throughout this paper.

A. Notation

We denote the set $\{a, a+1, a+2, \ldots, b\}$ by $[a, b]$ with a and b integers and $a \leqslant b$. When $a = 1$, the denotation $[a, b]$ is simplified to $[b]$. For a binary number x, we use $q(x)$ to represent its corresponding decimal number. The symbols $\|v\|$ and $|A|$ indicate the Hamming weight of a binary string v (i.e., the number of 1's in v) and the size of the set S (i.e., the number of its elements), respectively. For an n-bit string $v = v_1 v_2 \cdots v_n$, we denote the set of positions of all 1 bits by $P_v = \{p_1, p_2, \ldots, p_{\|v\|}\}$ such that $v_{p_1} = v_{p_2} = \cdots = v_{p_{\|v\|}} = 1$. We use $I_{m\times n}$ to denote the size $m \times n$ identity matrix and the symbol $\circ$ is used to concatenate m ($m \geqslant 2$) subcircuits $\{C_1, C_2, \ldots, C_m\}$ to form a circuit C such that $C = C_1 \circ C_2 \circ \cdots \circ C_m$.

B. Circuit characterization

The MCZR gate family for an n-qubit quantum circuit can be denoted by $\{C^{(k)}Z(\theta_{c,t}) : c \subset [n], t \in [n], k = |c|\}$, with c the control set, t the target, and $\theta_{c,t}$ a Z-rotation angle parameter. By definition, the action of an MCZR gate on each computational basis state is

$$C^{(k)}Z(\theta_{c,t}) : |x_1, x_2, \ldots, x_n\rangle \mapsto \exp\left(i\theta_{c,t} x_t \prod_{j\in c} x_j\right)|x_1, x_2, \ldots, x_n\rangle. \tag{1}$$

The global phase factor in Eq. (1) indicates that the function of gate $C^{(k)}Z(\theta_{c,t})$ remains unchanged under any permutation of k control and one target qubits in the set $\gamma = c \bigcup t$. Therefore, we can simply denote each MCZR gate acting on all qubits in a set $\gamma \subseteq [n]$ as $G(\gamma, \theta_\gamma)$ such that

$$G(\gamma, \theta_\gamma) : |x_1, x_2, \ldots, x_n\rangle \mapsto \exp\left(i\theta_\gamma \prod_{j\in\gamma} x_j\right)|x_1, x_2, \ldots, x_n\rangle. \tag{2}$$

In this way, any quantum circuit C consisting of m MCZR gates $G(\gamma_1, \theta_{\gamma_1})$, $G(\gamma_2, \theta_{\gamma_2})$, …, $G(\gamma_m, \theta_{\gamma_m})$ can transform each basis state as

$$C : |x_1, x_2, \ldots, x_n\rangle \mapsto \exp[ip(x_1, x_2, \ldots, x_n)]|x_1, x_2, \ldots, x_n\rangle, \tag{3}$$

with

$$p(x_1, x_2, \ldots, x_n) = \sum_{k=1}^{m} \theta_{\gamma_k}\left(\prod_{j\in\gamma_k} x_j\right) \tag{4}$$

a phase polynomial associated with the circuit C. In other words, any given n-qubit MCZR circuit C corresponds to a unique phase polynomial with real coefficients and degree at most n.

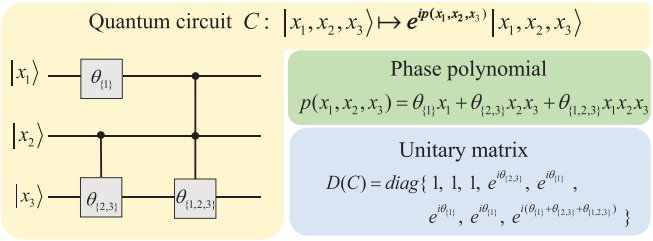


FIG. 1. Three-qubit circuit C consisting of three MCZR gates with angle parameters $\theta_{\{1\}}$, $\theta_{\{2,3\}}$, and $\theta_{\{1,2,3\}}$, respectively, which can add a phase factor $e^{ip(x_1,x_2,x_3)}$ to the basis state $|x_1,x_2,x_3\rangle$ with a phase polynomial $p(x_1,x_2,x_3)=\theta_{\{1\}}x_1+\theta_{\{2,3\}}x_2x_3+\theta_{\{1,2,3\}}x_1x_2x_3$. The unitary matrix represented by C is a diagonal one as $D(C)=\mathrm{diag}\{1,1,1,e^{i\theta_{\{2,3\}}},e^{i\theta_{\{1\}}},e^{i\theta_{\{1\}}},e^{i\theta_{\{1\}}},e^{i(\theta_{\{1\}}+\theta_{\{2,3\}}+\theta_{\{1,2,3\}})}\}$.

Now we turn to the unitary matrix representation of n-qubit MCZR circuits. Equation (2) reveals that each MCZR gate can be explicitly expressed as a diagonal unitary matrix of size $2^n\times 2^n$ as

$$G(\gamma,\theta_\gamma)=\sum_{x\in\{0,1\}^n}\exp\left(i\theta_\gamma\prod_{j\in\gamma}x_j\right)|x\rangle\langle x|, \tag{5}$$

with all its diagonal elements being 1 or $e^{i\theta_\gamma}$. Since all MCZR gates are diagonal and commutative, two or more MCZR gates that act on the same set of qubits in a circuit can be merged into one by just adding their angle parameters. Without loss of generality, in this paper we focus on the nontrivial MCZR circuit C such that all the constituent m gates have a distinct qubit set γ_k $(k=1,2,\ldots,m)$ and its unique phase polynomial in Eq. (4) exactly has degree $\max\{|\gamma_k|:k=1,2,\ldots,m\}$ and m terms with real coefficients being the angle parameters $\{\theta_{\gamma_k}:k=1,2,\ldots,m\}$. Accordingly, the circuit C in Eq. (3) would function as a diagonal unitary matrix as

$$D(C)=\sum_{x\in\{0,1\}^n}\exp[ip(x)]|x\rangle\langle x|, \tag{6}$$

with the polynomial $p(x=x_1,x_2,\ldots,x_n)$ defined in Eq. (4). Obviously, two MCZR circuits over different gate sets would implement two distinct diagonal unitary matrices. For clarity, we display an instance circuit with $n=3$ and its polynomial as well as unitary matrix representation in Fig. 1.

III. OPTIMAL SYNTHESIS OF MCZR CIRCUITS

In the preceding section we revealed that an MCZR circuit can implement a diagonal unitary matrix. This in turn raises a natural question: Can an arbitrary diagonal operator be implemented by an MCZR gate circuit exactly? This is an attractive subject since diagonal unitary matrices have a wide range of applications in quantum computing and quantum information [14,50–53].

In this section we address this issue by proposing a circuit synthesis method to construct an n-qubit gate-count-optimal MCZR circuit for implementing a size $N\times N$ $(N=2^n)$ diagonal unitary matrix

$$D(\vec{\alpha}=[\alpha_0,\alpha_1,\ldots,\alpha_{N-1}])=\begin{bmatrix}e^{i\alpha_0}&0&\cdots&0&0\\0&e^{i\alpha_1}&\cdots&0&0\\\vdots&\vdots&\ddots&\vdots&\vdots\\0&0&\cdots&0&e^{i\alpha_{N-1}}\end{bmatrix}$$
$$=\sum_{x\in\{0,1\}^n}\exp(i\alpha_{q(x)})|x\rangle\langle x|, \tag{7}$$

with $q(x)$ being the decimal number of x, which simultaneously enables the circuit depth optimal for specific cases. In particular, we emphasize that the optimality mentioned in this paper always indicates an exact optimal value for the gate count and circuit depth rather than asymptotically optimal results, indicating that our optimal results cannot be improved any more. For convenience, here we rewrite each available gate $G(\gamma,\theta_\gamma)$ in Eq. (2) as $G(v,\theta_v)$ by associating γ with an n-bit string $v=v_1v_2\cdots v_n\in\{0,1\}^n$ such that

$$v_j:=\begin{cases}1, & j\in\gamma\\0, & j\in[n]\backslash\gamma.\end{cases} \tag{8}$$

Our main results in this section are summarized in Theorems 1–3.

Theorem 1. The MCZR gate set $\{G(v,\theta_v)\}$ for implementing a target diagonal unitary matrix $D(\vec{\alpha})$ in Eq. (7) with 2^n given parameters $[\alpha_0,\alpha_1,\ldots,\alpha_{N-1}]$ is unique and each gate parameter can be computed analytically as

$$\theta_v=(-1)^{\|v\|}\sum_{x:P_x\subseteq P_v}(-1)^{\|x\|}\alpha_{q(x)},\quad v\in\{0,1\}^n, \tag{9}$$

with $q(x)$, P_v, P_x, $\|v\|$, and $\|x\|$ defined in Sec. II A. Since $\theta_v=0$ indicates a trivial identity gate that can be omitted, the optimal gate count for implementing $D(\vec{\alpha})$ is thus $|\{G(v,\theta_v\neq 0)\}|$ with θ_v from Eq. (9).

Proof. According to Eq. (8), there are totally 2^n-1 different types of gates $\{G(v,\theta_v):v\in\{0,1\}^n\backslash 00\cdots 0\}$ available to construct an MCZR circuit C that functions as Eq. (6), with its phase polynomial $p(x)$ in Eq. (4) rewritten as

$$p(x)=\sum_{v\in\{0,1\}^n\backslash 00\cdots 0}\theta_v\left(x_1^{v_1}x_2^{v_2}\cdots x_n^{v_n}\right). \tag{10}$$

Since two quantum circuits which differ only by a global phase factor are equivalent, we suppose that a circuit C described by Eq. (6) can perform the target diagonal matrix $D(\vec{\alpha})$ in Eq. (7) as

$$e^{i\theta_{00\cdots0}}\sum_{x\in\{0,1\}^n}\exp[ip(x)]|x\rangle\langle x|$$
$$=\sum_{x\in\{0,1\}^n}\exp(i\alpha_{q(x)})|x\rangle\langle x|, \tag{11}$$

leading to

$$\theta_{00\cdots0}+p(x)=\alpha_{q(x)},\quad x\in\{0,1\}^n, \tag{12}$$

with $\theta_{00\cdots0}$ a global phase factor, $p(x)$ defined in Eq. (10), and $q(x)$ defined in Sec. II A. In total, Eq. (12) gives us 2^n linear

equations

$$\begin{aligned}
&x = 00\cdots00 : \theta_{00\cdots00} = \alpha_0,\\
&x = 00\cdots01 : \theta_{00\cdots00} + \theta_{00\cdots01} = \alpha_1,\\
&x = 00\cdots10 : \theta_{00\cdots00} + \theta_{00\cdots10} = \alpha_2,\\
&x = 00\cdots11 : \theta_{00\cdots00} + \theta_{00\cdots01} + \theta_{00\cdots10} + \theta_{00\cdots11} = \alpha_3,\\
&\quad\vdots\\
&x = 11\cdots11 : \sum_{v\in\{0,1\}^n} \theta_v = \alpha_{N-1}.
\end{aligned} \tag{13}$$

Thus, if we can solve a set of 2^n angle parameters $\{\theta_v : v \in \{0,1\}^n\}$ satisfying Eq. (13) for any given $\vec{\alpha} = [\alpha_0, \alpha_1, \ldots, \alpha_{N-1}]$, then we obtain an MCZR circuit over the gate set $\{G(v,\theta_v)\}$ for implementing any $D(\vec{\alpha})$ in Eq. (7). In the following, we give an exact analytical expression of the solution to Eq. (13) and prove its uniqueness.

The linear equations (13) can be succinctly summarized into a standard form as

$$J\begin{pmatrix}\theta_{00\cdots00}\\ \theta_{00\cdots01}\\ \theta_{00\cdots10}\\ \theta_{00\cdots11}\\ \vdots\\ \theta_{11\cdots11}\end{pmatrix} = \begin{pmatrix}\alpha_0\\ \alpha_1\\ \alpha_2\\ \alpha_3\\ \vdots\\ \alpha_{N-1}\end{pmatrix} \tag{14}$$

such that the size $2^n \times 2^n$ coefficient matrix J has elements

$$J_{\tilde{q}(x),\tilde{q}(v)} = \begin{cases}1 & \text{for } P_v \subseteq P_x\\ 0 & \text{otherwise,}\end{cases} \tag{15}$$

where $x, v \in \{0,1\}^n$, the function $\tilde{q}(\cdot) = q(\cdot) + 1$ transforms a binary string into a decimal number as the row or column index of a matrix, and the set $P_{x\,(v)}$ about a string x (v) is defined in Sec. II A. Consider another size $2^n \times 2^n$ matrix denoted by K with elements

$$K_{\tilde{q}(v),\tilde{q}(x)} = \begin{cases}(-1)^{\|v\|+\|x\|} & \text{for } P_x \subseteq P_v\\ 0 & \text{otherwise,}\end{cases} \tag{16}$$

where $x, v \in \{0,1\}^n$. Here we can prove the product of two matrices in Eqs. (16) and (15) as $Q = K \times J$ is exactly an identity matrix of size $2^n \times 2^n$. By definition, the matrix elements of Q are

$$\begin{aligned}
Q_{\tilde{q}(v_1),\tilde{q}(v_2)} &= \sum_{x\in\{0,1\}^n} K_{\tilde{q}(v_1),\tilde{q}(x)} J_{\tilde{q}(x),\tilde{q}(v_2)}\\
&= (-1)^{\|v_1\|} \sum_{x:P_{v_2}\subseteq P_x\subseteq P_{v_1}} (-1)^{\|x\|} + 0,\\
&\quad v_1, v_2 \in \{0,1\}^n.
\end{aligned} \tag{17}$$

For the diagonal element of Q with $v_1 = v_2$ and $P_{v_1} = P_{v_2}$, Eq. (17) turns into

$$Q_{\tilde{q}(v_1),\tilde{q}(v_1)} = (-1)^{\|v_1\|}(-1)^{\|v_1\|} = 1, \quad v_1 \in \{0,1\}^n \tag{18}$$

by taking $x = v_1$. For the off-diagonal elements of Q with $v_1 \neq v_2$ and $P_{v_1} \neq P_{v_2}$, we have two cases.

(i) If $P_{v_2} \not\subset P_{v_1}$, then no string x can satisfy $P_{v_2} \subseteq P_x \subseteq P_{v_1}$, leading Eq. (17) to $Q_{\tilde{q}(v_1),\tilde{q}(v_2)} = 0$.

(ii) If $P_{v_2} \subset P_{v_1}$, then there are in total $2^{\|v_1\|-\|v_2\|}$ strings x that can satisfy $P_{v_2} \subseteq P_x \subseteq P_{v_1}$, wherein $\|x\|$ is even for exactly half of these x and odd for the other half, leading Eq. (17) to $Q_{\tilde{q}(v_1),\tilde{q}(v_2)} = 0$.

At this point, we prove that $K \times J = I_{2^n\times 2^n}$ and thus the square matrix K defined in Eq. (16) is the unique inverse matrix of the coefficient matrix J in Eq. (14) by the common knowledge of linear algebra. By multiplying both sides of Eq. (14) with K and using Eq. (16), we obtain an analytic form of the solutions $\{\theta_v\}$ to Eq. (14) as

$$\begin{aligned}
\theta_v &= \sum_{x\in\{0,1\}^n} K_{\tilde{q}(v),\tilde{q}(x)}\alpha_{q(x)}\\
&= (-1)^{\|v\|} \sum_{x:P_x\subseteq P_v} (-1)^{\|x\|}\alpha_{q(x)}, \quad v \in \{0,1\}^n,
\end{aligned} \tag{19}$$

with $q(x)$, P_v, P_x, $\|v\|$, and $\|x\|$ defined in Sec. II A.

In summary, Eq. (19) represents a unique set of solutions so that the resultant MCZR circuit for implementing $D(\vec{\alpha})$ in Eq. (7) naturally achieves an optimal gate count. The angle parameter $\theta_v = 0$ indicates its associated MCZR gate $G(v,\theta_v)$ is a trivial identity gate that can be omitted. Therefore, the optimal gate count for realizing any diagonal unitary operator in Eq. (7) is $|\{G(v,\theta_v \neq 0)\}|$ with the gate parameters obtained from Eq. (19) and in the worst case is $2^n - 1$ when all angle parameters are solved to be nonzero. For clarity, an example with $n = 3$ is shown in Figs. 2(a) and 2(b). ■

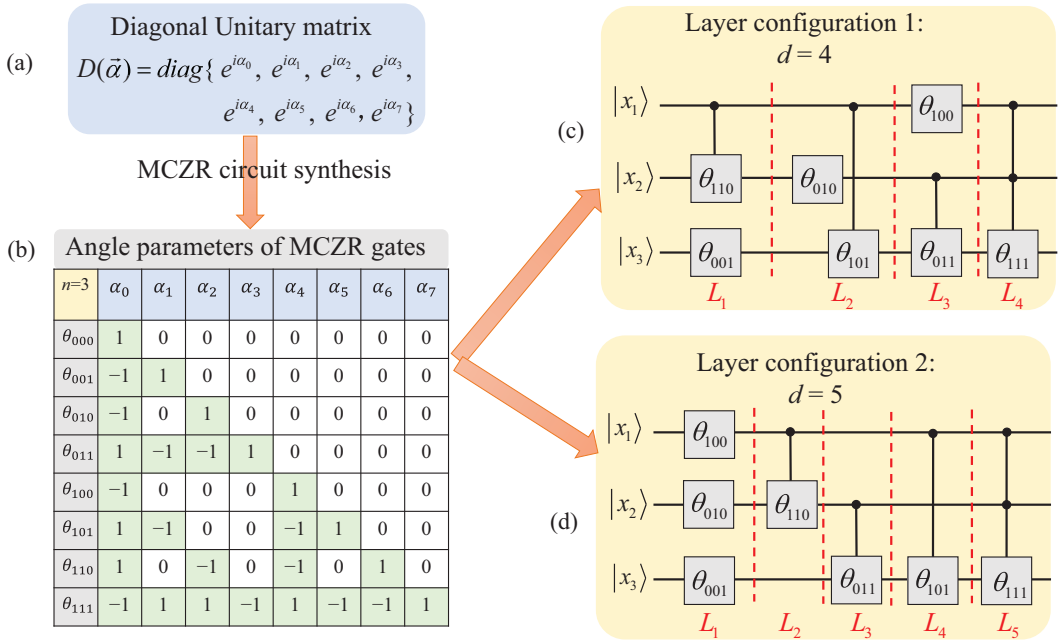
As a by-product, the uniqueness of the gate set $\{G(v,\theta_v)\}$ for implementing a diagonal unitary matrix as declared in Theorem 1 gives us Lemma 1.

Lemma 1. All MCZR gates in $\{G(v,\theta_v) : v \in \{0,1\}^n, \theta_v \in [0, 2\pi)\}$ are independent, that is, none of them can be decomposed into a combination of the others.

Besides the gate count, the circuit depth is another important circuit cost metric that needs attention, since a reduced depth means less circuit execution time and the mitigation of decoherence effect. A quantum circuit can be represented as a directed acyclic graph in which each node corresponds to a circuit's gate and each edge corresponds to the input or output of a gate. Then the circuit depth d is defined as the maximum length of a path flowing from an input of the circuit to an output [54]. In other words, d is the number of layers of quantum gates that compactly act on disjoint sets of qubits [55,56]. For example, the depth of the circuit in Fig. 1 with three nonzero angle parameters is $d = 2$. Note that a set of MCZR gates may form distinct layer configurations with respective circuit depths, as exemplified by the comparison between the depth-4 circuit in Fig. 2(c) and depth-5 circuit in Fig. 2(d). More generally, in Theorem 2 we reveal the optimal circuit depth of any MCZR circuit constructed from pairs of complementary gates as defined in Definition 1.

Definition 1. We call a pair of MCZR gates $G(v_1,\theta_{v_1})$ and $G(v_2,\theta_{v_2})$ complementary if and only if they satisfy $v_1 \oplus v_2 = 11\cdots11$.

Theorem 2. The optimal circuit depth of any MCZR circuit constructed from d_1 pairs of complementary gates is exactly d_1.



n=3	α_0	α_1	α_2	α_3	α_4	α_5	α_6	α_7
θ_{000}	1	0	0	0	0	0	0	0
θ_{001}	−1	1	0	0	0	0	0	0
θ_{010}	−1	0	1	0	0	0	0	0
θ_{011}	1	−1	−1	1	0	0	0	0
θ_{100}	−1	0	0	0	1	0	0	0
θ_{101}	1	−1	0	0	−1	1	0	0
θ_{110}	1	0	−1	0	−1	0	1	0
θ_{111}	−1	1	1	−1	1	−1	−1	1

FIG. 2. Example with $n = 3$ to show the gate-count-optimal synthesis of quantum MCZR circuits. To construct a circuit for realizing a given diagonal unitary matrix $D(\vec{\alpha})$ of size 8×8 in (a), we can first use Eq. (9) to solve the angle parameters $\{\theta_v : v \in \{0, 1\}^3\}$ of all employed MCZR gates as linear combinations of given $\{\alpha_0, \alpha_1, \ldots, \alpha_7\}$ with nonzero coefficients marked green shown in (b). Note that the angle parameter $\theta_v = 0$ indicates a trivial identity gate that can be removed in the circuit. Then these gates are arranged in different layers to give a circuit layer configuration. For a general case, we present a circuit consisting of all gates in complementary pairs with a depth $d = 4$ in (c), while another circuit with a depth $d = 5$ is depicted in (d) for comparison. As a summary, the circuit in (c) to implement (a) can be directly obtained by Theorem 3.

Proof. Suppose we construct an n-qubit MCZR circuit over d_1 pairs of complementary gates $\{G(v, \theta_v)\}$ by arranging them into d layers denoted by $\{L_1, L_2, \ldots, L_d\}$ such that all gates in each layer L_i $(i = 1, 2, \ldots, d)$ are disjoint. Here we prove that the minimum value of d is d_1.

For brevity, we denote each gate layer L_i by an n-bit string as

$$s(L_i) = \sum_{v:G(v,\theta_v)\in L_i} v, \quad i = 1, 2, \ldots, d, \tag{20}$$

and all d such strings have in total nd bits of 0 and 1. On the other hand, the total number of 1 bits in $2d_1$ strings v representing these gates is nd_1. Therefore, we have

$$nd \geqslant nd_1 \tag{21}$$

and the lower bound of the circuit depth is

$$d \geqslant d_1. \tag{22}$$

Obviously, the equality in Eq. (22) can be achieved when every gate layer L_i $(i = 1, 2, \ldots, d)$ has a pair of complementary gates, thus forming a circuit with an optimal depth d_1. ■

A typical application of Theorem 2 is to construct a depth-optimal MCZR circuit over all $2^n - 1$ nonzero gate parameters solved from Theorem 1 for implementing a given diagonal operator. Specifically, when all these gates are arranged into $(2^n - 2)/2 = 2^{n-1} - 1$ layers of complementary gates as $L_1 = [v = 00\cdots01, v = 11\cdots10]$, $L_2 = [v = 00\cdots10, v = 11\cdots01]$, …, $L_{2^{n-1}-1} = [v = 01\cdots11, v = 10\cdots00]$ plus a sole gate in $L_{2^{n-1}} = [v = 11\cdots11]$, a circuit with an optimal depth 2^{n-1} is obtained. For clarity, a circuit example with $n = 3$ and the optimal depth $d = 4$ is shown in Fig. 2(c), while another circuit with a larger depth $d = 5$ is shown in Fig. 2(d) for comparison.

Finally, the combination of Theorems 1 and 2 leads to a pairwise circuit synthesis method described as Theorem 3.

Theorem 3 (pairwise MCZR circuit synthesis). An MCZR circuit C over the gate set $\{G(v, \theta_v)\}$ for implementing an arbitrary diagonal unitary matrix $D(\vec{\alpha})$ in Eq. (7) can be synthesized by uniquely determining each gate parameter θ_v according to Eq. (9) in a pairwise way as $L_1 = [v = 00\cdots01, v = 11\cdots10]$, $L_2 = [v = 00\cdots10, v = 11\cdots01]$, …, $L_{2^{n-1}-1} = [v = 01\cdots11, v = 10\cdots00]$, $L_{2^{n-1}} = [v = 11\cdots11]$ such that $C = L_1 \circ L_2 \circ \cdots \circ L_{2^{n-1}}$. Note that $G(v, \theta_v = 0)$ is an identity gate that will not appear in C, and thus C has an optimal gate count $m_D = |\{G(v, \theta_v \neq 0)\}|$ for any $D(\vec{\alpha})$. Specifically, C has an optimal circuit depth when the implementation of $D(\vec{\alpha})$ only employs pairs of complementary gates. For example, this theorem gives us the circuit in Fig. 2(c) to implement Fig. 2(a).

In summary, we provide a gate-count-optimal circuit synthesis (that is, Theorem 3) to realize a given diagonal unitary matrix in Eq. (7), which also enables the optimal circuit depth when all obtained nonzero angle parameters correspond to pairs of complementary gates. Furthermore, in the following we consider how to optimize the depth of any other types of MCZR circuits.

IV. DEPTH OPTIMIZATION OF MCZR CIRCUITS

Since all MCZR gates are diagonal and commutative, the task of optimizing the depth of any given MCZR circuit is equivalent to rearranging all its gates into as few disjoint layers as possible. In this section we propose a gate-exchange strategy together with a flexible algorithm for effectively reducing the circuit depth.

A. Gate-exchange strategy for optimizing circuit depth

First of all, we present a simple but useful strategy in Lemma 2 that can reduce (or retain) the depth of any MCZR circuit.

Lemma 2. For a depth-d_1 MCZR circuit C_1 over the gate set $S = \{G(v, \theta_v)\}$, suppose that (a) a pair of complementary gates $G(v_1, \theta_{v_1})$ and $G(v_2, \theta_{v_2})$ are located in two different layers of C_1 and (b) the gate $G(v_1, \theta_{v_1})$ and a subset of gates $\{G(v', \theta_{v'})\} \subset S$ are located in the same layer of C_1. Then the exchange of $\{G(v', \theta_{v'})\}$ and $G(v_2, \theta_{v_2})$ in C_1 would arrange $G(v_1, \theta_{v_1})$ and $G(v_2, \theta_{v_2})$ into one layer, leading to a new depth-d_2 circuit C_2 with $d_2 \leqslant d_1$.

We give an intuitive explanation of Lemma 2. In the original depth-d_1 circuit C_1, suppose the gate $G(v_1, \theta_{v_1})$ and gates in $\{G(v', \theta_{v'})\}$ are located in a layer indexed by L_1, while the gate $G(v_2, \theta_{v_2})$ is located in another layer indexed L_2. Then the exchange of $G(v_2, \theta_{v_2})$ and $\{G(v', \theta_{v'})\}$ arranges the former and the latter into the layers L_1 and L_2, respectively. Since the gate $G(v_2, \theta_{v_2})$ alone acts on more qubits than any gate in $\{G(v', \theta_{v'})\}$ does, such a gate-exchange operation would lead to two possible situations about the resultant circuit C_2: (i) C_2 has the same depth d_1 as C_1 or (ii) some (or all) of the gates in $\{G(v', \theta_{v'})\}$ and the gates adjacent to layer L_2 can be merged into the same layer, thus causing a depth reduction over C_1.

Based on Lemma 2, we can derive a two-step framework for achieving a depth-optimal MCZR circuit as described in Lemma 3.

Lemma 3. In principle, the optimal circuit depth d_{opt} of the MCZR circuits constructed from a given gate set $S = \{G(v, \theta_v)\}$ with $|S| = m$ can be achieved by two steps: (a) Arrange all d_1 pairs of complementary gates in S into a depth-d_1 configuration and (b) find a depth-optimal circuit over the other $r = m - 2d_1$ gates. Then d_{opt} is equal to the total depth of these two parts.

A special case of Lemma 3 is Theorem 2 such that $m = 2d_1$ gives us $d_{\text{opt}} = d_1$. In general, we can accomplish the second step of Lemma 3 by comparing at most $r!$ different layer configurations and finding the depth-optimal circuit over a given gate set S. However, for S with a moderate value r, the number of all possible layer configurations can be quite large and thus the optimal depth is usually hard to determine. To deal with such complicated cases, in the following we further propose a flexible iterative algorithm for optimizing the depth of a circuit with no complementary gates.

B. Flexible iterative depth-optimization algorithm

In this section we propose an iterative algorithm, Algorithm 1, for optimizing the depth of MCZR circuits with no complementary gates, and reveal its flexibility with a use case.

Algorithm 1. Iterative depth-optimization algorithm for MCZR circuits.

Input: A depth-d MCZR circuit C with its constituent gates located from left to right as a sequence $S = [\gamma_k : k = 1, 2, \ldots, m]$, with γ_k the qubit set of the kth gate, an iteration number $T \geqslant 1$.
Output: A circuit C_{opt} over gates in S with a layer configuration $R = \{L_i : i = 1, 2, \ldots, d_{\text{opt}}\}$ such that $d_{\text{opt}} \leqslant d$.

main program:
Calculate the circuit depth lower bound d_L for S by Eq. (23).
$[R^{(1)}, d^{(1)}] =$ `Greedy_Layer_Formation` (S); $t \leftarrow 1$;
if $d^{(1)} > d_L$ & $T \geqslant 2$ **then** // `Perform iterative layer formation.`
  for $t \leftarrow 2$ **to** T **do**
    $S^{(t)} =$ `Generate_New_GateSeq`$(R^{(t-1)})$;
    $[R^{(t)}, d^{(t)}] =$ `Greedy_Layer_Formation`$(S^{(t)})$;
    if $d^{(t)} == d_L$ **then**
      break;
    end if
  end for
end if
$d_{\text{opt}} \leftarrow d^{(p)} = \min\{d^{(q)} : q \in [t]\}$; $R \leftarrow R^{(p)}$;
return $[R, d_{\text{opt}}]$.
function `Greedy_Layer_Formation`(S)
  $i \leftarrow 0$;
  while $|S| \neq 0$ **do**
    $i \leftarrow i + 1$; $c \leftarrow 0$; $L_i \leftarrow \varnothing$; remove_set $\leftarrow \varnothing$;
    for $k \leftarrow 1$ **to** $|S|$ // `Greedily form the layer` L_i.
      if L_i and $S[k]$ have no integers in common **then**
        $c \leftarrow c + 1$; $L_i[c] \leftarrow S[k]$; remove_set$[c] \leftarrow k$;
      end if
    end for
    Delete S[remove_set];
  end while
  $d \leftarrow i$;
  return $[R = \{L_1, L_2, \ldots, L_d\}, d]$.
end function
function `Generate_New_GateSeq`$(R = \{L_i = [\gamma_1^i, \gamma_2^i, \ldots, \gamma_{|L_i|}^i] : i = 1, 2, \ldots, d\})$:
  $S = [\gamma_1^1, \gamma_1^2, \ldots, \gamma_1^d, \gamma_2^1, \gamma_2^2, \ldots, \gamma_2^d, \ldots, \gamma_{|L_p|}^p]$ with the layer index p such that $|L_p| = \max\{|L_i| : i \in [d]\}$;
  return S .
end function

The input of Algorithm 1 includes a given MCZR circuit C with its constituent gates located from left to right as a sequence $S = [\gamma_k : k = 1, 2, \ldots, m]$, with γ_k the set of qubits acted upon by the kth gate and an iteration number $T \in \mathbb{N}^+$. The output is a circuit over gates in S that has a depth smaller than or equal to that of C. Notice that

two subroutine functions `Greedy_Layer_Formation` and `Generate_New_GateSeq` are introduced here: The former receives a gate sequence S and can arrange as many disjoint gates in S into each layer as possible to form a circuit layer configuration R, while the latter can generate a new gate sequence S from a given circuit $R = \{L_i : i = 1, 2, \ldots, d\}$ by extracting and regrouping gates in original layers L_i. Since the application of our greedy layer formation procedure on different sequences over a given MCZR gate set may result in distinct circuits, we will iteratively use these two functions in our main program to seek circuits with the shortest possible depth as follows.

First, since two gates that act on the same qubit must be located in different layers of a circuit, a depth lower bound d_L on all possible circuits constructed from the input gate set S can be derived as

$$d_L(S) = \max\{c(j, S) : j \in [n]\}, \tag{23}$$

where $c(j, S)$ indicates the number of integer j appearing in S. Second, we apply the function `Greedy_Layer_Formation` to the input gate sequence S and obtain a new depth-$d^{(1)}$ circuit with layer configuration $R^{(1)}$ such that $d^{(1)} \leqslant d$. Third, if $d^{(1)} > d_L$ and $T \geqslant 2$, we can further iteratively generate a new gate sequence $S^{(t)}$ from the previous circuit $R^{(t-1)}$ via `Generate_New_GateSeq` , followed by applying `Greedy_Layer_Formation` to obtain a new circuit $R^{(t)}$ of depth $d^{(t)}$ in each loop $t \geqslant 2$. In this process, we can terminate the loop when getting the optimal depth as $d^{(t)} = d_L$. Finally, we choose the circuit with the shortest depth among all constructed $\{R^{(t)}\}$ above as our output depth-optimized circuit $R = \{L_1, L_2, \ldots, L_{d_{\text{opt}}}\}$. As a result, Algorithm 1 ensures that (i) $d_{\text{opt}} \leqslant d^{(1)} \leqslant d$ and (ii) $d_{\text{opt}_2} \leqslant d_{\text{opt}_1}$ for two iteration numbers $T_2 \geqslant T_1$. Therefore, Algorithm 1 controlled by an iteration number T is a flexible depth-optimization algorithm by considering the relation between the reduced depth and optimization time cost.

A demonstrative example of Algorithm 1 is shown in Fig. 3. The gate sequence for the six-qubit and depth-7 circuit C consisting of nine two-qubit CZ(θ) gates as shown in Fig. 3(a) is

$$S = [\{1, 2\}, \{1, 3\}, \{2, 3\}, \{1, 4\}, \{4, 5\}, \{5, 6\}, \{2, 5\}, \{3, 6\}, \{4, 6\}]. \tag{24}$$

We apply Algorithm 1 with $T = 2$ to achieve a depth-optimized circuit as follows.

(i) First, we calculate the depth lower bound on circuits for S by Eq. (23) as $d_L = 3$.

(ii) Second, we apply `Greedy_Layer_Formation` to S in Eq. (24) and obtain a new circuit $C^{(1)}$ of depth $d^{(1)} = 4$ as shown in Fig. 3(b), which has a layer configuration $R^{(1)} = \{L_1, L_2, L_3, L_4\}$ with

$$\begin{aligned} L_1 &= \left[\gamma_1^1 = \{1, 2\}, \gamma_2^1 = \{4, 5\}, \gamma_3^1 = \{3, 6\}\right], \\ L_2 &= \left[\gamma_1^2 = \{1, 3\}, \gamma_2^2 = \{5, 6\}\right], \\ L_3 &= \left[\gamma_1^3 = \{2, 3\}, \gamma_2^3 = \{1, 4\}\right], \\ L_4 &= \left[\gamma_1^4 = \{2, 5\}, \gamma_2^4 = \{4, 6\}\right]. \end{aligned} \tag{25}$$

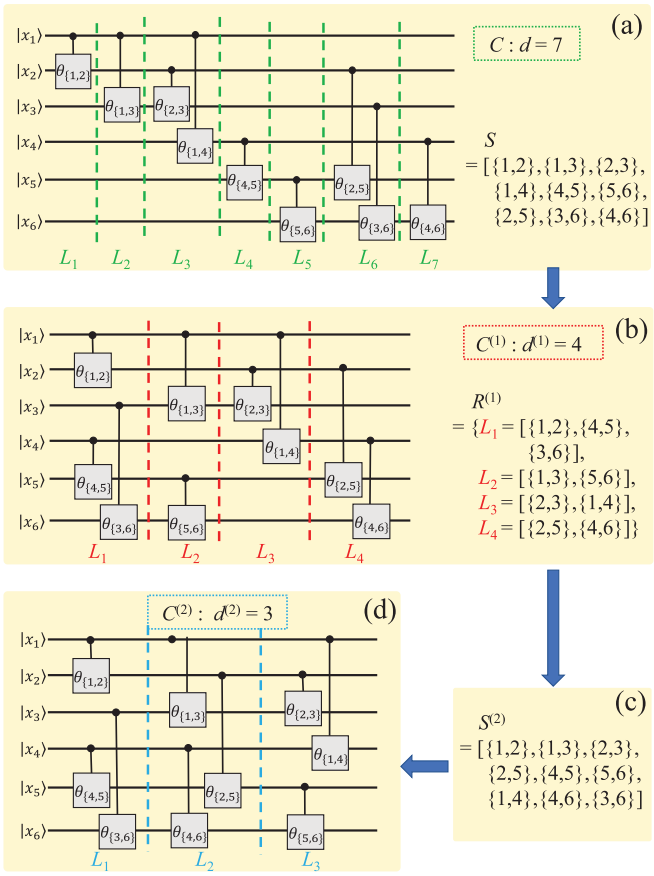


FIG. 3. Example demonstrating Algorithm 1 with $T = 2$. (a) Given six-qubit MCZR circuit C of depth $d = 7$, with its nine two-qubit gates CZ($\theta_{\{i,j\}}$) being separated by green dashed lines as $\{L_1, L_2, \ldots, L_7\}$ and in a sequence $S = [\{1, 2\}, \{1, 3\}, \ldots, \{3, 6\}, \{4, 6\}]$. The circuit depth lower bound for S is $d_L = 3$ by Eq. (23). Then we apply the function `Greedy_Layer_Formation` to (a) and obtain a circuit $C^{(1)}$ of depth $d^{(1)} = 4$, as shown in (b), where its four gate layers are separated by red dashed lines as $R^{(1)} = \{L_1, L_2, L_3, L_4\}$ and Eq. (25). Due to $d^{(1)} > d_L$ and $T = 2$, next we apply the function `Generate_New_GateSeq` to $R^{(1)}$ and generate a new gate sequence $S^{(2)}$ in (c). Once again, we apply `Greedy_Layer_Formation` to (c) and obtain a new circuit $C^{(2)}$ of depth $d^{(2)} = 3$ in (d), achieving the optimal circuit depth d_L.

Intuitively, the comparison between the circuit C in Fig. 3(a) and $C^{(1)}$ in Fig. 3(b) reveals that the working principle of our function `Greedy_Layer_Formation` is to move the gates in the right column of the original circuit to fill the vacancies in the left column as much as possible, thus causing a circuit depth reduction.

(iii) Third, we apply `Generate_New_GateSeq` to $R^{(1)}$ in Eq. (25) due to the condition $d^{(1)} > d_L$ and $T > 1$ and generate a new gate sequence $S^{(2)}$ shown in Fig. 3(c) as

$$S^{(2)} = [\{1, 2\}, \{1, 3\}, \{2, 3\}, \{2, 5\}, \{4, 5\}, \{5, 6\}, \{1, 4\}, \{4, 6\}, \{3, 6\}]. \tag{26}$$

(iv) Finally, we apply `Greedy_Layer_Formation` again to Eq. (26) and obtain a new layer configuration $\{L_1, L_2, L_3\}$, that is, the circuit $C^{(2)}$ of depth $d^{(2)} = 3$ as shown in Fig. 3(d).

Note that if we apply Algorithm 1 with only $T = 1$ to S in Fig. 3(a), the resultant depth-optimized circuit would be just $C^{(1)}$ in Fig. 3(b). This simple example implies that if we apply `Greedy_Layer_Formation` to more distinct gate sequences generated from `Generate_New_GateSeq` , the more significant depth reduction over the original circuit is likely to occur at the expense of more optimization time. More practical cases of applying Algorithm 1 to optimize the MCZR circuit depth will be demonstrated in Sec. V.

V. PERFORMANCE EVALUATION

To further evaluate the performance of the proposed synthesis and optimization methods, here we refine them into two explicit workflows and consider their applications to two typical use cases in quantum computing. All evaluations are performed with MATLAB 2022A on an Intel Core i5-12500 CPU operating at 3.00 GHz frequency and with 16 GB of RAM.

A. Workflow of our synthesis and optimization methods

For convenience, here we summarize the main results in Secs. III and IV into the workflow to fulfill two types of tasks as follows.

Task 1. Determine how to construct a gate-count-optimal MCZR circuit followed by further depth optimization to implement a given diagonal unitary matrix in Eq. (7).

Workflow 1. First, we synthesize a gate-count-optimal MCZR circuit according to Theorem 3 with m gates, which includes two parts: (i) d_1 layers of complementary gates denoted by C_1 and (ii) the other $(m - 2d_1)$ gates. Second, we apply Algorithm 1 with a specified parameter T to optimize part (ii) into a depth-d_2 circuit C_2. Finally, the overall output circuit is $C = C_1 \circ C_2$ of depth $d_1 + d_2$.

Task 2. Determine how to optimize the circuit depth of a given MCZR circuit C over the gate set $S = \{G(v, \theta_v)\}$ with $|S| = m$.

Workflow 2. First, we perform the gate-exchange operation to C according to Lemma 2, which arranges all d_1 pairs of complementary gates in S into a depth-d_1 circuit denoted by C_1. Second, we apply Algorithm 1 to the other $m - 2d_1$ gates and obtain a circuit C_2 of depth d_2. Finally, putting these results together gives an optimized-depth circuit $C_{\text{opt}} = C_1 \circ C_2$ of depth $d_1 + d_2$.

In the following, we demonstrate the utility of the above workflows for two practical quantum computing tasks: (i) constructing diagonal Hermitian quantum operators and (ii) optimizing the depth of QAOA circuits.

B. Diagonal Hermitian quantum operators

We use $D_H^{(n)}$ to denote an n-qubit diagonal Hermitian quantum operator with its diagonal elements being ± 1, and there are totally 2^{2^n-1} different such operators since $D_H^{(n)}$ and $-D_H^{(n)}$ are essentially equivalent. Note that operators of this type act as the oracle operator or fixed operator in the well-known Deutsch-Jozsa algorithm [57,58], Grover's algorithm [59], and some recent algorithms showing quantum advantage for string learning and identification [53,60,61]. Therefore, an efficient construction of $D_H^{(n)}$ over MCZR gates would facilitate the implementation of relevant quantum algorithms on specific devices [23,28,31].

Prior work [36] has revealed that $D_H^{(n)}$ can be synthesized by at most $2^n - 1$ multiple-controlled Pauli Z gates, that is, MCZR gates with a fixed angle parameter π, based on a binary representation and solving linear equations over the binary field $\mathbb{F}_2$. As a comparison, here we apply our synthesis and optimization methods to construct circuits for realizing such operators; to be more specific, our strategies include a pairwise synthesis method in Theorem 3 (app01) and our Workflow 1 in Sec. V A with $T = 1$ (app02), $T = 5$ (app03), and $T = 20$ (app04), respectively. We compare their performance on all 8, 128, and 32 768 diagonal Hermitian operators $D_H^{(n)}$ for $n = 2, 3, 4$, respectively, as well as 100 randomly selected ones for each $5 \leqslant n \leqslant 12$, and compare our results with the previous work. Due to the uniqueness property, our constructed circuits have the same MCZR gate set as that from Ref. [36] and therefore we mainly illustrate our circuit depth reduction. The detailed evaluation results are presented in Fig. 4.

In Fig. 4(a) we present the average circuit depth of n-qubit MCZR circuits ($n \in [2, 12]$) constructed from the previous work [36] and our four strategies app01, app02, app03, and app04 by the blue, purple, orange, green, and red curve, respectively. Accordingly, the average execution time to construct a circuit of size n by these strategies is recorded in Fig. 4(b). Typically, the time growth of our sole circuit synthesis algorithm app01 as a function of n agrees well with the total time complexity of calculating Eq. (9), that is, proportional to $n3^n$. As a comparison, the time of previous work [36] increases more drastically with n, since its most time-consuming procedure for solving linear equations over $\mathbb{F}_2$ to determine whether each MCZR gate exists or not would require time scaling roughly as $O(N^3) = O(8^n)$. It is worth noting that all four of our strategies have both a reduced circuit depth and less execution time compared to the previous work. In Fig. 4(c) the circuit depth reduction curve for each of our strategies shows an explicit upward trend as the circuit size n increases, which can achieve as high as 28.88%, 40.51%, 41.40%, and 42.27% for constructing a circuit of $n = 12$ on average for times 38.40, 38.79, 40.16, and 45.78 s, respectively. Also, the usefulness of Algorithm 1 is reflected by observing that app02 can achieve a 11.57% smaller depth than the sole synthesis algorithm app01 at the expense of only 1.03% more time for circuits of $n = 12$, while app03 and app04 give us shorter and shorter depths as T increases. Finally, in Fig. 4(d) we evaluate the overall average performance of our strategies app01, app02, app03, and app04 for all involved circuit instances with $n \in [2, 12]$, including the average depth reductions of 23.29%, 32.16%, 32.88%, and 33.40% and the average time ratios of 36.93%, 37.31%, 38.59%, and 43.67% with respect to the previous work, respectively. It seems that for such circuit instances, the average depth-optimization trend would rise slowly as the iteration number T in Workflow 1 increases.

In summary, we have demonstrated our Workflow 1 for synthesizing and optimizing MCZR circuits by taking diagonal Hermitian operators as an example, which can show substantial improvement over the previous work in terms of both circuit depth and execution time. In addition, our results

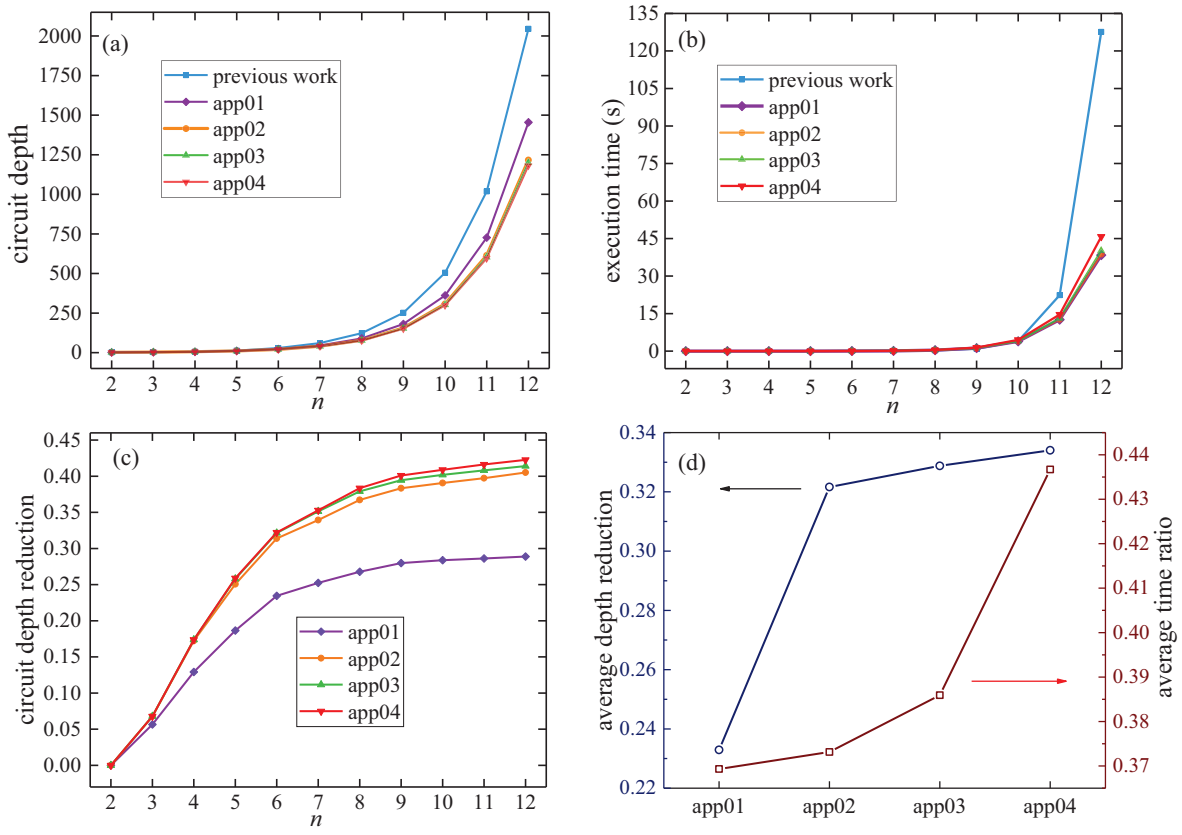


FIG. 4. Evaluation results of constructing diagonal Hermitian operators with size $n \in [2, 12]$ by applying a previous method [36], our circuit synthesis method in Theorem 3 (app01), and our Workflow 1 with $T = 1$(app02), 5(app03), and 20(app04), respectively. (a) Blue, purple, orange, green, and red curves indicate the average depth of circuits obtained from previous work and app01–app04 for each n, respectively. Accordingly, the execution time and circuit depth reduction over the previous work as a function of n on average are recorded in (b) and (c), respectively, indicating that our four strategies can achieve both a reduced circuit depth and less execution time compared to previous work. Notably, all our strategies can have a more significant depth reduction for large-size n, and the effectiveness of our depth-optimization Algorithm 1 can be reflected by comparing app02–app04 with app01. (d) As an overall performance evaluation, the average depth reduction and time ratio of our four strategies over the previous work for the entire set of instances are displayed by dark blue and dark red lines, respectively, such that on average we can achieve a 33.40% depth reduction with only 43.67% time by app04.

empirically validate that a shorter circuit depth is likely to be achieved by increasing the iteration number T in Algorithm 1 with more time [see Fig. 4(d)], thereby demonstrating the applicability of our algorithm for the general case that consists of one-qubit to n-qubit MCZR gates. In the following, we focus on another example to highlight the flexibility of Algorithm 1 for realizing controllable depth optimization.

C. Phase-separation part in the QAOA circuit

The quantum approximate optimization algorithm is a well-known hybrid quantum-classical algorithm designed to solve combinatorial optimization problems. A typical stage of the QAOA circuit for the max-cut problem consists of three parts: a layer of Hadamard gates, a phase-separation part consisting of CZ(θ) gates, and a layer of R_x rotation gates. Here we focus on reducing the depth of the middle part in n-qubit max-cut QAOA circuits of 3-regular graphs [50] by using our Workflow 2 in Sec. V A, which is thus Algorithm 1 for $n \geqslant 6$.

Prior work [50] has used a so-called min-layer formation (MLF) procedure to reduce the number of CZ(θ) gate layers in QAOA circuits, which is exactly a particular case of our Algorithm 1 with the iteration number taken as $T = 1$. For comparison, here we apply Algorithm 1 with $T = 1, 2, 3, 4, 5$ to optimize such a phase-separation part consisting of two-qubit CZ(θ) gates in QAOA circuits, respectively. According to the definition of 3-regular graphs such that every vertex is connected to three other vertices, the circuit depth lower bound in Eq. (23) is determined to be 3 for any circuit instance input to Algorithm 1. As an example, the depth optimization of a six-qubit phase-separation circuit C of depth 7 by taking $T = 2$ has been presented in Fig. 3. More broadly, here we pick the n-qubit circuit instances corresponding to n-node 3-regular graphs with n an even number in the range from 6 to 50, and for each size n we randomly pick 100 graphs. Thus, a total of $23 \times 100 = 2300$ max-cut QAOA circuit instances have been used for the evaluation. The evaluation results are presented in Fig. 5.

The black curve in Fig. 5(a) indicates the average circuit depth of 100 original randomly selected n-qubit QAOA circuits with $3n/2$ CZ(θ) gates for $n \in [6, 50]$, showing an overall rising trend with some small oscillations. This is because a larger number of qubits provide the possibil-

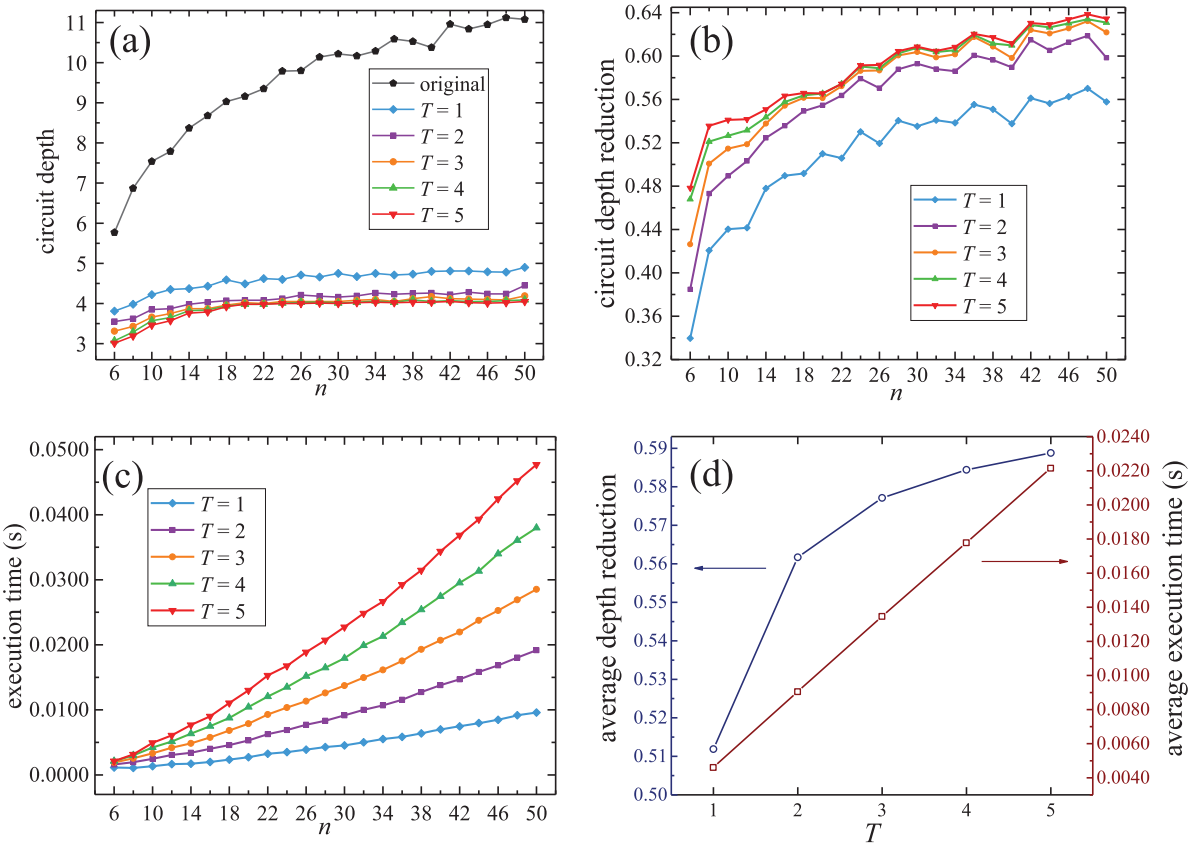


FIG. 5. Evaluation results of optimizing the depth of phase-separation parts in 100 randomly selected n-qubit QAOA circuits with even $n \in [6, 50]$ by applying Algorithm 1 with $T = 1, 2, 3, 4, 5$, respectively. (a) Black, blue, purple, orange, green, and red curves indicate the average circuit depth of original 100 random n-qubit instances as well as optimized ones with $T = 1, 2, 3, 4, 5$, respectively. Accordingly, the circuit depth reduction and execution time as a function of n on average are recorded in (b) and (c), respectively, both of which show an upward trend on the whole. Note that the results for $T = 1$ are equivalent to the previous min-layer formation method aimed at optimizing QAOA circuits [50], while as comparison our Algorithm 1 is more flexible and useful since it can achieve a more significant circuit depth reduction by adjusting the parameter T at the cost of more execution time. (d) As an overall performance evaluation, the average depth reduction and execution time for all 2300 circuit instances with different T are displayed in dark blue and dark red, respectively, where the time cost shows a nearly linear growth when increasing T.

ity of applying more CZ(θ) gates in parallel and thus may cause a smaller circuit depth compared to that with a lower number of qubits for randomly picked circuits. As a comparison, the blue, purple, orange, green, and red curves indicate the optimized circuit depth obtained from performing Algorithm 1 with $T = 1$ (that is, the MLF procedure in Ref. [50]) and $T = 2, 3, 4, 5$, respectively. Specifically, the optimized circuit depth as indicated by the red line in Fig. 5(a) with $T = 5$ grows quite slowly and ranges from 3.00 to 4.05 for $n \in [6, 50]$. Accordingly, Figs. 5(b) and 5(c) show the circuit depth reduction and execution time for each instance with size n on average, respectively. In particular, the depth-reduction curve for each setting T in Fig. 5(b) is calculated from Fig. 5(a) and grows overall with small oscillations as n increases, which can achieve as high as 63.45% for $n = 50$ in time less than 0.05 s when adopting $T = 5$. Furthermore, Fig. 5(d) shows the overall performance of Algorithm 1 with $T = 1, 2, 3, 4, 5$ on all 2300 circuit instances, where on average we can achieve depth reductions of 51.19%, 56.17%, 57.71%, 58.44%, and 58.88% over one original randomly selected QAOA circuit instance by using times of 0.0046, 0.0090, 0.0135, 0.0178, and 0.0222 s for each $T \in [1, 5]$, respectively. Notably, the average execution time scales nearly linearly as T increases from 1 to 5, and the average depth obtained from $T = 5$ is 15.55% smaller than that from $T = 1$ at the expense of a 4.81× increase in time. Once again, these results reflect the flexibility of Algorithm 1 as it can achieve a shorter circuit depth at the expense of more execution time. Therefore, to deal with such a QAOA circuit case one can take Algorithm 1 with gradually increasing iteration number T to seek the best possible results.

Finally, we point out that the expense of depth-optimization time overhead is especially worthwhile in the use case of QAOA since the obtained circuit needs to be executed on the quantum hardware many times to solve the max-cut problem and thus a shorter circuit depth obtained from the precedent optimization procedure could save a large amount of time in the subsequent process of running the QAOA circuit. As a result, our depth-optimized circuits might be executed on the scalable quantum processor with nonlocal connectivity [62] or can act as a better starting point for possible further circuit compilation if needed [50].

VI. CONCLUSION

In this study we presented a systematic study of quantum circuits over multiple-control Z-rotation gates with continuous parameters. Based on an established polynomial representation, we derived a gate-count-optimal synthesis of such circuits to implement any diagonal unitary matrix, which simultaneously enables the circuit depth optimal for specific MCZR circuits. Furthermore, we proposed practical optimization strategies for reducing the circuit depth of any given MCZR circuit, which can show substantial performance improvement over prior works for typical examples in quantum computing. Compared to the conventional study of implementing diagonal unitary operators over the single- and two-qubit gate set [63–65], here we provided an alternative scheme by utilizing a multiqubit gate set as the computational primitives, which would match the quantum experimental progress in certain directions, such as neutral atoms [22,23] and superconducting systems [28,30]. In addition, note that above techniques were introduced to deal with general cases; we point out there may also exist other useful ideas aimed at special-case circuits. For example, particular quantum graph states [55] or hypergraph states [66] can be prepared with linearly many MCZR gates and constant depth by observing their underlying lattice graphs.

A relevant practical challenge is how to adapt our constructed circuits to quantum hardware that has certain physical constraints, such as limited qubit connectivity. We anticipate that such a quantum circuit compilation problem is likely to be addressed by borrowing ideas from previous quantum compilation work oriented to specific physical systems with multiqubit gates [50,67,68]. For example, the strategy of exchanging adjacent qubits with a SWAP gate enables an MCZR gate that originally acts on a set of unconnected qubits to be accomplished. Meanwhile, the gate count and circuit depth are two cost metrics of the compiled MCZR circuit that need to be minimized to improve error resiliency and circuit execution time. We believe the fruits of these explorations in future work would lead to performing experimental validation on real quantum hardware, which would enhance the practical relevance of the study on MCZR circuits.

Although this paper mainly focused on quantum circuits over MCZR gates, it may help the research on other types of circuits as well. First, the circuit-polynomial correspondence put forward to characterize MCZR circuits extends the concept of phase polynomial representation [69], again implying that an appropriate representation could facilitate circuit synthesis and/or optimization. Second, the depth-optimization strategies introduced in Sec. IV are actually suitable for any quantum circuit over commuting gates, such as instantaneous quantum polynomial-time circuits used to demonstrate quantum advantage [70]. Third, this study sheds light on implementing diagonal unitary operators over alternative gate sets; for example, a $C^{(k)}Z(\theta)$ gate with $k \geqslant 2$ and any parameter θ in our constructed circuit can be replaced by a set of multiple-control Toffoli gates that act on no more than k qubits together with single-qubit Z-rotation gates [4], leading to more types of circuit constructions and potential applications. A detailed investigation of these interesting topics is left for future work.

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