# Quantum circuit engineering for correcting coherent noise

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(Received 2 September 2021; accepted 1 February 2022; published 18 February 2022; corrected 1 March 2022)

Crosstalk and several forms of coherent noise are invisible when a qubit or a gate is calibrated or benchmarked in isolation. These are unlocked during the execution of a full quantum circuit applying entangling gates to several qubits simultaneously. Unitary crosstalk noise, such as an unwanted *Z*-*Z* coupling, limits the state fidelity during the execution of cross-resonance controlled-NOT (CNOT) gates in superconductor quantum computers. This work presents (1) a method of tracing coherent errors by exploiting their sensitivity to the arrangement of CNOT gates in the circuit and (2) a correction scheme that modifies the original circuit by inserting carefully the chosen compensating gates (single- or two-qubit) to possibly undo coherent errors. On two vastly different types of IBMQ processors offering quantum volume 8 to 32, our experimental results show up to 25% reduction in the infidelity of [[7, 1, 3]] code $|+\rangle$ state (Clifford circuits) and five- to 15-qubit $W$ states (non-Clifford circuits). Our experimental circuits aggressively deploy forced commutation of CNOT gates to obtain low-noise state-preparation circuits. An encoded state initialized with fewer errors marks an important step towards successful demonstration of fault-tolerant quantum computers.

DOI: 10.1103/PhysRevA.105.022428

## I. INTRODUCTION

In state-of-art quantum processors, two-qubit gates, being at least an order of magnitude noisier than their single-qubit counterparts, dictate the state fidelity [1–4]. Higher operational inaccuracy is not the only bottleneck of state fidelity; the action of the controlled-NOT (CNOT) gate sequence adds to several context-dependent noise sources including crosstalk [5], coherent or systematic errors [6,7], correlated errors [8], and non-Markovian baths [9,10]. These are some examples of unforeseen errors [11] mostly unfolding during the execution of the quantum circuit. Such circuit-level errors are less visible in the individual gate calibration usually performed prior to the circuit run. Several recent studies illustrate prevention [12–17], hardware mitigation [8,18–21], and software mitigation [22–24] of circuit-level noise. Unfortunately, in the presence of a large number of uncorrected errors, it still remains unclear how to leverage improved CNOT gate fidelities to prepare higher fidelity quantum states.

This study illustrates quantum circuit engineering for correcting unwanted *Z*-*Z* coupling crosstalk and other unitary errors [20] pervasive in the superconductor cross-resonance CNOT gates [25,26]. Our noise-compensated circuits initialize a higher fidelity Steane code [27] graph state on state-of-art IBM quantum processors. One of the main findings of our study reveals the sensitivity of state fidelity to the placement of the CNOT gate with *Z*-*Z* crosstalk, and it serves one part of our noise probe. Commuting CNOT gates, when infected with crosstalk, may yield noncommuting quantum operations in a physical circuit, leaving the state fidelity dependent on execution order of the gates. Figure 2 below provides a proof-of-concept state-preparation circuit mapped to the IBMQ device ibmq_melbourne (Melbourne), which is known for high crosstalk noise [28] because of its denser topology. Our simulation and experimental error analysis show approximately 20% change in the phase-flip error probability $p_z$ when two commuting CNOT gates are reordered as illustrated in Fig. 2. Here $p_z$ is defined as the probability that there is at least one phase-flip error in the [[7, 1, 3]] logical $|+\rangle$ state. The other part of the noise probe comes from tracing $p_z$ along the time axis describing the circuit execution progress. Addition of crosstalk may significantly raise the likelihood of phase-flip errors and introduce a marked deviation from an otherwise smoothly decaying decoherence curve. Figure 3 below highlights a precipice at gate 6 in the experimental phase fidelity, $\sqrt{(1-p_z)^n}$, which sharply contrasts with the simulated decoherence curve without crosstalk or unitary phase-flip errors. Section III C contains further elaboration of these results. Once detected, the likely *Z*-*Z* coupling can be largely canceled out by inserting a compensating gate, $R_{ZZ}(\theta)$, defined as

$$R_{ZZ}(\theta) = e^{-i\frac{\theta}{2}}|0\rangle\langle 0| + e^{i\frac{\theta}{2}}|0\rangle\langle 1| + e^{i\frac{\theta}{2}}|1\rangle\langle 0| + e^{-i\frac{\theta}{2}}|1\rangle\langle 1|$$

The correction procedure can be direct or indirect; the former is illustrated in Figs. 1 and 2. In the circuit identities of Fig. 2(d), the *Z*-*Z* coupling on CNOT gate simplifies to a single-qubit rotation about the $Z$ axis. It can be corrected by applying a conjugate single-qubit gate at the appropriate circuit location. Notice that experimental phase-flip error probabilities are significantly higher than those of simulation. Even though predicting circuit error rates is not the central objective of this study, our experience working with the IBMQ qiskit noise simulator suggests that the gap may be attributed

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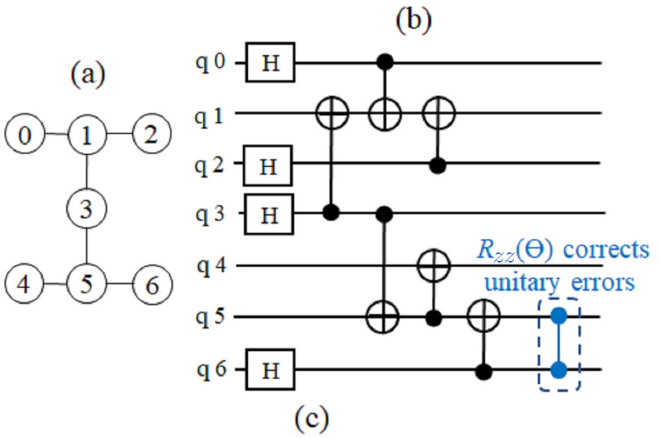



(c)

| Circuit | Phase Fidelity | Overall Fidelity |
|---|---|---|
| Without $R_{zz}(\Theta)$ gate | $0.90 \pm 0.003$ | $0.86 \pm 0.002$ |
| With $R_{zz}(\Theta)$ gate | $0.95 \pm 0.001$ | $0.90 \pm 0.001$ |

FIG. 1. An example of quantum circuit engineering. (a) Topology of IBMQ seven-qubit processors including ibm_lagos that ran the circuit. (b) A noise-compensated state-preparation circuit containing $R_{ZZ}(\theta)$ gate prepares a seven-qubit fully entangled state with higher fidelity than the uncompensated circuit [without $R_{ZZ}(\theta)$]. The table (c) compares fidelities with and without $R_{ZZ}(\theta)$. Note that in this example $\theta = -\pi/3.5$.

to several unmodeled circuit-level errors. Novel benchmarking tools, for example, cycle benchmarking [29], may better correlate simulation and experiment error probabilities.

Indirect cancellation is more subtle and relies on experimental intuition that *Z-Z* coupling on two CNOT gates in the circuit can cancel each other. Inserting a compensating two-qubit stabilizer gate of the form *H a*; CNOT (*a, b*); *H a*; *X b* into a carefully chosen circuit location may introduce an opposite angle *Z-Z* coupling to cancel original crosstalk, in a manner very similar to the direct method. Figure 3 evidences this effect in the form of nearly identical compensated circuit infidelity curves; both schemes insert compensating gates at the same circuit location and prevent the fidelity curve from plummeting at gate 7. Our experiments also highlight a significant overall improvement in the state fidelity on both the noisier [quantum volume (QV) = 8] as well as the less noisy (QV = 16 and 32) IBM quantum processors. On QV = 32 chips, we also show similar performance gains for an *X*-basis *W* state of sizes five to 15 qubits. The state preparation circuit is a nonstabilizer circuit because it requires small rotations about the *Y* axis.

There is another interesting dimension of unitary error correction; it overcomes important performance limiting factors of experimental quantum error correction. A stray single-qubit rotation transforms into an unwanted two-qubit gate (1) on multiple encoding qubits or (2) between an encoding qubit and ancilla, as it propagates through entangling gates implementing parity-check operations. In principle, an accurate tracing of these errors remains a difficult problem in fault-path counting and threshold estimates [30]. A state-preparation circuit low in coherent noise can adequately address this problem and facilitates effective implementation of error correction in the near-term quantum processors. The methods developed in this work can be extended to quantum circuits implementing fault-tolerant gates. For example, it has been shown that on Melbourne, the bulk of failure probability of the Steane logical CNOT gate comes from weight-2 errors due to large unitary noise on specific encoding qubit(s). Interested readers may wish to consult Ref. [24] for detailed experiments.

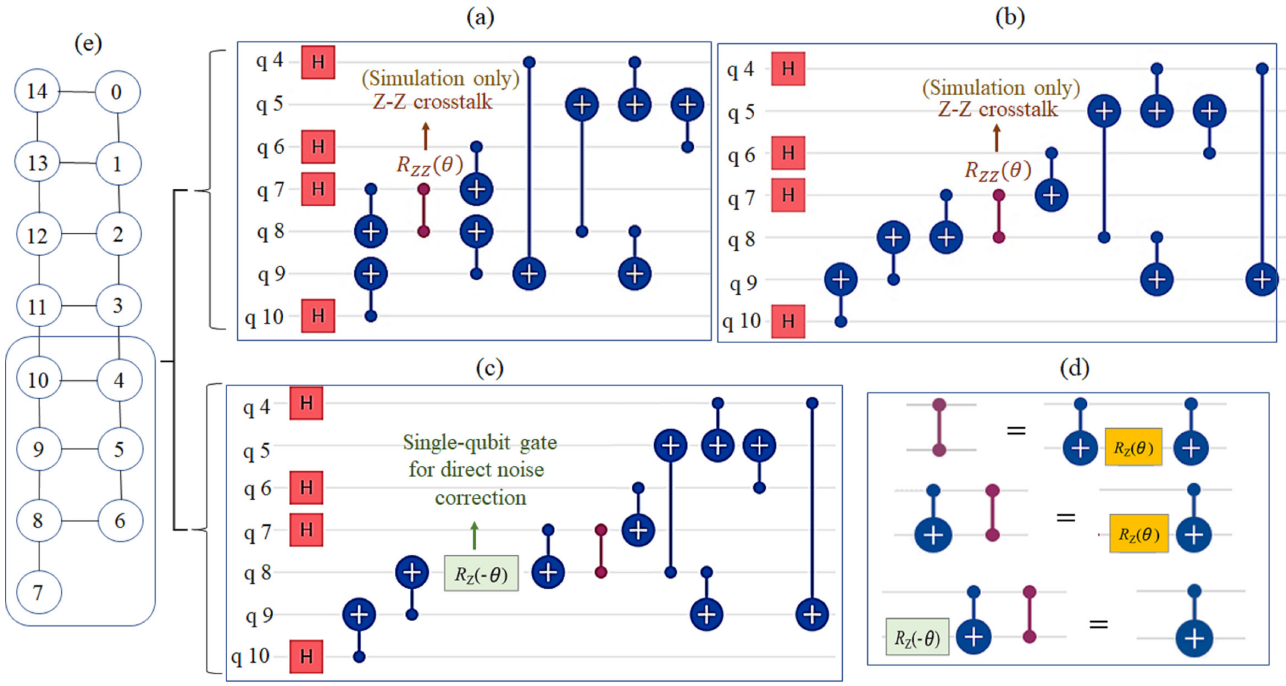
The remaining discussion is organized into five sections. Section II contextualizes the contribution of this work with respect to state-of-art noise mitigation schemes. Experiment setup details, state preparation circuits, and fidelity calculations can be found in Sec. III; results and discussion compose Sec. IV. The summary of relevant prior work can be found in Sec. V, while the conclusion constitutes Sec. VI. Note that in the terminology of this paper, the term *noise correction* means correcting coherent errors by inserting compensating gate(s) into the quantum circuit. Such a circuit is called a *noise-compensated* or simply a *compensated* circuit, whereas an *uncompensated or original* circuit is without the compensating gate.

## II. NOISE CANCELLATION IN THE CONTEXT OF RANDOMIZED COMPILING AND CYCLE BENCHMARKING

In the context of this work, it is worth citing a recently proposed noise mitigation technique called randomized compiling [31]. It transforms coherent noise into a depolarizing channel by applying a random Pauli gate before each CNOT gate and equivalent inverse gate(s) after the gate. Inverse gate(s) are obtained by commuting random Pauli gates through the CNOT gate. In this way the Pauli-*dressed* CNOT gate remains functionally invariant. The same procedure applies to the single-qubit gates of the circuit. Random Pauli gates, however, depolarize the coherent noise channel and lower the likelihood of constructive interference of noise sources causing large errors. This increases the probability of obtaining the correct result from the quantum algorithm or circuit. Reference [32] provides a useful case of randomized compiling; it improves the probability of obtaining the correct output of a four-qubit quantum Fourier transform circuit.

Randomized compiling has inspired a novel and efficient benchmarking scheme, cycle benchmarking [29]. It reports the average gate fidelity under randomized compiling, quantifying the presence of coherent errors surviving Pauli depolarization of quantum gates executed in the same cycle. For a quantum application circuit containing multiple operation cycles, this benchmarking scheme registers both coherent and incoherent errors on parallel gates (and their operand qubits) in the circuit and accurately measures cycle-level error rates. One of its important contributions lies in validating constant gate error rates in the presence of circuit-level noise sources. For example, using cycle benchmarking, one can show that in spite of coherent errors, average fidelities of single-qubit and multiqubit gates remain independent of the number of qubits on the ion-trap quantum computer [29].

Pauli randomization improves the probability of obtaining the correct outcome of a quantum circuit at the expense of higher state impurity [32]. However, it remains unclear if it




| Phase-flip error probability | Circuit (a) | Circuit (b) | Circuit (c) |
|---|---|---|---|
| Simulation | 0.072±0.001 | 0.091±0.001 | 0.072±0.001 |
| Experiment | 0.177±0.003 | 0.233±0.005 | 0.176±0.002 |

FIG. 2. The contextual influence of $Z$-$Z$ crosstalk on phase-flip error probability $p_z$ and how it can be corrected. Circuits (a) and (b) prepare the $[[7, 1, 3]]$ $|+\rangle$ state with a slightly different sequence of CNOT gates. However, simulation (sim) and experiment (expt) results show that (b) has 20% higher $p_z$ than (a). Note that the $R_{ZZ}(\theta = -\pi/3.5)$ crosstalk model is used for simulation only. In circuit (c), the noise-correcting single-qubit $Z$-rotation gate $R_Z(\theta = -\pi/3.5)$ cancels crosstalk in (b) by utilizing the circuit identities in (d). The topology of the ibmq_melbourne (Melbourne) processor is displayed in (e).

also boosts state fidelity. Table I compares randomized compiling with noise cancellation on the circuit given in Fig. 4. It is a typical seven-qubit processor state-preparation circuit used in our experiments. The table data shows that unlike noise cancellation, randomized compiling fails to elevate the baseline state fidelity i.e. the fidelity of the state prepared by the uncompensated circuit. This preliminary comparison suggests that vanishing contours of coherent noise may be

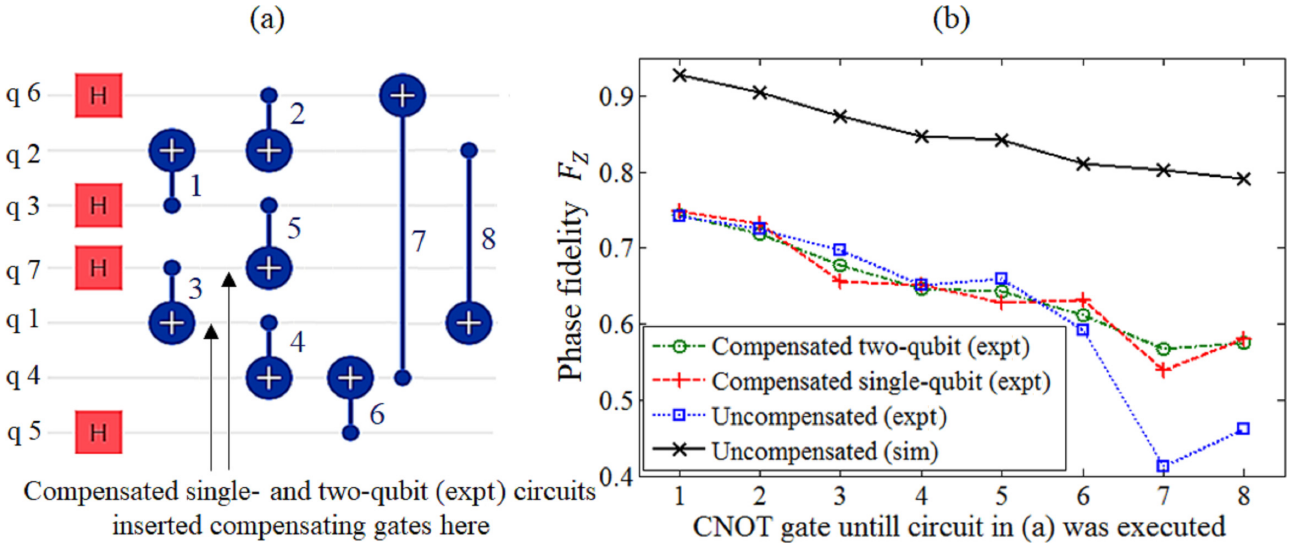



FIG. 3. (a) Example of the Melbourne circuit for tracing errors in the $[[7, 1, 3]]$ code $|+\rangle$ state. (b) The phase fidelity profile. The curve plummets at CNOT gate 7, indicating large coherent error(s). The compensated circuit elevates the curve and lowers infidelity by 33%. The circuit (a) also assigns distinct labels to CNOT gates. These act as the abcissa of the phase fidelity plot in (b).

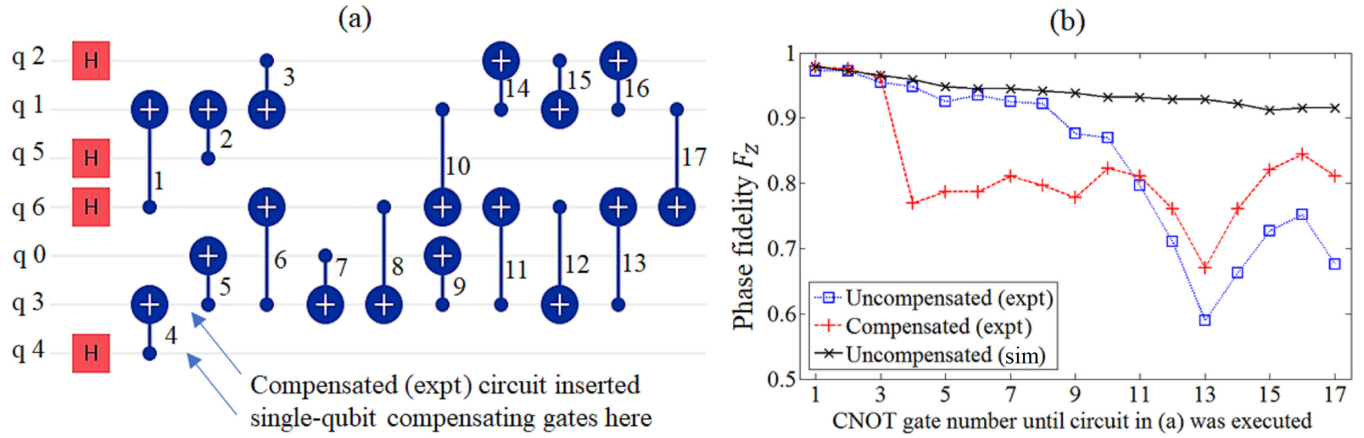



FIG. 4. (a) Example of the ibm_lagos circuit for tracing errors in the [[7, 1, 3]] $|+\rangle$ state. (b) The phase fidelity profile. The curve plummets at CNOT gate 13, indicating large coherent error(s). The compensated circuit elevates the curve and lowers infidelity by 50%. The circuit (a) also assigns distinct labels to CNOT gates. These act as the abcissa of the phase fidelity plot in (b).

unsuitable for their *in situ* correction or cancellation, at least for the entangled states. Yet fault-tolerant quantum computation will eventually need entanglement for implementing logical qubits and gates. How do coherent noise and other circuit-level errors accumulate in the entangled states, and how can these be effectively corrected? Is there a specific structure or pattern to the noise and a way to eliminate its dominant component? These questions expand the active area of research; our work opens avenues to find their answers by means of experimental investigations and insights.

## III. EXPERIMENT TOOLS AND SETUP

The Steane code logical $|+\rangle$ state, $|\bar{+}\rangle$, is defined as

$$|\bar{+}\rangle = \frac{1}{\sqrt{8}}(|+++++++\rangle + |-+-+-+-\rangle + |+--++--\rangle + |--++--+\rangle + |+++---\rangle + |-+--+-+\rangle + |+---+++\rangle + |---+-++-\rangle),$$

where $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$. Designing state-preparation circuits with lower decoherence rate and stochastic errors is critical to effectively unearth otherwise hidden coherent errors. The IBMQ platform enables preparation of the Steane $|+\rangle$ state on the 15-qubit Melbourne and on the seven-qubit ibmq_casablanca ibmq_jakarta, ibm_lagos, and ibm_perth processors. Their topologies, showing qubit-qubit connectivity, can be found in Figs. 1(a) and 2(e). Topologies can be modeled as an undirected graph describing device –level qubit-qubit connectivity. Edges and vertices represent channels of the CNOT gates and their operand qubits, respectively. The logical $|+\rangle$ state encoding requires entangling any seven qubits on the quantum processor. Therefore, in the case of seven-qubit processors, only a single partition of seven qubits is possible. On the other hand, Melbourne can be partitioned into 15 different ways such that each partition clusters seven qubits in a fully connected graph. Figure 2(e) shows one such partition. Because of the fully connected graph, we call these *local* partitions. The significance of the local partition lies is reducing the overhead of noisy swaps for CNOT gate on the nonlocal qubit operands. Minimizing SWAP gates in turn lowers decoherence noise floor and helps unearth otherwise less prominent coherent errors.

TABLE I. Comparison of different noise reduction or mitigation approaches for the [[7, 1, 3]] $|+\rangle$ state-preparation circuit. The state was prepared on the ibmq_casablanca circuit the same as in Fig. 4(a). We chose $\theta = -3\pi/14$ for the noise correction (this work) scheme. For randomized compiling, we ran 20 Pauli randomized experiments of the circuit per datum of state fidelity. A single standard deviation quantifies the margin of error. Mean fidelity and and standard deviations were calculated from at least three experiments, each running 8192 instances of the same circuit.

| Denoising scheme | State fidelity |
|---|---|
| Noise correction ($R_Z(\Theta)$) | 0.55 ± 0.0052 |
| Randomized compiling | 0.44 ± 0.0072 |
| Noise correction ($R_Z(\Theta)$) and randomized compiling combined | 0.44 ± 0.0313 |
| None (uncompensated) | 0.43 ± 0.0041 |

### A. [[7, 1, 3]] State preparation (encoding) circuits

There are multiple ways to map virtual qubits (i.e., qubits in a hardware agnostic circuit) to physical qubits (i.e., qubits in the real processor) for any local partition. Different maps may produce a different sequence of CNOT gates, and hence different circuits in the physical device. Note that for the remaining discussion, the term *circuit* encapsulates the qubit map as well as the CNOT gate sequence. To date, the smallest Steane $|+\rangle$ state circuit contains nine CNOT gates.

#### *1. Zero overhead (nine-gate) circuit for Melbourne*

The gate count can increase only when device topological constraints are taken into consideration. On any processor including Melbourne, a nonlocal CNOT gate is inevitable, which necessitates additional entangling gates for physically nonadjacent qubits. However, by leveraging existing circuit optimization tools such as the following:

(1) Dynamic (re)labeling of qubits [33]

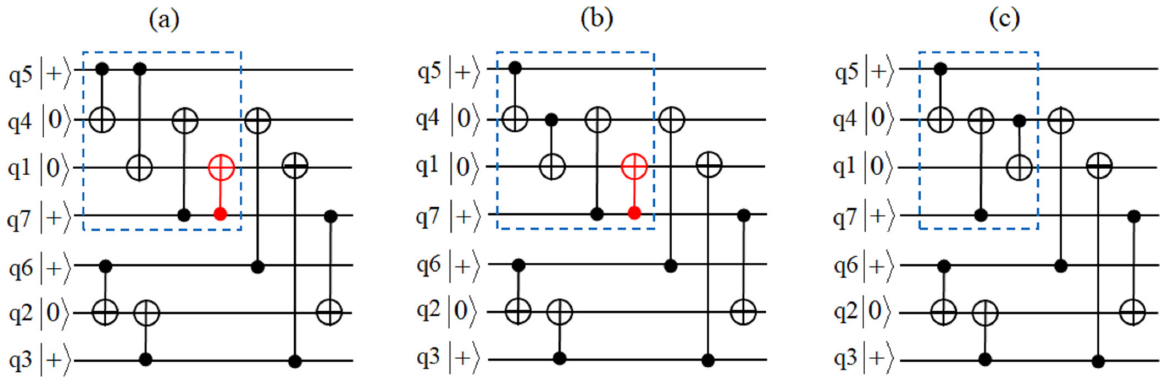



FIG. 5. Forced commutation technique for decrementing CNOT gate count and circuit depth in the [[7, 1, 3]] $|+\rangle$ state-preparation circuit. (a) The nine-gate circuit. (b) The equivalent circuit prepares the qubit-5, 6, and 7 cat-state by changing the control operand of one of the CNOT gates. (c) Swapping the order of CNOT (q7, q4) and CNOT (q4, q1) produces a new CNOT (q7, q1). The new gate cancels the existing CNOT (q7, q1) and produces an eight-gate circuit. The technique doubled the number of circuits for Melbourne experiments.

(2) CNOT gate commutation [14,24]

(3) Alternate three-qubit cat-state circuit shown in Fig. 5(b) we have designed a circuit which incurs no overhead entangling gate and contains only nine CNOT gates (nine-gate) when mapped to the Melbourne hardware sketched in Fig. 2(e). In the figure, both circuits initialize qubits into the Steane $|+\rangle$ state and swap q7 and q8. Final qubit labels are inconsequential, and hence are omitted from the figure. Almost 60% of Melbourne experiments in Figs. 6 and 7 below ran a nine-gate circuit with valid reordering of CNOT gates.

#### *2. Negative overhead (eight-gate) circuit for Melbourne*

It is possible to further decrease the CNOT gate count with the help of another optimization called *forced commutation*, never explored before to the best of our knowledge. The nine-gate circuit in Fig. 5(b) eliminates a (red colored) CNOT (q7, q1) gate by reordering noncommuting CNOT (q7, q4) and CNOT (q4, q1) gates and invoking the circuit identity in (1) to obtain the simpler circuit of Fig. 5(c):

$$\begin{aligned}&\text{CNOT}(a,c)\ \text{CNOT}(b,c)\ \text{CNOT}(a,b)\\ &\quad=\text{CNOT}(a,b)\ \text{CNOT}(b,c).\end{aligned}\tag{1}$$

A resulting decrease in gate count also reduces circuit depth to 4. The eight-gate circuit comprises around 40% of Melbourne experiments in Figs. 6 and 7. It has provably lower phase-flip error probabilities than the nine-gate version for the given partition. In certain Melbourne partitions, adequate noise cancellation can be achieved only in the eight-gate version. An example of an eight-gate circuit is shown in Fig. 3.

#### *3. Circuits for seven-qubit processors*

By contrast, the seven-qubit processors exhibit an order of magnitude lower gate error rates. These offer two- to fourfold higher quantum volume (QV), and their CNOT gates exhibit an average failure probability nearly five times smaller. On the other hand, a higher QV comes at the expense of sparser qubit-qubit connectivity; these devices add several swap gates and double the number of CNOT gates in the physical circuit. Using the same set of gate reduction techniques, we obtained 17- and 18-gate state-preparation circuits. Both are identical except one superfluous CNOT gate. We did not notice any meaningful difference in state preparation error probabilities of 17- and 18-qubit versions. Error analysis of Figs. 6 and 8 uses the 18-gate version. On the other hand, the error-tracing example of Fig. 4(a) contains the 17-gate version.

To summarize, all experiments ran circuits derived by valid reordering of commuting CNOT gates of the example circuits given in Figs. 2 and 3 for Melbourne and Fig. 4 and the last two rows of Table III for seven-qubit processors.

### B. Computing error probabilities

Algorithm 1 details an experimental method of computing and tracing fidelity of the evolving stabilizer state $\rho$. The

**Algorithm 1.** Algorithm of tracing full fidelity of a stabilizer state.

**Input**: An $m-$qubit quantum circuit C containing $n$ gates, annotated with some valid gate execution order $S = [g_1, g_2, g_3, \ldots, g_n]$
**Output**: Array $F$ containing fidelities indexed by gate in $S$
**for** $i \longleftarrow 1$ to $n$ **do**
  $g_i \longleftarrow S[i]$;
  $Fsum \longleftarrow 0$;
  **for** $j \longleftarrow 1$ to $2^m$ **do**
    $s_j^{(i)} \longleftarrow$ obtain $j$-th stabilizer of quantum state by simulating ideal circuit till gate $g_i$
    probSum $\longleftarrow 0$
    **repeat**
      Execute C on real device till $g_i$. It will generate noisy quantum state $\rho$;
      ▷ Destructively measure $\rho$ in $s_j^{(i)}$ to obtain 0/1 outcome
      outcome $\longleftarrow$ Measure $s_j^{(i)}$ on $\rho$
      probSum $\longleftarrow$ probSum + outcome
    **until** $N$ iterations;
    $prob := \text{Tr}[s_j^{(i)}\rho] \longleftarrow \text{probSum}/N$
    $Fsum \longleftarrow Fsum + prob$
  **end**
  $F[i] \longleftarrow \sqrt{Fsum/2^m}$
**end**

method measures all $2^n$ state stabilizers $\{s_k\}_{k=1}^{k=2^n}$ on the state as follows:

$$\text{Fidelity} = \sqrt{\frac{1}{2^n}\sum_{k=1}^{k=2^n} \text{Tr}[s_k\rho]}.$$

Experimentally, calculating the fidelity of a general quantum state becomes computationally expensive as the number of qubits grows. It requires a prohibitively large number of state tomography experiments, although this number shrinks considerably for the stabilizer states. This allowed us to efficiently run state tomography for the [[7, 1, 3]] logical $|+\rangle$ state because only 128 stabilizers were needed to be measured, as generalized in Algorithm 1. For the nonstabilizer states, we have leveraged the fact that arbitrary noise can be decomposed into bit-flip ($X$), phase-flip ($Z$), and bit- and phase-flip ($Y$) errors upon measurement. It is possible to define observables whose measurement statistics reveal a specific subset of Pauli errors. For example, qubits (1) read out in the $Z$ basis will sense both $X$ and $Y$ errors, and state (2) read out in the $X$ basis will sense $Z$ and $Y$ errors. Partial fidelities for the two cases can be efficiently obtained and enable evaluation of correction scheme for the nonstabilizer states. The same framework was also used to quantify component fidelities of the stabilizer state. Next, we outline the procedure of calculating these fidelities from experiment statistics.

To revisit, the metric $p_z$, defined as phase-flip error probability, quantifies the likelihood of phase-flip error averaged over all encoding qubits. It is derived from the phase fidelity $F_z$ as $p_z = 1 - F_z^{2/n}$. We define $F_z$ to be the fidelity between projection $\sum_i p_i E_i \rho E_i^\dagger$ of the real state $\rho$ and the projection $\sum_i q_i E_i|\psi\rangle\langle\psi|E_i^\dagger$ of an ideal state $|\psi\rangle\langle\psi|$, where operators

$$E_i = H|i\rangle\langle i|H$$

constitute POVM with respective outcome probabilities $p_i = \text{Tr}(E_i\rho)$ and $q_i = \text{Tr}(E_i|\psi\rangle\langle\psi|$. By definition $E_i$ renders projection states density matrices diagonal in the $X$ basis only, and therefore their overlap can be computed by classical fidelity measure $\sum_k \sqrt{p_k q_k}$ set equal to $F_z$ as follows:

$$F_z = \sum_k \sqrt{\text{Tr}(E_k\rho)\text{Tr}(E_k\rho)}. \tag{2}$$

Since projective measurements discretize any noise process into Pauli errors, only $Z$ and $Y$ errors will impact $F_z$. This implies that overall fidelity $F(\rho, |\psi\rangle\langle\psi|)$ cannot exceed $F_z$. Experimental computation of the phase fidelity of both the [[7, 1, 3]] logical $|+\rangle$ and $X$-basis $W$ states use this definition throughout the paper. To quantify bit-flip errors, we define bit fidelity $F_x$ according to Eq. (2) with $E_i = |i\rangle\langle i|$. This figure of merit is used in Table II to measure bit-flip noise. Derived from bit fidelity, the probability of bit-flip error, $p_x = 1 - F_x^{2/n}$, compares the performance of the noise correction scheme for the [[7, 1, 3]] logical $|+\rangle$ state in Fig. 7(b) below. The partial fidelity metrics enable efficient experimental means of quantifying reduction in the dominant fidelity-limiting errors.

### C. Tracing unitary errors

Detecting unitary errors requires an adequate tool of tracing error probability in the circuit. Error tracing identifies the appearance of coherent errors by noting the uncharacteristic decline of the phase fidelity curve, for example, the appearance of deep valleys. Two such examples are given in Figs. 3 and 4 for Melbourne and ibm_lagos experiments, respectively. To put things in correct perspective, both figures compare experimental and simulation results so that we can quantify how much circuit level noise has been reduced. For better understanding, we provide relevant details of simulation noise model as follows. The qiskit Ignis tool [34] contains several noise models satisfying CPTP constraints, including a device-specific noise channel derived from latest calibration data. It employs a depolarizing channel to model imperfections in the unitary and nonunitary circuit operations, and amplitude and phase-damping channels for the qubit decoherence. The overall noise model then superimposes all these channels to simulate error probabilities for the whole circuit. However, because it discounts any circuit-level errors, the simulated error probabilities underestimated real noise. As a result, error probabilities obtained from the device noise model can set only the lower limit on $p_z$ and $p_x$ obtained from experimental circuits. The phase fidelity curve obtained from the simulation of the device-specific noise model provides a credible reference to quantify the circuit-level noise reduction. More details of the qiskit Ignis tool can be found in Ref. [34].

Error tracing skips a set of CNOT gates to initialize qubits in a *partial* [[7, 1, 3]] state before Steane measurements. For this purpose, CNOT gates are ordered according to some established rule of representing scheduling constraints, e.g., a dependency graph. We ran the state-preparation circuit only up to the $i$th CNOT gate to collect readout statistics. Tracing $p_z$ for each case of $i \in \{1, 2, 3, \ldots, n\}$ obtains a phase fidelity curve such as those in Figs. 3 and 4. Here $n$ is the total number of CNOT gates in the circuit. For an incomplete circuit, the $p_z$ computation first applies missing CNOT gates in postprocessing as reversible XOR gates before computing $p_z$. The $X$-basis Steane measurements swap the operands of classical XOR operations since *H a; H b;* CNOT *(a,b)*; *H a; H b* = CNOT *(b,a)*.

While the phase fidelity simulation curve declines smoothly throughout, a corresponding experimental curve shows a similar trend up to a point of steep fall, followed by resurrection. Our experiments show that noise correction proves effective whenever a curve shows similar behavior. A deeper valley enables compensated circuits to achieve higher reduction in $p_z$. In both figures, compensatory gates elevate the curve minima, leading to substantial fidelity gain. With reference to the simulation phase fidelity curve, noise correction slashes the infidelity by 50% and 33% for ibm_lagos and Melbourne, respectively. Therefore, it is evident that the most likely cause of sudden decrease in fidelity is a large error on the gate, possibly $Z$-$Z$ crosstalk, which can be corrected by an appropriate conjugate gate. However, curve resurrection behavior may be explained by two hypotheses. One possibility lies in attributing revival of fidelity to the non-Markovian noise. In this model, a quantum circuit can increase the fidelity of the evolving state by recovering the qubit coherence previously lost in qubit-environment interaction. The recovery is

possible if the environment coherence lasts till at least the next qubit-environment interaction [35–37]. Such an environment provides basis for the non-Markovian noise model. A second explanation views increasing fidelity as destructive interference of coherent errors on the gates, for example, CNOT gate-7 and CNOT gate-8 in the case of Fig. 3 and CNOT gate-13 to gate-16 in Fig. 4. The latter hypothesis is simpler and more consistent with the underlying reason of noise cancellation in our compensated circuits. That said, preliminary evidence of non-Markovian or another relevant noise model opens avenues for future work.

It is possible to sense coherent errors by reordering commuting CNOT gates, which can cause substantial change in $p_z$. Figure 2 illustrates this with the help of an example Melbourne circuit simulation as well as experiment. Two circuits (a) and (b) containing the same set of CNOT gates are functionally identical but differ in gate sequence. Circuit (b) dispatches CNOT (q4, q9) to the end and interchanges the order of CNOT (q7, q8) and CNOT (q9, q8). An $R_{zz}(\theta)$ gate simulating $Z$-$Z$ crosstalk on CNOT (q8, q7) produces different $p_z$. In (a), crosstalk acts trivially on the EPR pair, whereas in (b) it introduces nontrivial correlated phase flips on q7 an q8 and elevates $p_z$ by 20%. The error probabilities are higher in the experiments, yet $p_z$ still increases by at least 20%, from 0.177 in (a) to 0.233 in (b). Therefore, the altered gate sequence can sense such unitary errors.

The above example illustrates how reordering commuting CNOT paves the way for reducing circuit-level noise. While this may work fine for the stabilizer circuits containing several commuting CNOT gates, it does not constitute a general solution because the gates may not always commute. Therefore, we need a noise correction tool for general quantum circuits.

### D. Noise correction

#### 1. Melbourne

An effective noise correction tool should be able to decrease $p_z$ lower than gate reordering. On all local partitions we found that gate reordering provided up to a 20% change in $p_z$ in the presence of unitary errors. This number was obtained from rigorous analysis of experimental results of the nine-gate and eight-gate version of Melbourne circuits as well as 17-gate and 18-gate versions of seven-qubit processor circuits. For data collection and analysis, nearly 45 000 circuits were executed on the IBMQ platform. Figure 2 shows that while the error-compensating single-qubit gate $R_z(\theta)$ achieves 20% lower $p_z$ in simulation, the corresponding experiment attains higher reduction—nearly 24%—in the error probability. This underpins one of the main contributions of this work.

Yet $R_z(\theta)$ is not the only route to correct errors; we have found that other single-qubit gates, although not being exact conjugates of unitary errors, nevertheless can be just as effective in certain cases. We are omitting their details in the interest of more interesting results. A two-qubit stabilizer entangling gate of the form $H\,a$; CNOT $(a, b)$; $H\,a\,X\,b :=$ HCNOT, inserted at suitable location, can also undo coherent errors in a manner similar to that of $R_z(\theta)$. It somewhat contradicts the intuition developed in Fig. 2, which shows $Z$-$Z$ crosstalk cancellation necessitates nonstabilizer (conjugate) rotations about the $Z$ axis. However, it is not difficult to explain how the HCNOT gate may replicate crosstalk cancellation by $R_z(\theta)$. Earlier, we described that $Z$-$Z$ couplings on two different CNOT gates can interfere destructively. The HCNOT gate, like other entangling gates, is also noisy; however, it is possible to manipulate its noise to cancel errors and improve state fidelity. The physical HCNOT gate can introduce reverse rotation [e.g., $R_z(-\theta)$] or coupling [$R_{zz}$ $(-\theta)$] to become a noise-correcting gate. The location of the HCNOT gate becomes crucial nonetheless; it must be inserted at a circuit location to ensure that it acts trivially on the ideal state. Our experiments show that HCNOT-based error correction is more effective in Melbourne, whose gates are at least an order of magnitude higher error rate. This is not a surprising result; after all, we wish to counter noise with noise!

We further illustrate noise correction with HCNOT for an example circuit in Fig. 3. The nose-diving phase fidelity curve indicates error on CNOT (q4, q6). With the help of the qiskit qasm simulator, we systematically short-listed circuit locations wherein single or multiple insertions of HCNOT stabilize the evolving state, hoping that in real experiments, some form of a noise-correcting unitary would accompany the HCNOT gate. Among feasible candidate locations, our simulations revealed that a combination of HCNOT (q7, q1) and $R_{zz}$ $(\theta = -\pi/3.5)$ on qubits q4 and q1, inserted at the circuit location shown by arrows, best cancels error on CNOT (q6, q5). At the same location, the HCNOT gate with a tensor product of $R_z(\theta = -\pi/7)$ rotations on q4 and q1 also works equally well. Interestingly, in a real Melbourne experiment, inserting HCNOT works as expected, raising the phase fidelity curve at CNOT (q4, q6), as does the $R_z(\theta)$ curve. A close resemblance between the two experimental curves of Fig. 3(b) further strengthens the hypothesis that HCNOT adds noise-correcting gates to mimic the phase-flip curve of $R_z(\theta)$.

#### 2. Seven-qubit processors

Further experimental evidence of noise cancellation can be found in the phase fidelity curve of the ibm_lagos circuit. The processor exhibits lowest error rates among publicly accessible seven-qubit computing chips. Figure 4(b) shows that adding the $R_z(\theta)$ compensating gate to the circuit, in spite of lowering the curve initially, eventually elevates and sustains phase fidelity considerably higher than the uncompensated circuit gate 13 and onward. Initial decline is less visible in Melbourne experiments, probably due to the high decoherence rate dictating phase fidelity in the early stages of the circuit. On the other hand, ibm_lagos has much longer qubit coherence times; its circuit suffers lesser decoherence, allowing circuit-level noise to strongly influence fidelity. Therefore, the impact of adding unitary rotation can be seen even in the early stages of its circuit. A quick calculation in Fig. 4 shows that the initial 20% deficit of fidelity ($0.96 \rightarrow 0.76$) at gate 4 in the compensated circuit transforms into a 19% gain in fidelity ($0.68 \rightarrow 0.81$) by the end of the circuit. This remarkable symmetry provides much cleaner evidence of noise cancellation.

## IV. EXPERIMENTAL RESULTS AND DISCUSSION

We now discuss phase-flip error-probability experiment results for various Melbourne and seven-qubit processor circuits containing a single partition. The goal is to (1) show

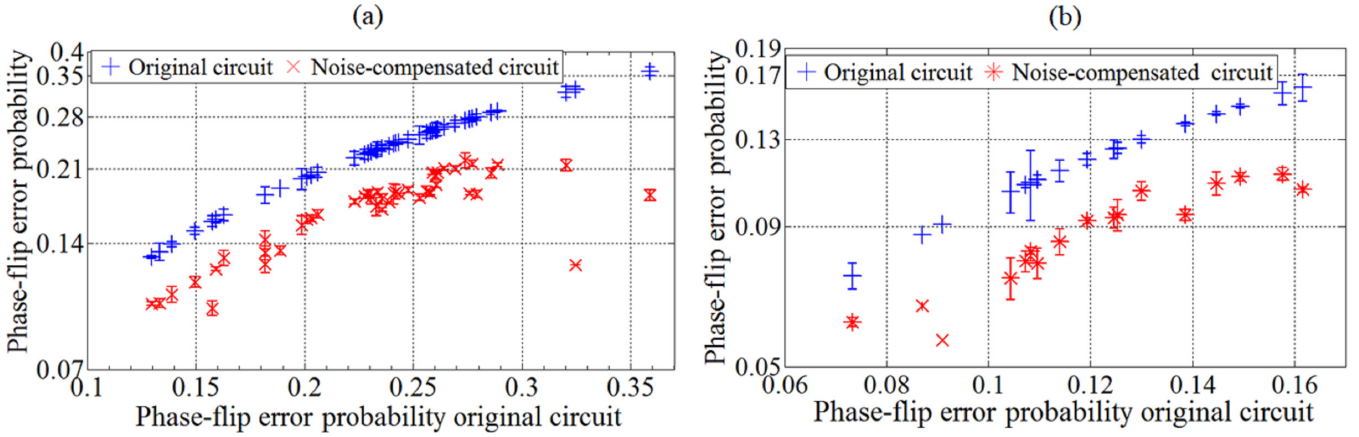



FIG. 6. Compensated circuits lower phase-flip error probability $p_z$ of the [[7, 1, 3]] $|+\rangle$ state on (a) Melbourne and (b) seven-qubit devices (b). All compensated circuits inserted a $R_Z(\theta)$ gate(s) at appropriate locations and lowered error probability by at least 20%. The value of $\theta$ and the circuit location were carefully selected to minimize the compensated circuit error probability. Each data point (original circuit error probability, compensated circuit error probability) is vertically aligned on the graph for a given abscissa and corresponds to a unique circuit (i.e., qubit map and CNOT gate sequence). Melbourne circuits explore noise correction at higher error rates, whereas circuits of seven-qubit devices show that it works even at lower error rates. Error bars show the 95% confidence interval.

at least 20% lower $p_z$ with the compensated circuit and (2) obtain a trend of noise-corrected $p_z$ with an overall increase in the noise. A large number of circuits were experimentally explored to satisfy both requirements. Results of Melbourne and seven-qubit processors are distinguishable because of a significant difference in topologies, error rates, circuit sizes, and depths.

### A. Reducing phase-flip errors using single-qubit compensatory gate: $R_z(\theta)$

Figure 6 compares $p_z$ of an uncompensated (original) and corresponding noise-compensated circuit containing $R_z(\theta)$ gates. It plots ordered pairs $p_z$ (original), $p_z$ (noise-compensated) w.r.t. $p_z$ (original) for a given circuit. The two error probabilities in the pair are vertically juxtaposed, that is, these are meant to be compared along the graph ordinate. This setting enables comparison over a wide range of $p_z$ (original) describing noise levels available in experimental circuit space. We note that noise correction decreases phase-flip error probability in the compensated circuits. In fact, all order pairs lower the error probability by at least 20%. In some cases, the decrease can be 25% or even higher. Melbourne experiments [Fig. 6(a)] examine the efficacy of noise correction at comparatively higher noise levels, whereas seven-qubit processors [Fig. 6(b)] highlight its performance at lower noise levels. Compensated circuits are adequately effective in both cases. On the other hand, adding $R_z(\theta)$ does not change bit-flip error probability $p_x$ except for negligibly small statistical fluctuations. When plotted on the graph, data points of the two circuits were indistinguishable, and hence excluded from the discussion.

Achieving minimal $p_z$, hence maximum phase fidelity, requires fine tuning of the $R_z(\theta)$ gate rotation angle. To this end, we experimentally searched for optimal $\theta$ in the range $0 < \theta \leqslant \pi/2$ by systematically incrementing its value in small steps. Figure 10(c) plots phase fidelity with $\theta$ to locate the optimal rotation angle of the compensating gate.

### B. Reducing phase-flip errors using two-qubit compensatory gate: HCNOT

The HCNOT compensated circuit similarly lowers the phase-flip error probability although at the cost of a slight increase in $p_x$. Still, in most cases, the difference remains less than height of error bars representing a 95% confidence interval. Figure 7(a) displays all ordered pairs in which $p_z$ is lowered by at least 20% in the compensated circuit. Corresponding $p_x$ are compared in Fig. 7(b) showing a small increase in $p_x$, conserving a net decrease in overall error probability. The compensated HCNOT noise correction represents an indirect form of noise correction and remains exclusive to Melbourne, whose entangling gates have high error rates. Adding a noisy stabilizer two-qubit gate can bring new unitary error, which cancels the one on the original circuit.

### C. Quantifying overall noise reduction

The last set of experiments compute fidelity to show overall noise reduction. Algorithm 1 computes fidelity by measuring 128 stabilizers on the [[7, 1, 3]] logical $|+\rangle$ state. This requires 128 experiments per fidelity datum. For selected local partitions of Melbourne and a qubit map of seven-qubit devices, the fidelity results are summarized in Figs. 8 and 9 for $R_z(\theta)$ and HCNOT compensated circuits, respectively. Both figures show fidelity improvement with and without measurement of noise mitigation [38] for selected circuits of Figs. 5 and 7. Qiskit Ignis contains readout noise-mitigation routines that apply linear filtration: $\mathbf{v} = \mathbf{B}^{-1}e$. Here $\mathbf{B}$ is a $2^n \times 2^n$ matrix containing conditional probabilities, and the vectors $v$ and $e$ represent filtered and unfiltered (actual) readout probability distributions. Entries in the $\mathbf{B}$ matrix are conditional probabilities, $P$(actual_readout | correct_readout), and come from a separate set of experiments. The random variables *actual_readout* and *correct_readout* are a seven-bit-long string, quantifying the likelihood of obtaining the correct result for a known (classical) state of qubits. Coherent errors are more

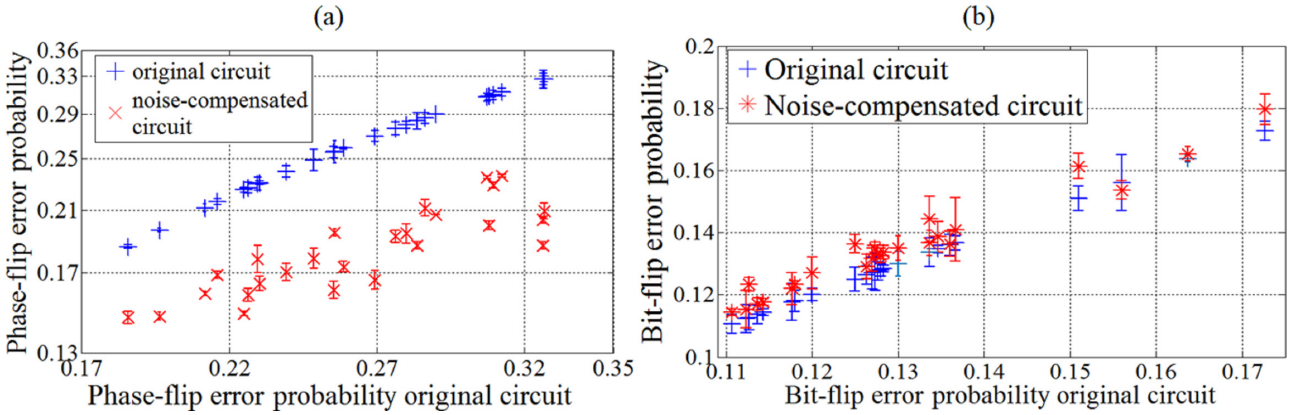



FIG. 7. Performance of HCNOT noise-compensated [[7, 1, 3]] $|+\rangle$ state-preparation Melbourne circuits. (a) Compensated circuits lowered phase-flip error probability; (b) comparison of corresponding bit-flip error probabilities shows inconsequential rise in bit-flip noise. All instances lowered the phase-flip error probability by at least 20%. Each data point (original circuit error probability, noise-compensated circuit error probability) is vertically aligned on the graph for the given abscissa and corresponds to a unique circuit (i.e., qubit map and CNOT gate sequence). These and circuits of Fig. 6(a) exhibit a 20% or higher decrease in the phase-flip error probability on all local partitions of Melbourne. Error bars show the 95% confidence interval.

pronounced at lower readout inaccuracy and provide a greater opportunity of noise correction.

The bar charts in Figs. 8 and 9 juxtapose state fidelities for the compensated circuit $R_z(\theta)$) and original circuits. We define *infidelity* as 1-fidelity to situate these results within the context error-probability graphs. Because bit-flip errors remain uncorrected, only phase-flip error-probability dictates an overall infidelity. In the case of the HCNOT gate, these may slightly increase infidelity. Still, several compensated circuits achieved 20% less infidelity for both compensated circuits and on all devices with mitigated readout noise. Overall, these graphs show several compensated circuits lowering infidelities by more than 25%. In one circuit, $M_5$, the reduction even reach 35%, thereby validating the effectiveness of the noise-correction scheme.

### D. Noise reduction in the $X$-basis $W$ state circuits

For completeness, we show that nonstabilizer states can also be purified from coherent noise. For this set of experiments we choose $X$-basis $W$ state circuits of different sizes and depths. The $n$-qubit $X$-basis $W$ state, $|W_x\rangle$, is defined as

$$|W_x\rangle = \frac{1}{\sqrt{2^n}}(|+++\cdots+-\rangle + |+++\cdots-+\rangle + |++\cdots--\rangle + \cdots + |-++\cdots++\rangle).$$

Experimental circuits prepare the states on three devices: ibm_perth, ibm_lagos, and ibmq_guadalupe. Figure 10 shows ibmq_perth initializing the five-qubit $X$-basis $W$ state. Because circuits contain a controlled rotation about the $Y$ axis, i.e., $R_y(\theta)$, the state cannot be described by stabilizer formalism. In this case, full fidelity calculations become computationally prohibitive. Instead, we present phase fidelities and bit fidelities computed from Algorithm 2 as metrics for comparing noise levels of original and compensated circuits. Seven-qubit devices, ibmq_perth and ibm_lagos, initialize a five- and seven-qubit $W$ state, while a 16-qubit device, ibmq_guadalupe, prepares a nine-, 11-, 13-, and 15-qubit $W$ state. Table II shows that percentage increase in the phase fidelity generally trends upwards for larger and deeper circuits.

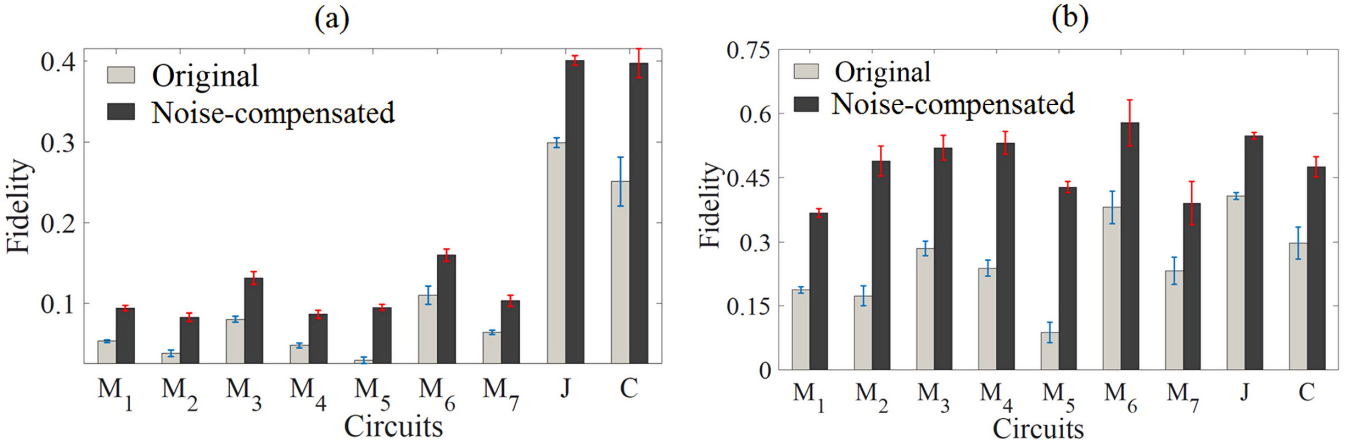



FIG. 8. $R_Z(\theta)$ noise correction increases fidelity of the [[7, 1, 3]] $|+\rangle$ state for selected circuits. (a) Without readout noise mitigation; (b) with readout noise mitigation [38]. Refer to Table III for circuit details. Error bars show standard deviation.

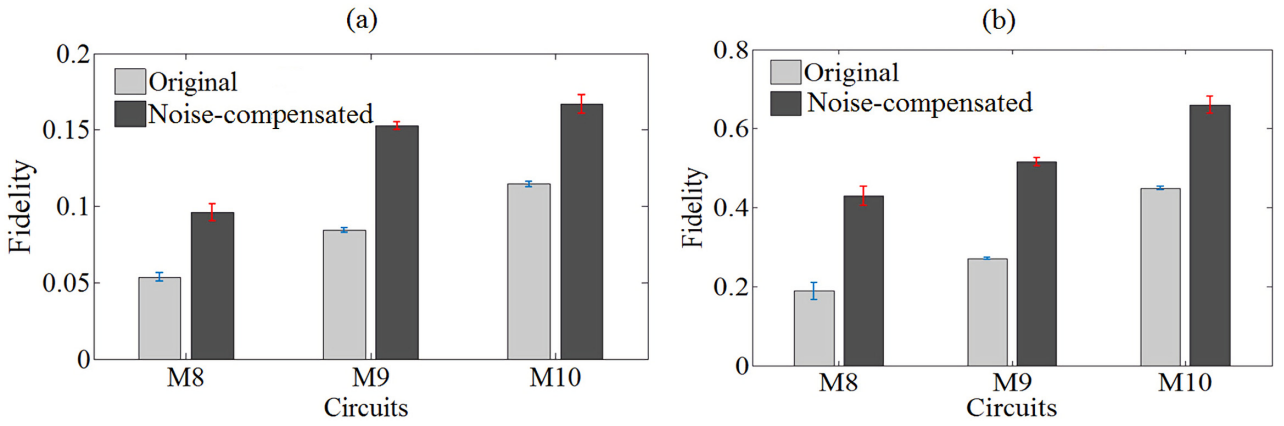



FIG. 9. HCNOT noise correction increases fidelity of the [[7, 1, 3]] $|+\rangle$ state for selected Melbourne circuits. (a) Without readout noise mitigation and (b) with readout noise mitigation [38]. Refer to Table III for the circuit details. Error bars show standard deviation.

The corresponding bit fidelities change only nominally. In the case of a HCNOT gate, this can be slightly higher, for example, up to 4.8%, although it still remains a very small fraction of the corresponding gain in the phase fidelity (see the 32.5% increase for the 15-qubit state). Finally, we observed familiar dips, though somewhat shallower, in the guadalupe circuits phase fidelity curves. In the interest of brevity, detailed analysis has not been included in this paper. The nonstabilizer state results highlight that the proposed scheme can be equally effective in calibrating general quantum circuits entangling almost all qubits on a chip as large as ibmq_guadalupe.

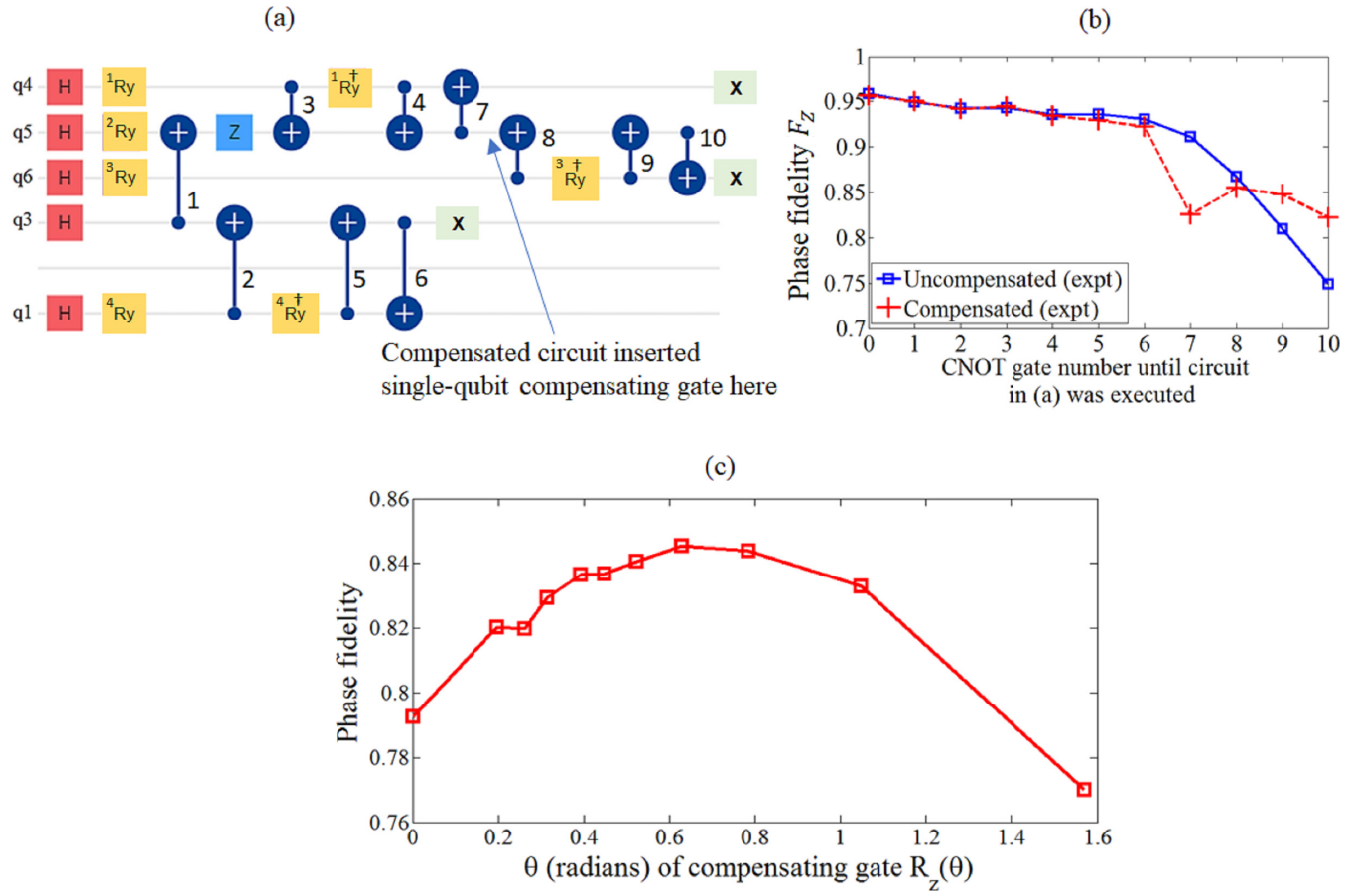



FIG. 10. (a) A five-qubit $X$-basis $W$ state circuit for ibm_perth. The compensated circuit inserted the $R_z(\theta)$ gate with $\theta = -\pi/3$. Note that ${}^1R_y$, ${}^2R_y$, ${}^3R_y$, ${}^4R_y$ (and their conjugates) are rotations about the $y$ axis, with corresponding rotation angles 0.615, 1.37, $\pi/4$, and $\pi/4$. (b) Phase fidelity profile. The compensated circuit increases phase fidelity by 9% (c) Role of $\theta$ in optimizing phase fidelity of compensated circuit. Optimal $R_z(\theta)$, one that maximizes the phase fidelity, can be obtained by systematically exploring the rotation angle in $[0, \pi/2]$.

**Algorithm 2.** Algorithm of tracing phase fidelity (or bit fidelity)

**Input**: An $m-$qubit quantum circuit C containing $n$ gates, annotated with some valid gate execution order $S = [g_1, g_2, g_3, \ldots, g_n]$
**Output**: Array $F_z$ containing phase-fidelities indexed by the gate in $S$
**for** $i \longleftarrow 1$ to $n$ **do**
  $g_i \longleftarrow S[i]$;
  $|\phi\rangle \longleftarrow$ Simulate ideal C till $g_i$ and compute state vector
  $prob\_prod \longleftarrow 0$
  **for** $k \longleftarrow 0$ to $2^m - 1$ **do**
    $E_k \longleftarrow H|k\rangle\langle k|H$
      ▷ $E_k \longleftarrow |k\rangle\langle k|$ for bit-fidelity
    pSum $\longleftarrow 0$ ; qSum $\longleftarrow 0$
    **repeat**
      Execute C on real device till $g_i$. It will generate noisy quantum state $\rho$
      ▷ Destructively measure $\rho$ in $E_k$ to obtain 0/1 outcome
      outcome $\longleftarrow$ Measure $E_k$ on $\rho$
      pSum $\longleftarrow$ pSum + outcome
        ▷ Destructively measure $|\phi\rangle\langle\phi|$ in $E_k$ to obtain 0/1 outcome
      outcome $\longleftarrow$ Measure $E_k$ on $|\phi\rangle\langle\phi|$
      qSum $\longleftarrow$ qSum + outcome
    **until** $N$ iterations;
    $p[k] := \mathrm{Tr}[E_k\rho] \longleftarrow \mathrm{pSum}/N$
    $q[k] := \mathrm{Tr}[E_k|\psi\rangle\langle\psi|] \longleftarrow \mathrm{qSum}/N$
    $prob\_prod \longleftarrow prob\_prod + \sqrt{p[k]q[k]}$
  **end**
  $F_z[i] \longleftarrow prob\_prod$
**end**

### E. Experiment time of finding the optimal location of the compensatory gate

We ran separate trial experiments for identifying the *best* circuit location to insert a compensating gate(s). All locations corresponding to the original circuit CNOT gates were explored, one at a time, and we selected the one where inserting the compensating gate maximized the overall increase in fidelity. In the case of $R_z(\theta)$, additional trial experiments were required to find optimal $\theta$ [see Fig. 10(c)] as well. This makes the total number of trials scale only linearly with the CNOT gates of the circuit. The last column of Table II lists the total experiment time consumed in searching for the optimal location of the compensating gate [and also $\theta$ in case of $R_z(\theta)$]. The time was obtained from the qiskit job status timeline. One can see that sizing the $W$ state from five to 15 qubits quadruples the number of CNOT gates, at the cost of only 2.2 times increase in the search time. We believe that time complexity can be improved by incorporating deeper insights into the circuit-level errors, possibly with the help of cycle benchmarking.

## V. PREVIOUS WORK

Noise cancellation adds to the repertoire of schemes designed to counter errors in near-term noisy intermediate-scale quantum (NISQ) computers [39]. At the same time, it features *in situ* correction of errors without ancilla overhead—a distinctive attribute in the context of relevant prior work. It can also be instrumental to achieve high-fidelity circuit execution on the generation of low-decoherence quantum processors. For example, many superconductor quantum computing platforms are converging to a heavy hexagonal topology, offering quantum volume as high as 64 [40]. Improved quantum hardware lowers decoherence and amplifies coherent error contribution to state infidelity. Several recent works have explored various forms of noise suppression, prevention, or mitigation that can be broadly characterized as either gate- or circuit-level methods, although such bifurcation may be less crisp in some cases.

Gate-level approaches typically rely on advances in pulse shaping [41], control [42–44], and dynamically corrected gates [8], in some cases adding compensating pulses [20,45] to decouple the principal quantum system state from the environment and cancel unwanted Hamiltonian terms in entangling gate implementation. Recently, dynamic decoupling [19] has been shown to effectively suppress the $Z$-$Z$ crosstalk noise and improving coherence times. Circuit-level noise approaches can be classified as either preprocessing or postprocessing in nature. The former techniques apply hardware calibration data to obtain a noise-aware qubit map and gate schedule [13,15,17,21]. Gate commutation properties [14,24] reduce SWAP gate overhead for a lower gate count to lower accumulated noise. Just-in-time [16] compilation takes fresh calibration into account for generating a low-noise circuit map. Detailed noise characterization and intelligent gate scheduling mitigate crosstalk [12] on 20-qubit IBM quantum processors.

On the other hand, the postprocessing circuit-level schemes modify the probability distribution of the circuit readout results such that the mean value of an observable of our interest becomes more accurate at the cost of increased variance. This can be achieved either by artificially scaling the error rates per gate [22,23] with the help slower execution (zero-noise extrapolation) or by carefully depolarizing [22] the circuit (probabilistic noise cancellation). These postprocessing schemes improve only the estimate of the mean value of an observable mapped to read out the probability distribution, and do not improve the likelihood of obtaining a correct distribution. Error-correction protocols have been shown to address this shortcoming although at the scale of single logical qubit protected by distance-2 [[4, 1, 2]] code [33] as well as distance-3 five-qubit [[5, 1, 3]] [46] and seven-qubit [[7,1, 3]] codes [47]. Very recently, arbitrary error correction for logical state preparation and measurement (SPAM) has been successfully demonstrated for the Steane code, achieving SPAM failure probability of a logical qubit lower than its unprotected (physical) counterpart [47]. In any experimental realization of quantum error correction, high-fidelity encoded state preparation will be a crucial milestone for NISQ processors; a large number of entangling gates can easily gather enough errors to leave subsequent parity checks operation ineffective [48,49]. Therefore, eliminating coherent errors is a prerequisite of successful quantum error correction.

TABLE II. Noise correction improves fidelity of $X$-basis $W$ states prepared on ibm_perth, ibm_lagos, and ibmq_guadalupe. The five-qubit state-preparation circuit is shown in Fig. 10. The last column lists qiskit-provided total experimentation time to find the optimal location (and angle) of the compensating gate that maximizes the net % increase in the fidelity.

| Size of X-basis $W$ state | IBM Quantum device | Total CNOT gates | Overall circuit depth | Phase fidelity | | | Bit fidelity | Compensating gate | Experiment time (sec) to find optimize compensated circuit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Original circuit | Compensated circuit | % increase | % increase | | |
| 5-qubit | Perth | 10 | 15 | 0.782 ± 0.006 | 0.844 ± 0.002 | 7.8 | within ±1 | $R_Z(-\pi/3)$ | 52.2 |
| 7-qubit | Lagos | 16 | 18 | 0.704 ± 0.004 | 0.850 ± 0.005 | 19.7 | within ±1 | $R_Z(-\pi/3)$ | 67.8 |
| 9-qubit(1) | Guadalupe | 22 | 21 | 0.563 ± 0.007 | 0.642 ± 0.006 | 13.7 | within ±1 | $R_Z(-\pi/3)$ | 78.8 |
| 9-qubit(2) | Guadalupe | 22 | 21 | 0.518 ± 0.005 | 0.639 ± 0.004 | 23.2 | −3.12 | HCNOT | 54.1 |
| 11-qubit(1) | Guadalupe | 28 | 21 | 0.517 ± 0.003 | 0.602 ± 0.003 | 17.6 | within ±1 | $R_Z(-2\pi/7)$ | 95.8 |
| 11-qubit(2) | Guadalupe | 28 | 21 | 0.432 ± 0.002 | 0.550 ± 0.002 | 21.4 | within ±1 | HCNOT | 70.2 |
| 13-qubit | Guadalupe | 34 | 24 | 0.359 ± 0.014 | 0.467 ± 0.009 | 29.7 | within ±1 | $R_Z(-\pi/2)$ | 113.2 |
| 15-qubit | Guadalupe | 40 | 26 | 0.215 ± 0.005 | 0.325 ± 0.001 | 33.9 | −4.81 | HCNOT | 113.7 |

## VI. CONCLUSION

Tracing and correcting unitary errors pose a challenging and important problem in state-of-art quantum computing platforms. We experimentally demonstrate unitary noise detection and correction on IBM quantum computing devices. We have shown that coherent errors, such as undesirable $Z$-$Z$ coupling, can be sensitive to the sequence of gates in the physical circuit and cause sudden decrease in fidelity, followed by a recovery trend. Such peculiar behavior is in sharp contrast with a monotonically declining decoherence curve. The depth of the curve valley may indicate the amplitude of coherent noise. Noise tracing requires a number of experiments proportional to the circuit size. Correction inserts compensatory gates that partly cancel unitary errors either directly or indirectly, and both have been shown to work effectively in respective circuits. Detailed experiments highlight overall gain in the fidelity of the [[7, 1, 3]] code $|+\rangle$ state as well as the nonstabilizer $X$-basis $W$ state of different sizes, prepared on various IBM quantum processors with quantum volume 8, 16, and 32.

TABLE III. Details of circuits used in Figs. 8 and 9.

| Circuit | Device | Qubit map Virtual qubit:Physical qubit | Sequence of CNOT (ctr, tar) gates |
|---|---|---|---|
| M1 | Melbourne | 1:3, 2:11, 3:10, 4:2, 5:1, 6:12, 7:4 | (7,1), (6,2), (3,2), (5,4), (4,1), (3,7), (1,4), (6,4), (1,2) |
| M2 | Melbourne | 1:13, 2:1, 3:0, 4:12, 5:11, 6:2, 7:14 | (5,4), (7,1), (3,7), (4,1),(1,4), (6,2), (3,2), (1,2), (6,4) |
| M3 | Melbourne | 1:4, 2:10, 3:9, 4:3, 5:2, 6:11, 7:5 | (5,4), (4,1), (7,1), (1,2), (6,2), (3,2), (3,7), (6,4), (1,4) |
| M4 | Melbourne | 1:2, 2:12, 3:13, 4:3, 5:4, 6:11, 7:1 | (5,4), (3,2), (7,1), (3,7), (6,2), (1,4), (2,1), (4,6) |
| M5 | Melbourne | 1:12, 2:2, 3:1, 4:11, 5:10, 6:3, 7:13 | (7,1), (3,7), (1,4), (3,2), (2,6), (6,2), (5,4), (2,1), (4,6) |
| M6 | Melbourne | 1:9, 2:5, 3:6, 4:10, 5:11, 6:4, 7:8 | (3,2), (6,2), (7,1), (1,4), (5,4), (3,7), (2,1), (4,6) |
| M7 | Melbourne | 1:11, 2:3, 3:2, 4:10, 5:9, 6:4, 7:12 | (7,1), (3,2), (1,4), (6,2), (3,7), (5,4), (2,1), (4,6) |
| M8 | Melbourne | 1:9, 2:5, 3:4, 4:8, 5:7, 6:6, 7:10 | (5,4), (4,1), (7,1), (3,7), (1,2), (6,2), (3,2), (1,4), (6,4) |
| M9 | Melbourne | 1:9, 2:5, 3:6, 4:10, 5:11, 6:4, 7:8 | (3,2), (6,2), (7,1), (1,4), (3,7), (5,4), (4,6), (2,1) |
| M10 | Melbourne | 1:5, 2:9, 3:8, 4:4, 5:3, 6:10, 7:6 | [(5,4), (4,1), (7,1), (3,7), (1,2), (6,2), (3,2), (1,4), (6,4)] |
| J | Jakarta | 1:4, 2:1, 3:0, 4:5, 5:6, 6:2, 7:3 | (7, 2), (3, 2), (2, 6), (6, 2), (5, 4), (4, 1), (4, 7), (1, 4), (7, 4), (4, 1), (2, 7), (4, 7), (7, 4), (4, 7), (2, 3), (3, 2), (2, 7), (2, 3) |
| C | Casablanca | 1:4, 2:1, 3:0, 4:5, 5:6, 6:2, 7:3 | (7, 2), (3, 2), (2, 6), (6, 2), (5, 4), (4, 7), (4, 1), (7, 4), (1, 4), (4, 1), (4, 7), (2, 7), (7, 4), (4, 7), (2, 3), (3, 2), (2, 3), (2, 7) |

Although our case study structures important details of noise behavior, it also unfolds some interesting questions for future work thereby. The presented cancellation approach, a form of circuit-level calibration, has been shown to work for multiqubit entanglement circuits. Is it possible to construct a noise model which can encapsulate circuit-level errors more accurately and predict the performance of similar circuits? Furthermore, the valleys traced by the fidelity curve strongly motivate investigation of the likely connection between non-Markovian noise and coherence revival. Can we use the tools developed in this work to better comprehend the role of non-Markovian noise in dictating the state fidelity? Finally, considering encouraging noise-cancellation results, it is tempting to alter noise composition in favor of more unitary than nonunitary errors. To a certain extent, increasing qubit coherence times and decreasing operational error rates and processor sparse topologies have already changed this composition. However, several unmodeled and unmitigated sources of circuit-level errors expand ample space for quantum circuit engineering.

## ACKNOWLEDGMENTS

The views expressed are those of the authors and do not reflect the official policy or position of IBM or the IBM Quantum team. The authors used ibmq_melbourne (retired), one of the IBM Quantum Canary Processors. They also used the seven-qubit ibmq_casabalanca, ibmq_jakarta, ibm_lagos, ibm_perth, and 16-qubit ibmq_guadalupe. These are IBM Quantum Falcon Processors. The authors also acknowledge the access to advanced services provided by the IBM Quantum researchers program access award.

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*Correction:* A misspelling introduced in the fourth sentence of the abstract during the initial production process has been fixed.