

What Can Sb_2Se_3 Solar Cells Learn from CdTe?

C. H. Don, T. P. Shalvey, and J. D. Major*

Department of Physics, Stephenson Institute for Renewable Energy, University of Liverpool, Liverpool L69 7ZF, United Kingdom



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This article provides an examination of the long-term potential of antimony selenide (Sb_2Se_3) as a leading photovoltaic absorber by considering lessons learned from the developmental route of CdTe. We consider the inherent advantages of Sb_2Se_3 , such as its ability to function efficiently in both substrate and superstrate configurations, its grain boundary tolerance, and wide scope of deposition possibilities. By drawing parallels with the historical evolution of CdTe solar cells, we highlight critical lessons that could guide the optimization of Sb_2Se_3 devices, including the importance of understanding and controlling doping mechanisms, band-gap grading, and device structure on performance. We also consider the feasibility of adapting existing CdTe production capabilities for Sb_2Se_3 fabrication, which could potentially lead to reduced production costs and shorter energy payback times. Despite the challenges and uncertainties that lie ahead, we argue that the promise shown by Sb_2Se_3 warrants significant research and development efforts, with the view of making it a viable contender in the solar industry.

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I. INTRODUCTION

As Sb_2Se_3 approaches a decade of meaningful research as a notable thin-film solar cell material, it is worthwhile to make a comparison with the standard bearer of thin-film photovoltaics (PVs), cadmium telluride. With an approximate 5% market share [1], CdTe solar cells have become the primary industrially established competitor to silicon-based modules. CdTe was not, however, an overnight success, experiencing the same gradual development curves as numerous other technologies and particularly pronounced “plateau” periods where efficiencies stagnated. After a period of rapid development caused by the advent of the chloride treatment process and Cu doping, which occurred in the 1980s and 1990s, CdTe solar cell research in the early part of this century became fixated on particular tropes in research. The primary focus during this period was on the CdS window layer [2], chloride treatment optimization [3,4], and back contacting featuring Cu doping [5]. The entire field seemed to have deviated down a relative dead end of research, resulting in a performance cap of 16.7% [6] for a decade between 2001 and 2011. Even more strikingly, the record efficiency was 15.8% as far back as 1993 [7], meaning 18 years’ worth of research

effort yielded 0.9% in improvements. Following the development of a Se-graded device design and alternate partner layers, the technology evolved, and the next 4 years saw progress from 16.7% to 22.1% [6,8]. However, the technology again stalled until recently when a new 22.3% record was provisionally announced [9], seemingly due to progress in group V doping.

In comparison, Sb_2Se_3 , and the related ternary sulfoselenide $\text{Sb}_2(\text{S}, \text{Se})_3$, is a relatively recent addition. It has attracted significant interest due to its relative abundance and the low toxicity of the material, coupled with a nanoribbon grain structure offering the potential for grain boundary tolerance [10,11]. It may however be the material’s supremely high absorption coefficient of $>10^5 \text{ cm}^{-1}$ in the visible spectrum [12,13] that becomes the key benefit longer term. This allows submicron absorber thicknesses to be used, which CdTe cannot match [14], and could ultimately translate to lower material usage and higher production speeds. Although it had been a known absorber material for a number of years, work from Choi *et al.* in 2014 [15] presented the first really notable efficiency of 3.2%, which precipitated greater research uptake. Efficiencies have since steadily increased to 10.6% for Sb_2Se_3 [16] and $>10.7\%$ for the $\text{Sb}_2(\text{S}, \text{Se})_3$ alloy [17,18]. As yet, we have seen no similar plateau periods in development, but there is certainly a slowing of development, with 10% having been achieved in 2020 [19]. This means that, in the 7-year period 2013–2020, the power conversion efficiency (PCE) went from 3% to 10% but only increased by 0.7% in the next 3 years. Are we in danger of hitting one of these technological barriers for this material

*jon.major@liverpool.ac.uk

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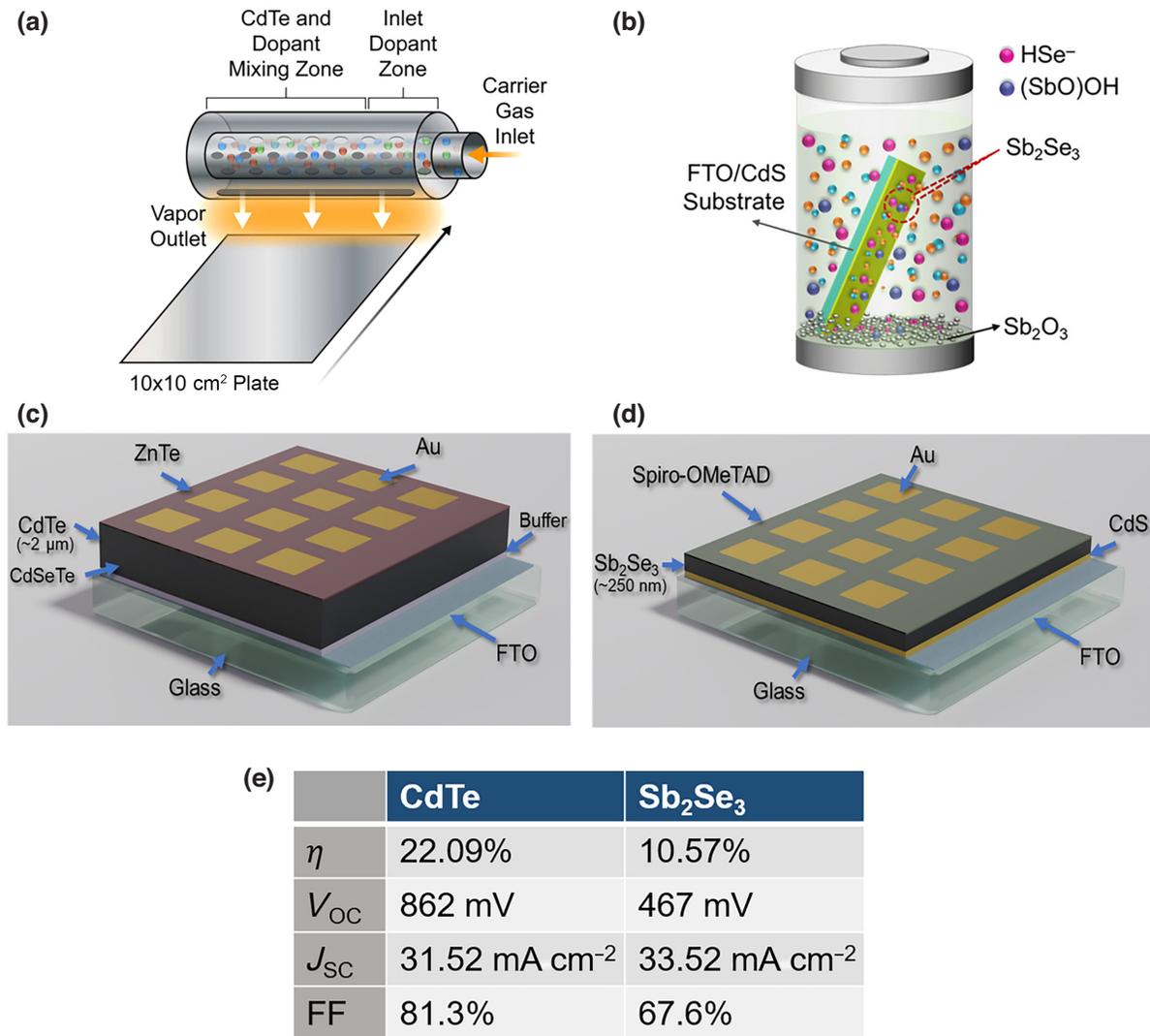


FIG. 1. Record reported devices for CdTe and Sb₂Se₃ showing absorber deposition methods used: (a) CdTe vapor transport deposition, (b) hydrothermal solution deposition of Sb₂Se₃; (c),(d) layer structures used; (e) record performance parameters of each device type. Reproduced from Refs. [8,16,19–22].

and what are the logical next steps to take? Currently, the research field is disparate, focusing on a variety of different deposition approaches and device structures, making consensus hard to come by. The intention with this article is to use the successes and pitfalls of CdTe as a technology to identify routes through which antimony chalcogenide absorbers may achieve comparable success in the long term. There is a logical basis for making a comparison between CdTe and Sb₂Se₃, as they share a great deal of connective tissue. Both are simple inorganic binaries, both often feature similar superstrate device structures, and both have been produced using similar industrially scalable techniques, such as vapor transport deposition (VTD), sputtering, and close space sublimation (CSS). Both have also gradually morphed towards ternary structures capable of graded band-gap approaches via Sb₂(S, Se)₃

and CdSe_{1-x}Te_x (CST). The current state of the art device structures are shown in Fig. 1, along with the deposition methods used for respective absorber layers and the champion cell performance parameters.

This Perspective compares the current state of the art for CdTe and Sb₂Se₃ technologies. Using the historical development of CdTe as a reference, we aim to pinpoint potential improvements in Sb₂Se₃, determine the research field's focus, and set realistic targets.

II. CHOOSING SIDES: COMPARING SUPERSTRATE AND SUBSTRATE GEOMETRIES

A significant distinguishing feature of Sb₂Se₃, compared to CdTe, is its effectiveness in both superstrate [19,22–24] [transparent conductive oxide

(TCO) first] and substrate [25–27] (TCO last) configurations, as shown in Fig. 2. The current champion superstrate device, shown in Fig. 1(d), has a cell structure of glass/ $\text{SnO}_2\text{:F}$ / CdS / Sb_2Se_3 /Spiro/Au and an efficiency of 10.5% [16]. The highest performance inverted substrate device reported has a much changed cell structure of glass/ Mo / MoSe_2 / Sb_2Se_3 / CdS / ZnO / ZnO:Al but still achieves an efficiency of 10.1% [28]. CdTe research has become almost entirely focused on the superstrate device structure. While CdTe has been tested in substrate orientation multiple times, owing to its high electron affinity, creating an ohmic back contact to CdTe has proven to be an enduring challenge [5,29]. This is true even for superstrate devices where the back surface is freely accessible, so for a substrate where the contact must self-form and remain stable during subsequent CdTe deposition and processing [30,31], it has become a seemingly insurmountable task. As a result of these contact and processing difficulties, substrate-CdTe devices have never exceeded an efficiency of 13.6% [32], leading to a near complete decline of research efforts in this area. Most other inorganic thin-film absorbers, such as $\text{Cu}_2\text{ZnSnS}_4$ (CZTS) and $\text{CuIn}_x\text{Ga}_{(1-x)}\text{Se}_2$ (CIGS), do perform optimally in substrate geometry, however, largely due to the requirements for postgrowth sulfurization or selenization processes or the impact of Cu migration into underlayers [33]. Notably, antimony chalcogenide absorbers stand apart from typical inorganic absorbers due to their capacity to function in both orientations. This distinctive characteristic offers the significant advantage of bridging the divide between the substrate and superstrate research factions of inorganic PVs. As a result, there has been a growing trend towards collaborative research among researchers from CdTe, CIGS, and CZTS backgrounds, working together on a single material that incorporates their collective expertise. This broadened pool of talent not only accelerates material development but also provides additional benefits of the two-structure approach. For instance, altering the under- or overlayers in either structure significantly expands processing options, with the material potentially

withstanding harsher processing in one orientation over the other. A prime example is postgrowth annealing, where selenization of a substrate device has led to significant improvements in V_{OC} [34]. However, applying similar postgrowth annealing to superstrate geometry can generate similar V_{OC} gains but ultimately result in reduced performance [35]. The ability to switch between device stack orientations also offers opportunities to examine various aspects of cell structures in a device-relevant manner. For CdTe superstrate devices, the p - n junction is typically buried beneath microns of CdTe, making its characterization a complex process that requires lift-off [36], etched bevels [37,38], or the creation of special nondevice structures for analysis. Such approaches can fundamentally alter the interface's nature, diluting its device relevance. The reverse is true for substrate devices, where back-contact interfaces become challenging to access. The high performance of Sb_2Se_3 in both cell orientations allows for a more comprehensive understanding of the entire device structure than is possible with CdTe, particularly at the main junction interface. Even now, our understanding of CdTe devices remains incomplete due to difficulties in accessing a device-relevant interface. The development process has often been empirical, guided by the principle “if the performance increases, then the interface must have improved.” This approach is not a criticism, but rather a pragmatic response to structural limitations. However, Sb_2Se_3 offers the potential for a more refined methodology. The substrate geometry allows for direct characterization of the interface in high-functioning devices, providing an analysis that directly correlates interface modifications with performance. This approach could provide guidance for superstrate devices, which, in contrast, has an easily accessible back interface, which could aid in the development of substrate cells.

Researchers, regardless of their background or preferred cell orientation, should consider how alternative structures can provide insights for each other. While CdTe has been isolated on a superstrate island, Sb_2Se_3 possesses the potential to circumvent this predicament.

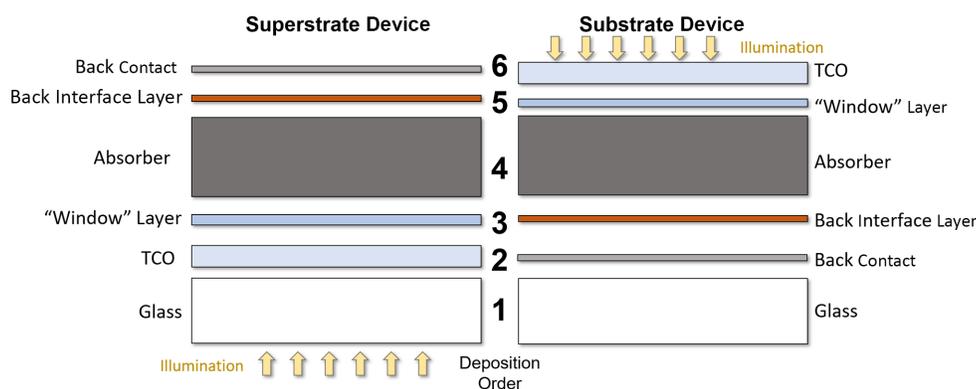


FIG. 2. Schematic diagram showing deposition order of typical device layers and orientation with respect to illumination for superstrate and substrate cell architectures.

III. SEEKING THE IDEAL MATCH: IDENTIFYING SUITABLE PARTNER LAYERS

Continuing from the previous discussion, we can explore why CdTe solar cells have clung to CdS as the *n*-type “window” layer of choice longer than was prudent, and why Sb₂Se₃ devices display a similar reluctance to change. CdS appears to be a universally appealing option across all thin-film inorganic technologies due to its functional reliability. Regardless of your absorber or CdS deposition technique—be it chemical bath deposition (CBD), sputtering, CSS, spray pyrolysis, electrodeposition, or any other method [2,39–41]—CdS has the happy knack of “working.” In part, this is because CdS has the helpful characteristic of exclusively forming as CdS, without any secondary phase issues or structural variation, and reliably high *n*-type doping. As a result, it is the most commonly used *n*-type layer across the dominant inorganic thin-film technologies based on CdTe, Sb₂Se₃, CZTS, and CIGS. However, CdS’s disadvantages are equally well-known. Despite its relative stability, it does contain cadmium, which brings with it associated health and environmental concerns. For CdTe devices, this just adds more cadmium, although the Cd-contamination risks are generally overstated [42–44]. For antimony chalcogenide materials though, the presence of CdS and the introduction of cadmium could be viewed as superfluous. Primarily, however, its 2.4 eV band gap is simply too low for an ideal window layer, leading to the loss of a vital few mA of current by blocking part of the useful spectrum. This can be observed in the external quantum efficiency curves of either CdTe or Sb₂Se₃ devices, where collection below 525 nm is compromised by absorption by CdS, which, due to the one-sided depletion region, correlates directly with current loss [45–47]. Prior to the evolution away from CdS layers, much of the CdTe device work aimed to minimize its negative impacts. The most straightforward strategy was to make the CdS layer as thin as possible, typically this was still found to be around 100 nm before losses in V_{OC} and fill factor occurred. An alternative approach was the adoption of a bilayer, which involved higher-band-gap oxide “buffer” layers, such as ZnO or SnO₂, being placed beneath the CdS [48–50] (it should be noted that there is a cross-platform nomenclature issue here; in CIGS and CZTS circles, the buffer would typically refer to the CdS layer itself). This buffer layer allowed the CdS layer to be further thinned by providing an additional barrier to the underlying TCO [51], while also improving band alignment at the interface [52]. CdS was eventually removed entirely and wider-band-gap oxides became the premier window layer for CdTe, but this required considerable research efforts due to the less straightforward functionality compared to CdS. CdS/CdTe was initially considered the optimal pairing due to S/Te interdiffusion at the interface, which alleviated strain caused by lattice mismatch [3] and had

implications for defect passivation [53–56]. Much of the subsequent work with oxide window layers first required the development of CdTe_xSe_{1-x} regions (discussed in Sec. IV), as this seemed to serve the same purpose as S-Te interdiffusion and circumvent the strict need for a good lattice match. This enabled the development of higher-band-gap alternative partner layers, such as Mg_{1-x}Zn_xO [57–59], and other oxides, such as SnO₂, which ultimately overcame the current limitations for CdTe and enabled the performance to surpass the previous benchmark of 16.7%.

For Sb₂Se₃, while CdS can be deposited more thinly, thereby minimizing current losses [16] (Fig. 1), there are already a number of direct replacement alternatives reported (Fig. 3). CdS remains the default window layer of choice though for 67% of devices found across the literature ($N = 170$). The reasons for this are unclear because, as mentioned, CdS is clearly an imperfect choice. Like in CdTe devices, it causes avoidable current loss and interdiffusion at the interface can be difficult to control. This is more problematic for higher deposition temperature methods, such as CSS, where the formation of Cd(S, Se) and/or Sb₂(S, Se)₃ regions at the near interface can lead to significant optical losses [47]. For lower temperature deposition methods, such as solution processing or thermal evaporation, interdiffusion does not occur to the same extent. However, even for lower temperature deposition, a defective interface region between CdS and Sb₂Se₃ is still observed [11]. There will also be differing requirements for superstrate and substrate geometry devices, wherein for substrate devices the interdiffusion level will be determined by the window layer deposition. This may make some alternatives to CdS unsuitable for substrate devices if high deposition temperatures are required. SnO₂ and ZnO have been investigated as alternatives to CdS and achieved reasonable performance levels [60,61] but do not seem to have been widely deployed. A number of groups have reported TiO₂ based devices [62–65], a window layer well-known from organic and CH₃NH₃PbI₃ (MAPI) perovskite materials to be capable of producing supremely high efficiency cells. It is unclear why TiO₂ has not been more widely used, but it is known to have a degree of process sensitivity that CdS does not, where if the phase and crystallinity of TiO₂ are not carefully controlled, this can lead to performance loss [65]. There is also the more practical possibility that a number of inorganic groups now working on Sb₂Se₃ have established CdS processes, but not alternative materials, such as TiO₂. Nevertheless, with a TiO₂/Sb₂(S, Se)₃ heterojunction device already exceeding 9% efficiency [66] [despite receiving relatively little research effort, Fig. 3(a)], there is clearly an opportunity for Sb₂Se₃ to learn from the development timeline of CdTe. CdS should not be persisted with as a window layer simply because of its ease, as it will always be an unnecessary limit to performance. This point is highlighted in Fig. 3(c) where TiO₂ window layer Sb₂Se₃ devices consistently

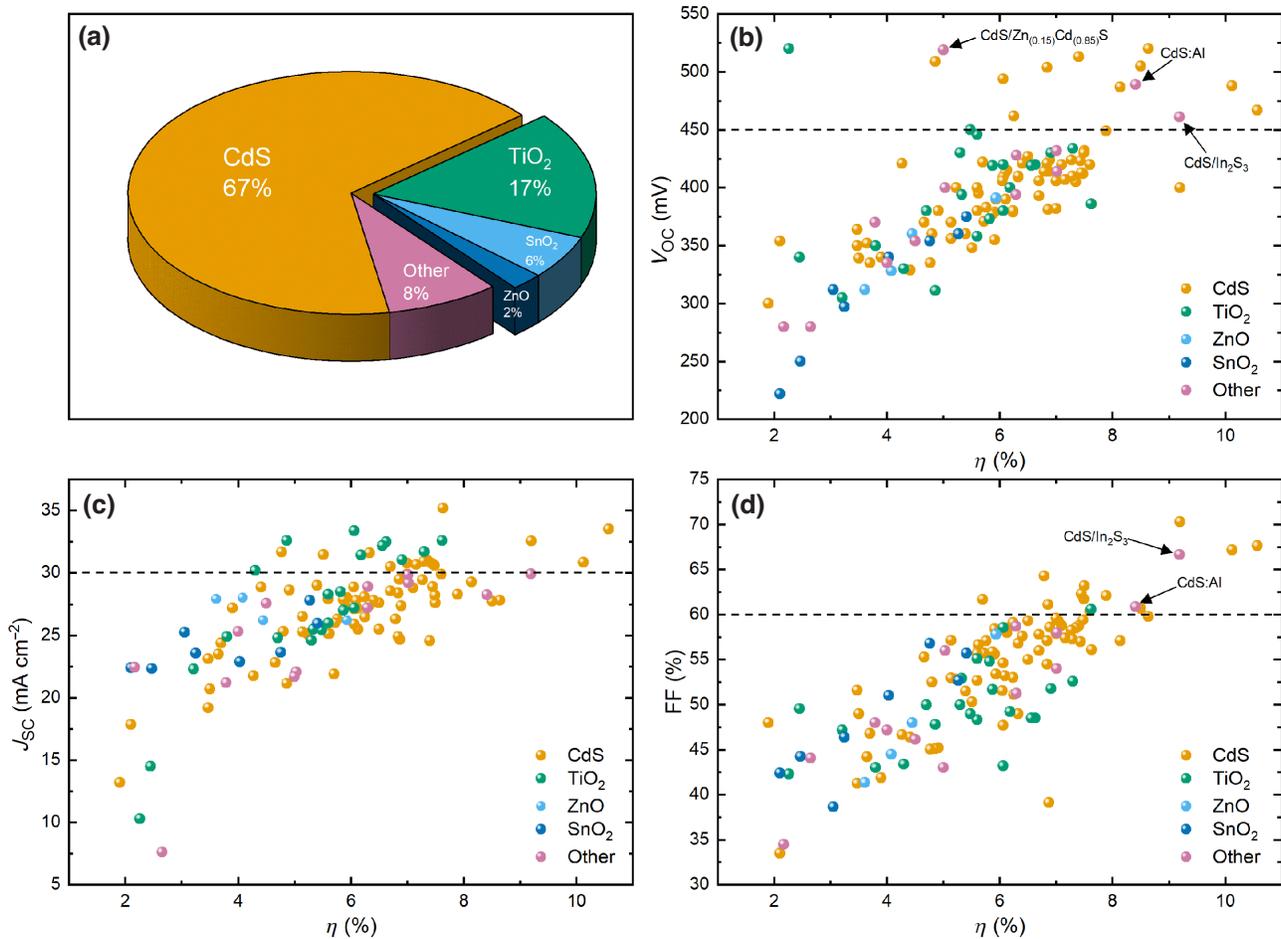


FIG. 3. (a) Percentage of $\text{Sb}_2(\text{S,Se})_3$ devices with each partner layer ($N = 170$); Sb_2Se_3 device performance results for (b) V_{OC} ; (c) J_{SC} ; (d) FF as a function of PCE found in the literature for various junction partner layers.

achieve about 32 mA cm^{-2} , which is approaching the theoretical limit (40 mA cm^{-2} for a 1.18 eV band gap under AM1.5) after accounting for optical transmission losses through the substrate.

While it appears from Fig. 3(b) that a CdS junction interface offers an inherent V_{OC} advantage, looking at the 14 devices $>450 \text{ mV}$, ten of these are in a substrate geometry that enables postgrowth selenization treatments, as mentioned previously. It remains to be seen whether substrate-oriented devices can be fabricated with wider-band-gap partner layers, or whether postgrowth treatments can be applied to stable nondiffusing heterojunctions, to effectively achieve the best of both worlds. The alternatives to CdS explored thus far are by no means the perfect solution, but fortunately there are a vast array of wide-band-gap metal oxide partner layers that can be explored. Their implementation may be more difficult than for CdS but CdTe has already shown us that removal of CdS is a key developmental step.

At the other side of the device, it is briefly worth considering the back-contact layer of choice for Sb_2Se_3 , although

this seems a fairly limited issue. The current champion device uses an organic contact interface layer of Spiro-OMeTAD ($\text{C}_{81}\text{H}_{68}\text{N}_4\text{O}$) [16] [Fig. 1(d)], popular with perovskite materials. This could be potentially problematic in the long term though for production due to high costs and potential stability issues. Unlike CdTe, which has perennially struggled with back-contacting issues, Sb_2Se_3 seems to have no such troubles. A wide range of effective contact layers have already reported, from simple metals, with or without etching [67], to multiple organics [23], various oxides [68], and even PbS [69]. Ultimately, if Sb_2Se_3 makes it to production, there will be a plethora of candidate materials such that the back contact of choice will likely be determined as much by the deposition method and stability as by performance.

IV. A GRADUAL DECLINE: MIXED PHASE ABSORBERS AND BAND-GAP GRADING

As alluded to in Sec. III, a key innovation that fostered the evolution of CdTe technology was the introduction of Se to produce $\text{CdTe}_x\text{Se}_{1-x}$ or CST regions. As well as

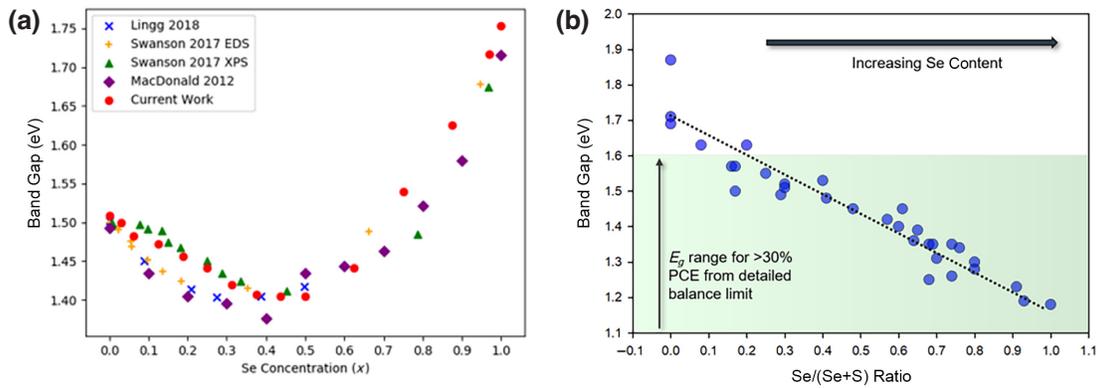


FIG. 4. (a) Band gap variation of zinc blende CST calculated by DFT (red) compared to experimental values of $\text{CdTe}_{1-x}\text{Se}_x$ and (b) $\text{Sb}_2(\text{S,Se})_3$ band gap energy dependence on the $\text{Se}/(\text{Se} + \text{S})$ ratio reported from various deposition methods. Reproduced from Refs. [74,75].

allowing the CdS layer to be removed, due to the band bowing effect, as shown in Fig. 4(a), and the high degree of Se solubility in CdTe, CST enabled the production of lower-band-gap regions and extended the spectral collection range [70–73]. This approach was first considered as simply a method for reducing the absorber’s band gap. While this was initially perceived as interesting, it was not considered particularly revolutionary, given the CdTe band gap was already nearly optimal. The inclusion of Se has proved to be instrumental in advancing the technology, offering a host of additional benefits. Owing to the higher degree of intermixing, and the subsequent relief of interfacial strain due to lattice mismatch, Se incorporation facilitated the elimination of the CdS layer. This was partly necessary due to S/Se interdiffusion causing interfacial complications [76], but primarily due to strain relaxation allowing the use of simple stable high-band-gap oxide layers, which yielded higher currents [76–78]. Moreover, Se has also been demonstrated to passivate grain boundaries and grain interiors of CdTe/CST [38,79], yielding higher minority carrier lifetimes with a fourfold increase and a lifetime of >20 ns being reported for CST [80,81]. This was underscored by recent work, which showed that smaller grained thermally evaporated CST performed to similarly high levels as larger grained CSS material [82]. This runs counter to CdTe only devices, where, due to grain boundary limitations, larger grained material is strongly correlated with increased performance [83]. For CST, it is presumed that smaller grained material is beneficial due to more effective Se incorporation into grain interiors following grain boundary diffusion. CST layers have been fabricated in high efficiency devices either via cosublimation [8,84] from CdSe and CdTe sources or from sequential deposition and interdiffusion to form the desired phase [76,82]. While both are effective, the dual deposition approach seems favorable due to the propensity for void formation in sequential deposition approaches [56,85]. The

sequential deposition route is more widespread though, due to the lack of dual deposition capability in the majority of CdTe research labs.

For Sb_2Se_3 devices, we can envisage analogous strategies involving Sb_2S_3 and $\text{Sb}_2(\text{S,Se})_3$, where a composition gradient from Se to S allows the band gap to be adjusted from 1.18 to 1.70 eV [12,86], although without the same apparent band bowing of CST, as shown in Fig. 4(b). In the simplest terms, it is possible to transition to a more optimal 1.4–1.5 eV range for AM1.5 applications by selecting the appropriate mixed phase [87,88]. In a broad sense, we can expect a wider band gap to lead to increased V_{OC} but at the expense of some current loss. A deeper understanding of how the mixed S/Se absorbers behave compared to the pure selenide or sulfide phases should also be developed. It will be key to understand if there are any phase segregation issues and if there are any defect passivation benefits of mixed S/Se similar to that observed for CST. The more intriguing possibility is to create graded band-gap structures for $\text{Sb}_2(\text{S,Se})_3$ by tailoring the S/Se composition similar to the CST approach. This should be relatively simple due to the similarity of the lattice structures, certainly compared to wurtzite versus zincblende mix for CdSe and CdTe. There have been some reports on band-gap grading approaches for $\text{Sb}_2(\text{S,Se})_3$ [89–91], but the optimal degree of grading achieved and its impact on carrier transport remain uncertain at this point. Certainly, there is also a body of literature from other fields, such as CIGS, to demonstrate that careful control of band-gap grading can lead to enhanced performance by mechanisms such as improved interfacial band alignment [92]. There is also the possibility to develop back reflector structures, such as those deployed in silicon and, albeit thus far unsuccessfully, trialed in CdTe to further improve carrier lifetimes [93].

Reflecting on the CdTe experience with CST and considering the opportunities provided by transitioning to

an $\text{Sb}_2(\text{S},\text{Se})_3$ mixed phase, researchers should aim to accomplish several objectives. First, it is important to reevaluate established window layers for mixed phases. Window layers that have been previously trialed and deemed inferior for Sb_2Se_3 may need reconsideration for $\text{Sb}_2(\text{S},\text{Se})_3$ due to shifts in interfacial band alignments and changes in interdiffusion rates. Second, assessing the defect content is necessary. A study by Tang *et al.* [19] suggested that the shift from selenide to sulfoselenide was associated with a reduction in active defect content. Although the broad fitting of deep level transient spectroscopy (DLTS) peaks makes it challenging to state this with certainty, it is worth investigating whether the mixed phases provide additional defect passivation, akin to what is seen in CST. This exploration is particularly important given the large defect content and large V_{OC} deficit known to exist in these materials [94] and the complexity of the defect formation energies [95] (Fig. 5).

Lastly, the grading approach should be considered. Established CST devices now have well-defined band-gap grading approaches, with a lower band gap at the near interfacial region leading to improved performance. On the other hand, CIGS devices have a more nuanced V-shaped interface. Intuitively, a similar approach could be beneficial for a sulfoselenide device, with an Sb_2Se_3 region at the front interface graded to a mixed phase at the back.

However, this is by no means guaranteed to be the optimal structure, and other approaches, such as back reflectors, also warrant consideration. Also, given the wide variety of deposition approaches and device structures being deployed, the degree of phase control attainable will likely be highly dependent on the particular fabrication approach. Certain device architectures may find particular limits, such as unintended interdiffusion with partner layers, that provide restrictions, i.e., substrate and superstrate devices may behave significantly differently. In any case, a careful analysis to compare the impact of various band structures on material properties and, ultimately, device performance is a key area for future research.

V. EMBRACE YOUR DEFECTS: DEFECT PASSIVATION AND DOPING APPROACHES

CdTe is typically lowly doped when relying on native defects. V_{Cd} has been identified to act as a poor-quality deep acceptor level [96], but the material in its nascent state is plagued by dominant recombination centers, such as the Te_{Cd} antisites, which severely limit the bulk carrier lifetime [97], as shown in Figs. 5(a) and 5(b). Effective doping for CdTe is reliant on extrinsic doping, as well as chloride defect passivation treatment, and has experienced a significant transformation in the past decade. The principal approach had been, and to some extent still is, doping using copper via the Cu_{Cd} level, which has been measured to be anywhere from 0.15 to

0.35 eV above the valence band maximum (VBM) [96]. This is usually accomplished *ex situ* via in-diffusion postdeposition from a very thin film (<15 nm) [98,99] of Cu or a Cu-containing solution, such as CuCl_2 [100]. This *ex situ* approach is necessary due to the issue of rapid Cu diffusion in CdTe and its tendency to introduce defects in CdS or accumulate at interfaces [98]. This in essence necessitates the postgrowth doping approach to attain an appropriate level of control. The inclusion of additional back surface layers, such as ZnTe [101,102], has become the established route to counter Cu migration and ensure the long-term stability of CdTe modules. While performance surpassed 22%, doping levels remained capped at $<10^{15} \text{ cm}^{-3}$, and there were suggestions of problematic Cu-related defect states [99,103,104]. More recently, focus has shifted from postgrowth Cu doping to pregrowth or *in situ* doping using group V elements like Sb, P, and in particular As, which has been shown to form shallower acceptor levels (<100 meV above VBM) via the As_{Te} center [105,106]. While As doping had been established for a while in thin films via metal-organic chemical vapor deposition [107], a number of subsequent more fundamental studies on single crystals [108,109] ultimately drove the development process. This has enabled doping densities to exceed 10^{18} cm^{-3} [105,110,111], as there is a lower likelihood of compensating for deep defect states forming in comparison to Cu-doped material [112]. This has now led to equivalent efficiencies of >22% being reported from a noncommercial laboratory via an *in situ* doping process [8], albeit with a higher doping density. Although this method is ultimately likely to be more effective, it certainly presents a more technologically challenging route than the relative simplicity of Cu doping. Most research laboratories have the ability to undertake postdeposition Cu doping, but the group V doping approaches established thus far require more bespoke equipment.

In comparison, it is fair to say the exact doping mechanism in Sb_2Se_3 is still a subject of debate. Often, the material is assumed to be *p* type, with intrinsic defects acting as the primary source of doping. However, given the complex defect chemistry of the material [95], as shown in Figs. 5(c) and 5(d), and with no obvious shallow *p*-type doping center, this may not be the case. The possibility exists that uncontrolled extrinsic impurities could be contributing to doping. For full transparency, our research group has worked with *n*-type Sb_2Se_3 absorber layers for a number of years [113], though not intentionally. We initially presumed, like many, that Sb_2Se_3 was *p* type, as, following years of CdTe experience, we were wedded to the concept of a *p-n* junction. However, after some unusual signals during DLTS analysis, we were eventually able to identify that the material produced was in fact *n* type. Further analysis via secondary ion mass spectrometry and comparison with single crystals enabled us to identify chlorine impurities in the feedstock Sb_2Se_3 ,

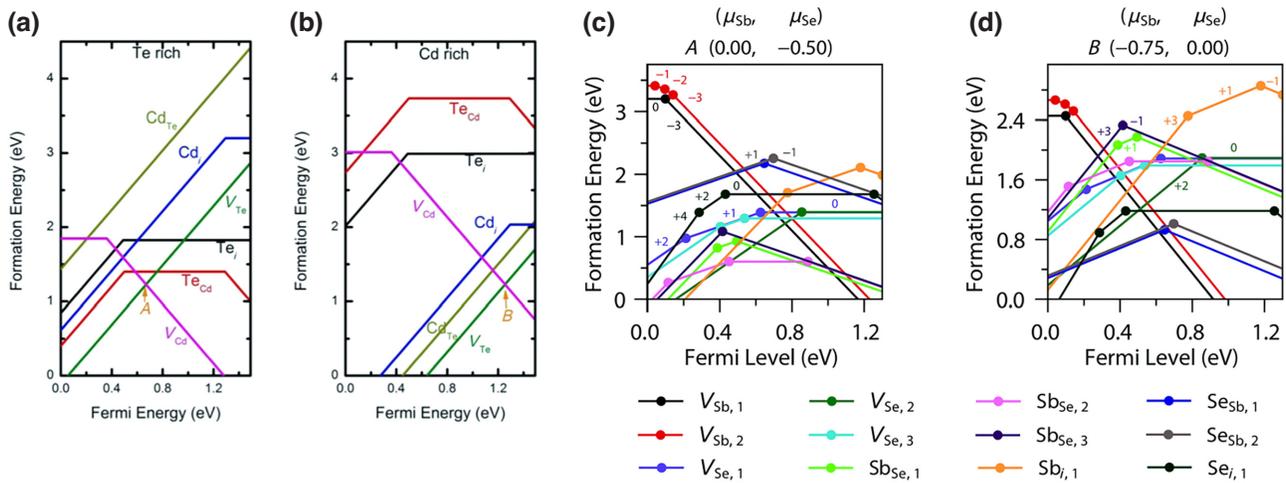


FIG. 5. Comparing and contrasting the complexity of defect formation chemistry in CdTe and Sb_2Se_3 . Density functional theory calculated defect formation energy values (eV) against position of the Fermi level above the valence band maximum for native defects in CdTe under (a) Te-rich and (b) Cd-rich conditions with Sb_2Se_3 under (c) Sb-rich and (d) Se-rich limiting chemical potential conditions. Reproduced from Refs. [95,96].

which were causing the n -type doping [113]. Determining an unknown carrier type in a polycrystalline material is surprisingly complex and may be a broader issue within the field than is appreciated. In creating a device structure, a p - n junction is commonly assumed, but an n - n^+ isotype junction is indistinguishable under normal operation. A typical capacitance-voltage method also only identifies expansion or contraction of the depletion region and does not actually distinguish between p - and n -type absorbers. Similarly, standard Hall effect systems struggle, in general, with relatively lowly doped polycrystalline materials, so most Sb_2Se_3 is unmeasurable. Consequently, unintended n -type doping could be occurring in various processes misidentified as p -type dopants. Alternatively, there could similarly be unintended p -type dopants present within the material. Without definitive characterization to identify the carrier type, caution is advisable in making assumptions in this regard. Given that doping densities of up to 10^{17} cm^{-3} are regularly reported, it is also challenging to argue for sufficient p -type, or indeed n -type, doping occurring from native defects [95]. Ultimately, a highly doped p -type absorber is preferable, and the field should adopt the approach CdTe has latterly arrived at to achieve greater control of both intended and unintended extrinsic dopants. In this regard, there have been a number of different reports on attempted p -type doping approaches for Sb_2Se_3 , utilizing a range of materials, such as Sn, Cu, Pb, Fe, or I [114–118], to varying degrees of success. For the most part, and for obvious reasons, at present, the field lacks the maturity of the CdTe group V approach. A more considered materials first approach, exploring a broad range of dopants, but with a focus on establishing the activation fraction and defect formation, would be beneficial.

There have been very few reports on single-crystal device work, possibly due to the challenging nature of avoiding needlelike growth, and where single-crystal device work has been reported, the performance is essentially negligible [119]. Rather than concentrating on postgrowth processing routes to introduce dopants, gaining control of dopants in the material at the source or *in situ* seems more effective but technically challenging. This is particularly important because the material does not seem to withstand particularly high postgrowth treatment temperatures, limiting the range and scope of materials that could be incorporated.

An important and related point is that the process of doping in CdTe is almost secondary to the passivation of grain boundary defect states using chlorine. Chlorine was initially believed to contribute to p -type doping via the formation of an A center [120], but the dominant influence now appears to be accepted as a grain boundary passivant [3,121–123]. Regardless, without the chloride postgrowth “activation” step, wherein the absorber is annealed in air in the presence of $CdCl_2$ or an alternative chloride [124], cell efficiency typically remains around 1%. The development of the chloride treatment in the early 1980s was instrumental in pushing CdTe to reach 16% efficiency levels. Passivating inherent defect states has thus far had a more significant impact on performance than highly effective doping. This is evident, as even the current state-of-the-art devices, which are doped with group V elements and incorporate Se, still require Cl treatment. In contrast, antimony chalcogenide materials have not yet experienced the consistent performance boosts associated with a “magic bullet” style passivation process that results in significant V_{OC} increases. Instead, as-deposited materials function well, and high-performance devices frequently feature

minimal postgrowth processing. This supports the theory that these materials are more tolerant of grain boundaries than CdTe. However, this is not to imply that there have not been any reports on postgrowth processing improving performance or indeed that V_{OC} is not a limitation. The current champion $\text{Sb}_2(\text{S}, \text{Se})_3$ device utilizes a post-growth alkaline metal fluoride process [17], similar to that deployed for CIGS, which improves the efficiency but not the V_{OC} . Postgrowth annealing or selenization is a logical approach and has been shown to improve performance in some devices [34,125,126]. What is apparent though is that, as yet, there is no postgrowth process that is as ubiquitous or essential as the CdTe chloride process. Whether such a process even exists or is required should be an area of great interest and something that should be considered in parallel with the development of doping techniques, as the two are likely to be highly symbiotic. It is also critical to understand not only how doping modifies the defect content, but also the impact this has on the overall stability of the final device. Careful considerations should also be given to which doping elements, postgrowth process, or contact materials might interact with other device layers adversely as the device structure evolves.

VI. THE COST OF DOING BUSINESS: COULD Sb_2Se_3 COMPETE WITH CdTe INDUSTRIALLY IN THE LONG TERM?

This is, quite literally, the multimillion-dollar question. We must preface this discussion with a hefty caveat: Sb_2Se_3 , despite the significant progress made, is not the first “next big material” to risk not delivering on its early promise and stalling indefinitely. CZTS, for instance, has struggled to capitalize on its initial development, while $\alpha\text{:Si}$ never reached its seemingly high potential. However, it is worthwhile to speculatively consider “if” Sb_2Se_3 lab-scale device efficiencies reached a similar level to that of CdTe, could it transition to industrial implementation and would there be any benefit in doing so?

One of the significant advantages of antimony chalcogenides is that they are the first inorganic absorbers, apart from CdTe, to function to a credible level in the superstrate configuration. This structure, in addition to offering key technological development opportunities, provides a proven credible path to market. To elaborate, it is not a far-fetched notion to conceive of existing CdTe deposition infrastructure being adapted for a Sb_2Se_3 or $\text{Sb}_2(\text{S}, \text{Se})_3$ process. CdTe manufacturing, such as First Solar’s, is based on the use of commercial $\text{SnO}_2\text{:F}$ coated glass with the addition of active layers via various combinations of VTD approaches and sputtering. All of these same techniques have already been shown as viable components of a lab-based Sb_2Se_3 fabrication process. Therefore, it seems plausible to assume they could be similarly

scaled up in the same manner as CdTe was, albeit with a selection of teething troubles to be expected. From a purely practical standpoint, there is therefore reason to believe that a Sb_2Se_3 production line could feasibly be developed. But what would be the benefit of doing so when CdTe is already established? A significant advantage would be a reduction in power required for fabrication and, consequently, energy payback time. Using our own lab-based CSS deposition process, a variation of vapor transport deposition, as an example, CdTe is deposited at source temperatures of around 600–650 °C with the substrate held in the 520–575 °C range [124]. For Sb_2Se_3 deposited in an identical system, these ranges drop to 460–525 and 410–500 °C [113], although the latter can be as low as 350 °C. Furthermore, because of its higher absorption coefficient, the Sb_2Se_3 absorber can be much thinner. The current record Sb_2Se_3 has an absorber thickness of <300 nm, compared to CdTe, which requires >3 μm [8]. This means less power is required for a much shorter duration (assuming equivalent deposition rates), which could potentially save significant fabrication costs, reduce the payback time, or increase production rates.

Material costs are even harder to quantify given economies of scale and other nebulous economic factors, but again we can make ballpark estimates for the purposes of forecasting.

Using the US Geological Survey Mineral Commodity Summaries 2023 [127] as a reliable source of market elemental pricing, we can make broad estimates for raw material costs per kg as a comparative measure. Assuming we fabricate materials from constituent elements gives an estimate of 34.67\$/kg for CdTe compared to only 17.52\$/kg for Sb_2Se_3 , which would drop further for Sb_2S_3 at 5.64\$/kg. This is a significant drop and there is also the abundance factor to consider as well with the crustal abundance for Te being <0.001 ppm with only 440 tonnes of annual global production. This has often been cited as a limitation of CdTe, but it remains to be seen if this is truly an issue in the long term. For comparison, both Sb and Se are orders of magnitude more abundant, at 0.201 and 0.130 ppm, with 140 000 and 2800 tonnes of global production, respectively. Given this and the reduced absorber thicknesses required, it seems safe to project Sb_2Se_3 and $\text{Sb}_2(\text{S}, \text{Se})_3$ as more abundant lower cost raw materials.

To reiterate, the above discussion must be heavily caveated; this is purely projection based on some laboratory experience and raw material costs. What can be said, however, is that all of the above indicate that Sb_2Se_3 has the potential to offer technology that utilizes the same deposition technology as CdTe but based upon a thinner cheaper less CO_2 intensive material. The problem with this, of course, is that for it to be in anyway feasible the technology needs to go from 10% PCE to realistically around 20%. This requires vast concerted research

efforts and even then, it may not get anywhere close to that benchmark due to some as-yet unidentified Achilles heel.

VII. OUTLOOK: MIND THE GAP

Predicting and therefore influencing the developmental arc of solar cell technologies presents significant challenges. As highlighted, CdTe has seen plateaus in its development, whereas the MAPI perovskite developed unencumbered past 20% PCE before stability issues became the more pressing concern when moving towards industrialization. What can Sb_2Se_3 learn from the lived experience of CdTe device development then?

A vital lesson is the importance of choosing optimal material-based developments over convenient options. CdTe research overemphasized Cu doping and CdS window layers because of their reliability and consistency. However, despite their value in device studies, they did not advance the technology. Researchers understood the limitations of both (parasitic absorption of CdS and low or unstable p -type doping from Cu), but developing alternatives necessitated a more complex cell process. The CST band-gap grading approach was developed alongside a transition to oxide window layers to mitigate CdS absorption losses and maximize short circuit currents. The shift towards group V doping required a more sophisticated approach compared to the straightforward postgrowth process for Cu doping. This shift was preceded by extensive single-crystal analysis to comprehend optimal dopants, stability, activation fraction, and defect formation before incorporating into polycrystalline films. This long-term approach was crucial to attain higher doping and lower defect levels needed to improve the absorber material.

In contrast to the united front often seen in CdTe research, Sb_2Se_3 research appears more fragmented. There is currently no consensus on optimal partner layers, doping, postgrowth processing, or even device geometry. This diversity is partly due to researchers from various thin-film technologies now working on Sb_2Se_3 . However, this varied background is also a strength, offering a broader range of process knowledge and encouraging innovative approaches, thus potentially avoiding dead ends in development. Where should we, as a research field, focus our efforts to best advance Sb_2Se_3 then? Addressing the open circuit voltage deficit is the immediate performance issue, as most devices currently exhibit $V_{\text{OC}} < 40\%$ of the band gap [128]. The history of V_{OC} development in CdTe provides somewhat mixed messages to inform an approach for Sb_2Se_3 . The development of an effective defect passivation chloride treatment has allowed CdTe devices to exceed 60% of the band gap at >870 mV [8]. The large caveat here is that, despite significant performance improvements via J_{SC} optimization, devices with a V_{OC} of 850 mV were obtained as far back as 1992 [129]. Essentially, after

initial success with the chloride passivation treatment, little has changed since and a similar roadblock to that experienced by Sb_2Se_3 persists. Single-crystal CdTe devices have shown the ability to attain V_{OC} values in excess of 1.1 V [130,131], giving credence to the belief that the present limit can eventually be overcome.

The challenge of the V_{OC} for Sb_2Se_3 is more multifaceted, as we are starting from a less certain base structure. The dominant loss mechanisms, effective doping approaches, and optimal partner layers all need to be considered in parallel to overcome the V_{OC} limitation. At present, it is difficult to even pin down the exact cause of losses for antimony chalcogenides. Enough different measurement techniques have now been applied to establish that the material certainly contains a large amount of defect levels [94,132,133]. The majority of reported defect measurements have also indicated these are deep within the band gap [134], to the extent we would expect a significant impact on carrier lifetime, and thus, V_{OC} . More worrying is recent analysis suggesting that carrier self-trapping may also occur in these materials [135,136]. This would represent a more fundamental problem, as it is proposed to result from the inherent softness of the material due to the relatively weak inter-ribbon bonding [135]. Unlike native or impurity-related defects, this is incredibly challenging, if not impossible, to engineer out. Self-trapping signatures [135], as well as a high deep level content [94], have been observed for both single crystals and thin films, suggesting problems may indeed be inherent within the material irrespective of form. Unlike for CdTe, Sb_2Se_3 single-crystal device work is highly limited, so there is no evidence to give an upper V_{OC} limit we can realistically attain and there may be a fundamental limit. This pessimism can be tempered somewhat by the fact that there is contradictory evidence from theoretical work [137] and that devices with higher V_{OC} have been reported [27,34]. Also, various postgrowth approaches have been shown to improve V_{OC} [34,35,138], indicating that perhaps there is something that can be done. To address this, further research is needed to fully understand the intricacies of the doping mechanism and source of defect-related limitations in Sb_2Se_3 . Can we pin down what defects are native and what are extrinsic? First, the adoption of a more considered predoping approach with better chemical control, similar to that used in CdTe with the group V dopants [8,139], seems to be a logical step forward. This would allow the activation fraction and defect formation to be disentangled and may shed further light on dominant recombination mechanisms. In parallel to a greater interrogation of defects, there also needs to be a greater understanding developed of how this impacts interfacial band alignment and partner layer selection. If dopant control can be achieved, this will warrant a reevaluation of the suitability of partner layers, as this is intrinsically linked. Linked to this, device stability should be another critical area of focus

as a more efficient but highly unstable device is of little appeal. The inherent stability of Sb₂Se₃ and its resistance to degradation, even when exposed to air [140,141], bodes well for long-term device performance. Further studies are needed to understand how different deposition processes impact this stability and devise strategies to enhance it. This will be particularly important as, if and when, new doping approaches or partner layers are adopted, as this will impact on stability. Definitively establishing the principle limitations for Sb₂Se₃ is a key area of investigation for surmounting the current V_{OC} limit and continue to drive performance improvements.

Looking to the longer term on the manufacturing front and making the large assumption that required performance levels can be reached, the ability to deposit Sb₂Se₃ in both substrate and superstrate configurations opens up valuable technological development opportunities both as module technology and beyond. The feasibility of adapting existing CdTe deposition infrastructure for Sb₂Se₃ production is an exciting prospect, potentially reducing both power consumption and energy payback time, but is not the only option given the vast array of viable deposition approaches established. Sb₂Se₃ and Sb₂(S,Se)₃ have the potential to provide a more adaptable technology given the easy tunability of the band gap and lower deposition temperatures.

CdTe has shown that for thin-film technologies the journey from lab-scale devices to industrial implementation is fraught with potential hurdles but is ultimately possible. The promise shown by Sb₂Se₃ suggests that it is highly worth pursuing this path, given the potential reward for success. Learning from CdTe's evolution offers valuable insights, and it is vital to consider these lessons to avoid repeating past mistakes.

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