Quantum Dynamics for Energetic Advantage in a Charge-Based Classical Full Adder

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We present a proposal for a one-bit full adder to process classical information based on a few electrons in a triple quantum dot system, serving as a proof of principle for the development of energy-efficient information technologies operating through coherent quantum dynamics. The device works via the repeated execution of a Fredkin gate implemented through the dynamics of a single time-independent Hamiltonian. Our proposal uses realistic parameter values and could be implemented on currently available quantum dot architectures. We compare the estimated energetic costs for operating our full adder with those of well-known fully classical devices, and we identify a few important factors for the future success of this technology.

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I. INTRODUCTION

The ever-growing dependence of society on information technologies has led to remarkable developments over the past few decades. Transistor counts in modern processing devices have roughly doubled every 2 years, as empirically described by Moore's law [1,2], accompanied by similar gains in energy efficiency [3]. However, this exponential increase in computing power is reaching its limits, as miniaturization is becoming increasingly challenging due to thermal constraints [4] and the inevitable influence of quantum effects. At the same time, recent efficiency gains have been mostly due to architecture and algorithmic optimizations, while transistor efficiency has mostly stagnated since the early 2000s [3,4]. This combination of factors is leading computationally intensive tasks to take up an increasing amount of the world's energy budget [5], accompanied by a similar growth in their carbon footprint [6]. The energetic cost of information processing has become one of the key challenges to be solved by future generations of information technologies.

Solving these problems may require the development of alternative computing technologies that are both quantum compatible [7,8], and prioritize the use of energy-efficient building blocks. In this work, we explore this idea by using reversible quantum dynamics to perform classical information processing. Three-bit logic gates such as the Fredkin and Toffoli gates are both reversible and universal for classical computation [9] and could act as building blocks for a universal classical machine operating locally through unitary quantum dynamics. The use of logically reversible building blocks opens up the possibility of

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having a reversible computing machine [10,11], thus avoiding the potential source of dissipation associated with bit erasure implied by Landauer's principle [12].

Our proposal is closely related to quantum computation, a field that has grown significantly in the last few decades [13]. To do quantum computation, quantum coherence must be preserved from start to finish, a task that requires the computing device to be well protected from errors, in terms of both isolation from the environment and the robustness of error-correction protocols [14]. While many implementations of small-scale devices and algorithms have been demonstrated [15,16], including some preliminary examples of quantum advantage [17,18], these have been limited to fewer than 100 noisy qubits and small computation depth. With the current race to achieve full-scale quantum computation, the development of these devices has been fast. Nevertheless, scaling up quantum computing systems is proving to be a challenging problem, and we are still very far from achieving the qubit numbers and robustness needed for fault-tolerant quantum computation [19,20]. As a spin-off technology, quantum-based classical computing could prove to be an easier task, differing in two key ways: Firstly, it allows binary logic to be encoded in quantum states that do not necessarily form a *quantum bit*, for example, different charge states in a quantum dot (QD) [21], since there is no need for a coherent superposition of 0 and 1. Secondly, for an extended computation, quantum coherence is required only at the level of each individual gate [22], as the relevant information to be transmitted between gates is entirely classical, and can be limited to computational basis states. Designing energy-efficient quantum-coherent data buses for the transmission of classical data poses also an interesting challenge for quantum-based classical computing, as explored in Ref. [23].

As a first step toward the development of a quantum-based classical computer, and to explore potential energetic advantages, we introduce a proof-of-principle one-bit full adder composed of a sequence of Fredkin gates implemented in semiconductor quantum dots [24] to maximize compatibility with current classical semiconductor technology [25]. Each Fredkin gate is realized by a few electrons evolving coherently under a single time-independent Hamiltonian. Furthermore, we present energetic estimates for our full adder and discuss how these estimates compare with estimates for other proposals.

II. BACKGROUND

The full adder is a basic circuit for addition of binary numbers that can be used to add many-bit numbers when cascaded [26], and it is a crucial piece of a computer's arithmetic and logic unit [27]. Besides their constant use in modern-day electronics, full adders continue to be a focus in semiconductor electronics research [28,29] and alternative computing technologies [30–33], as described next.

A. Semiconductor quantum dots

Semiconductor quantum dots are one of the many platforms currently being explored for quantum information processing, with various qubit proposals [34–37] relying on the manipulation of charge and spin degrees of freedom of only a few electrons, typically allowing these devices to be small and with fast operation times [38,39]. The great development behind the semiconductor industry that supports our modern-day computers is expected to be very advantageous for the development of semiconductor-based quantum processors [25].

Besides the goal of quantum information processing, semiconductor quantum dots have also been used to propose devices for energy-efficient classical information processing based on quantum dot cellular automata (QDCA), which have seen continued development over the last two decades. Early experimental results demonstrated the implementation of single QDCA cells and basic logic gates [40–42], and since then there have been many proposals for more complex operations, namely, full adders [30–33]. To the best of our knowledge, there have been no experimental demonstrations of a working QDCA full adder.

B. Energetics of classical devices

To benchmark the energy efficiency of our proposal, it is useful to briefly review and estimate the energetic costs of classical information processing devices. We consider three types of device: modern supercomputers, research proposals for efficient transistor-based full adders, and research proposals for alternative full adders based on QDCA.

Modern supercomputer benchmarks can be found in the TOP500 project [43], which regularly updates the list of the top-performing and most efficient supercomputers being used commercially. The values provided by this project are measured during the execution of large-scale linear algebra tasks. However, our proposal is still restricted to the addition of single bits, and thus it is not directly comparable to the values obtained from the TOP500 project. Instead, we can use the values therein to get an estimate of the energetic cost per bit operation, as detailed in Sec. I in Supplemental Material [44]. At the time of writing, the estimate for the top-performing supercomputer (Frontier) is 1.19×10^5 eV per bit operation, and the estimate for the most energy-efficient supercomputer (Frontier TDS) is 9.95×10^4 eV per bit operation.

Besides the aforementioned estimates for modern supercomputers, there are also numerous proposals for energy-efficient full-adder designs based on different technologies. Recent comprehensive reviews of semiconductor-based

full adders are provided in Refs. [28,29], with detailed simulations of their power consumption, delay, and power-delay product, which quantifies the total energy spent during one gate operation. Overall, in the proposals analyzed, the power-delay product ranges from 1.8×10^2 to 1.3×10^3 eV for one single-bit addition.

In regard to quantum dot cellular automata, referenced above, simulations of various full-adder designs estimate that their energetic cost could be on the order of 1 eV [32]. However, these designs require dozens of QDCA cells, which is far beyond what has been experimentally demonstrated.

III. A QUANTUM-COHERENT CLASSICAL FULL ADDER

Our proposed full adder is built via the repeated execution of a Fredkin gate based on the coherent dynamics of a triple quantum dot system. We first describe the physical model for the Fredkin gate and then describe the protocol to operate the full adder.

A. Fredkin gate model

The Fredkin gate is a three-bit operation, where the logical states of two target bits are swapped if and only if the control bit is in the 1 state. A truth table for this operation is presented in Table I in Supplemental Material [44]. We encode each logical state into the charge occupancy of a single-level quantum dot, with an empty quantum dot representing the logical state $|1\rangle$ and a charged quantum dot representing the logical state $|0\rangle$. Note that this encoding does not represent a qubit, as no superposition of $|0\rangle$ and $|1\rangle$ can be prepared [21]. Nevertheless, it is sufficient for classical computation. The reverse encoding, with the logical $|0\rangle$ represented by an empty quantum dot, could also be used by appropriate adjustment of each quantum dot's on-site potentials. Furthermore, we note that in our model $|0\rangle$ is encoded in a nondegenerate state with either one or two electrons (or, generally, either odd or even electron numbers). Both cases can be represented by the same Hamiltonian and, in principle, the same physical device can realize any of the encodings. Moreover, the choice of encoding is, in practice, implemented by tuning specific parameters in the Hamiltonian (e.g., the strength of a static, uniform magnetic field) and changing details of the control protocol.

Our discussion regarding the logical encoding is twofold. On the one hand, we wish to present a single device that can be easily implemented with current laboratory techniques to provide motivation for continued research into this topic. On the other hand, we wish to explore ways in which this device can be scaled up into a more complex architecture in the future. The single-electron encoding is certainly more amenable for near-term experimental studies, as single-electron hopping in quantum dots has been widely studied experimentally, and the device can be tuned to perform the transition irrespective of the spin. To make the device scalable, however, it is important that it performs the operation consistently without needing to be tuned on the fly. One way to solve that challenge is by fixing the electrons to be in either the spin-up state or the spin-down state by imposing a uniform static magnetic field to lift spin degeneracy. Another way would be to use a double-electron encoding through a singlet state. This is a more challenging encoding for near-term implementation, and to the best of our knowledge the coherent tunneling of two electrons has not been observed experimentally. Nevertheless, the possibility of scaling up a system without the need for an external magnetic field could be beneficial in the future, and this is the main motivation for also considering it here as a conceptual case.

We start by presenting our model in terms of the two-electron encoding, and we discuss changes resulting from use of the single-electron encoding. The computational basis is thus defined as

$$|0\rangle = c_\uparrow^\dagger c_\downarrow^\dagger |\emptyset\rangle, \qquad |1\rangle = |\emptyset\rangle, \tag{1}$$

where $|\emptyset\rangle$ represents the empty QD, and $c_\sigma^\dagger$ creates an electron with spin σ, either $\uparrow$ or $\downarrow$.

We model our device through a general-form three-site Hubbard Hamiltonian:

$$H_F = \sum_{l\sigma} \varepsilon_l \hat{n}_{l\sigma} + \sum_{\sigma} \Gamma (c_{1\sigma}^\dagger c_{2\sigma} + c_{2\sigma}^\dagger c_{1\sigma}) + \sum_{\sigma\sigma'} V(\hat{n}_{0\sigma}\hat{n}_{1\sigma'} + \hat{n}_{1\sigma}\hat{n}_{2\sigma'}) + \sum_{l} U_l \hat{n}_{l\uparrow}\hat{n}_{l\downarrow}, \tag{2}$$

where $l = 0$, 1, or 2 is the index of each quantum dot, ε_l is the single-particle energy of quantum dot l (QD1), Γ is the tunnel coupling between QD1 and QD2, U is the charging energy of each quantum dot, which we consider equal for simplicity, and V is the capacitive coupling between nearest-neighbor quantum dots. We use the operators $c_\sigma^\dagger$ (c_σ) for the creation (annihilation) of an electron with spin σ, and we define the number operators as $\hat{n}_{l\sigma} = c_{l\sigma}^\dagger c_{l\sigma}$. We present a schematic of the triple quantum dot system in Fig. 1(a). Several experimental studies have demonstrated that, by tuning the control gate voltages, it is possible to tune the parameters of quantum dot arrays for specific purposes [45–47]. We further discuss experimental details in Sec. II E in Supplemental Material [44,48].

A complete analysis of the dynamics implemented by Eq. (2), including the effects of quasistatic and high-frequency noise, is presented in Sec. II in Supplemental

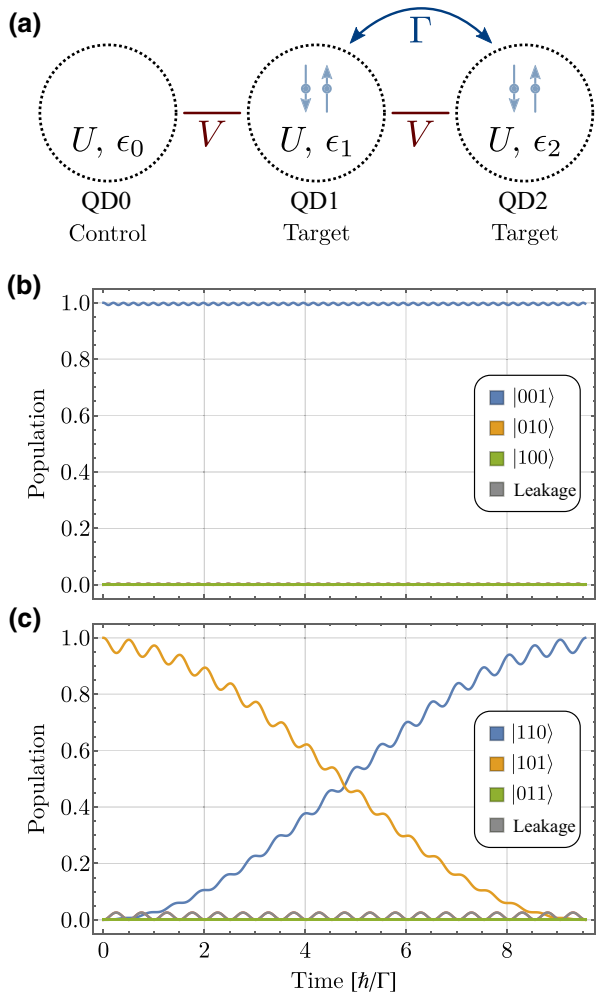

FIG. 1. Fredkin gate dynamics. (a) Interactions represented by the Hamiltonian in Eq. (2). By default, we consider the energy levels of QD1 and QD2 to be tuned at resonance ($\varepsilon_1 = \varepsilon_2$), allowing the tunneling of electrons. The presence of electrons in QD0 translates to a shift in the energy levels of QD1 produced by the capacitive coupling between these two quantum dots, which detunes QD1 from QD2, thus blocking any coherent tunneling. (b),(c) Amplitude squared (population) of logical states as a function of time obtained by the time evolution of the Hamiltonian in Eq. (2) for two example initial states, $|001\rangle$ and $|101\rangle$, respectively, showing the conditional SWAP operation. We label only the relevant logical states, in color, and represent all leakage states in gray. We use $\Gamma \sim 44\ \mu$eV, $U = 21.83\Gamma$, $V = 10\Gamma$, and $\varepsilon_0 = \varepsilon_1 = \varepsilon_2 = 0$, estimates based on realistic values from the experimental literature [45].

Material [44]. The Fredkin gate is complete after a time

$$t^* = \frac{2\pi\hbar}{|U - V - \sqrt{16\Gamma^2 + (U-V)^2}|}. \tag{3}$$

In our simulations we use $\Gamma = 44\ \mu$eV, $V = 10\Gamma$, and $U \sim 20\Gamma$, a realistic set of parameter values obtained from Ref. [45]. With these values we obtain a gate time of roughly 143 ps. In Figs. 1(b) and 1(c) we show a simulation of the time evolution of the Hamiltonian in Eq. (2) for two initial states, demonstrating the dynamics of the conditional swap between the two target bits. While the time evolution of this Hamiltonian does not implement an exact Fredkin gate, this model allows sufficient flexibility in the parameters to implement a good approximation. For the parameter values used, the theoretical fidelity of the gate remains above 0.999, with quasistatic and high-frequency noise leading to fluctuations in the 10^{-3}–10^{-2} range, as described in Secs. II A and II B in Supplemental Material [44].

As mentioned earlier, our model also works with a single-electron encoding, in which case we have

$$|0\rangle = c_\sigma^\dagger\,|\emptyset\rangle\,, \qquad |1\rangle = |\emptyset\rangle\,, \tag{4}$$

with σ fixed to either spin up or spin down by our imposing a uniform static magnetic field to lift spin degeneracy. While the need for a magnetic field may introduce some challenges when one is attempting to scale up the system, this encoding may still be more amenable to a near-term experimental implementation given that the SWAP operation comprises the hopping of a single electron. In contrast to the double-electron encoding, this is faster and less susceptible to dephasing errors. A potential source of dephasing errors is energy relaxation due to electron-phonon coupling. These errors are especially relevant in the two-electron encoding since they will cause two electrons in a single quantum dot to spread to neighboring quantum dots, leading to leakage states in this configuration. Our estimates for gate speeds, based on typical semiconductor quantum dot parameters, are in the range of hundreds of picoseconds for the double-electron encoding and tens of picoseconds for the single-electron encoding. Recent experimental studies of coherent quantum dynamics have reported energy relaxation times in the nanosecond range [37], indicating that the gate implementation we propose here is fast enough to avoid decoherence induced by energy relaxation in both cases. We note that the Hamiltonian we consider has already been implemented experimentally in the work reported in Ref. [47] using a triple quantum dot system, a concrete first step in demonstrating the feasibility of our proposal, at least for the single-electron encoding.

B. Full-adder protocol

A full adder sums three bits, p, q, and r, outputting two bits: *parity* and *carry*. This operation can be done with a sequence of five Fredkin gates by use of two additional bits, as represented schematically in Fig. 2(a). A direct, fully coherent implementation of that scheme can, in principle, be done by coupling at least five distinct quantum dots, each encoding one of the initial $\{p, q, r, 0, 1\}$ logical bits, and then applying the illustrated sequence of

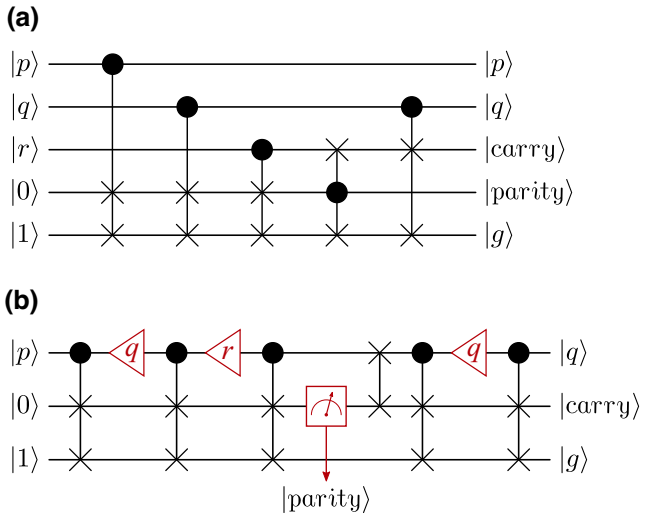

FIG. 2. One-bit full adder with Fredkin gates. (a) A single-bit full adder summing bits p, q, and r composed of Fredkin gates can be implemented with two extra ancilla bits initialized in 0 and 1. (b) To represent the same operation with only three physical bits, we collapse the top three lines into a single line representing the control bit for each Fredkin gate. The control bit, first initialized to the logical state $|p\rangle$, must be reinitialized with other logical states during the protocol, marked in the circuit by the left-pointing red triangles. After the third Fredkin gate, the second bit must be measured to save the $|\text{parity}\rangle$ value, which is part of the full-adder output. Then, a SWAP operation changes $|\text{parity}\rangle$ to the top bit to be used as a control bit in the following Fredkin gate. The final Fredkin gate is done after reinitialization of the control bit with $|q\rangle$. The output $|\text{carry}\rangle$ from the second bit and the previous $|\text{parity}\rangle$ value form the output of the full adder. The extra $|g\rangle$ output serves only to maintain logical reversibility.

five Fredkin gates. Instead, in this section, we focus on a physically simpler setup using only three quantum dots to implement the classical one-bit full adder, following the circuit scheme in Fig. 2(b). The trade-off is the need to perform at least one intermediate measurement, and the need to reinitialize the control quantum dot with different logical bits. This sacrifice in coherence may incur an additional energetic cost, but the reduced physical system should be advantageous for a near-term experimental demonstration of our work.

A quantum dot implementation of the circuit in Fig. 2(b) can be done with minimal changes to the triple quantum dot system used for the Fredkin gate. The key change is the need for electrons to tunnel between QD0 and QD1 in order to implement the intermediate SWAP operation in the circuit. This means that we must modify the previous triple quantum dot Hamiltonian in Eq. (2) by adding a new tunnel coupling parameterized by Γ^*:

$$H_A = H_F + \sum_{\sigma} \Gamma^* (c^\dagger_{0\sigma} c_{1\sigma} + c^\dagger_{1\sigma} c_{0\sigma}). \tag{5}$$

The protocol to run the full adder with three quantum dots according to the circuit in Fig. 2(b) is described schematically in Fig. 3. It requires a sequence of six steps, after an initial step 0 to load the information for the first Fredkin gate. In the first, second, and fifth steps, the control quantum dot must be reinitialized with a different logical state, stored in a classical register. Between each step, the dynamics are turned on via the tunnel coupling Γ, allowing the Fredkin gates to operate. During the third step, a measurement on QD1 is performed, obtaining the logical state corresponding to the parity bit. After the third step, the dynamics are activated via the tunnel coupling Γ^*, instead of Γ, together with a raise of $2V = 20\Gamma$ in the on-site potential ε_0 of QD0, conditional on $|\text{parity}\rangle = |1\rangle$. This ensures the execution of an auxiliary SWAP operation between QD0 and QD1 independent of the state of QD2. Following this extra operation, the remaining steps are performed as described previously, with a final measurement on QD1 returning the value of the carry bit. Both the parity bit and the carry bit correspond to the output of the full adder, which can be stored in a classical register after measurement. Scaling up this system may instead shuttle these quantum states directly into the input of a subsequent full adder. The full scheme and description of the steps can be seen in Fig. 3. Fidelity estimates for the proposed full-adder protocol are presented in Sec. III in Supplemental Material [44], showing values close to 0.99 for all input states, obtained by independent simulations of each intermediate step of the protocol.

IV. ENERGETICS

We now wish to estimate the energetic cost of running a full adder based on our proposed model. For this purpose, there are a few things to consider. First, we look at the energy changes at the Hamiltonian level. These constitute the lower bound on the energetic cost for the most efficient implementation of our proposed device. Second, we discuss a more realistic dissipation estimate based on current technology for gate-based quantum dots, as the true dissipation will come from the control pulses that implement the changes in the Hamiltonian. Third, we discuss the interplay between energetic cost and desired fidelity. Fourth, we discuss the energetic costs originating from the cryogenic equipment required to maintain the operational temperatures of quantum dots.

A. Hamiltonian-based estimate

The estimates we describe here are based on the theoretical Hamiltonian model used. The main cost to consider is the change in the tunnel coupling required to control the flow of electrons between neighboring quantum dots in each step of the protocol, as illustrated by the pulse sequence at the bottom of Fig. 3. This parameter can be controlled by raising or lowering the potential barrier

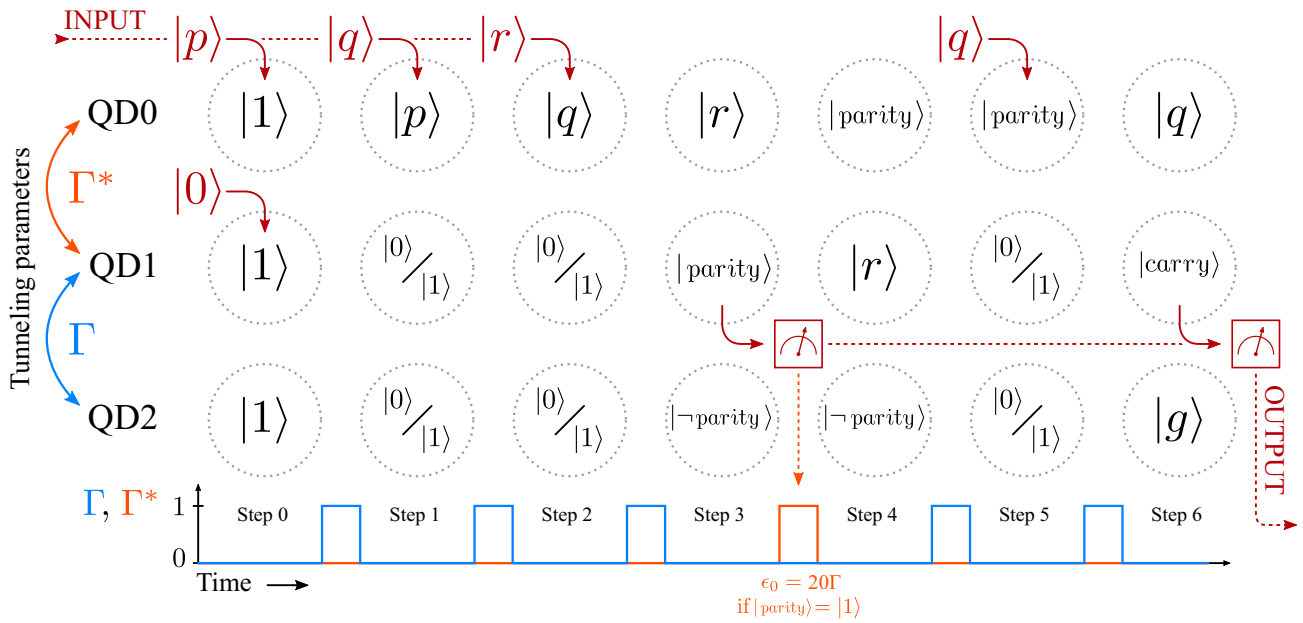

FIG. 3. One-bit full adder with three quantum dots. Schematic representation of the logical states in all three quantum dots, where QD0 is represented by the top row, QD1 by the middle row, and QD2 by the bottom row. The seven steps of the protocol are represented from left to right. Considering three initially empty quantum dots, the states $|p\rangle$ and $|0\rangle$ are loaded to QD0 and QD1, respectively (step 0). The coherent Hamiltonian dynamics are then unfrozen by activation of the coupling Γ during a time t^* corresponding to the Fredkin gate time. In steps 1 and 2, the state of QD0 is loaded with $|q\rangle$ and $|r\rangle$, respectively, and two more Fredkin gates are executed. In step 3, the state of QD1 corresponds to the *parity* bit, which must be measured: if it is 1, the on-site potential ϵ_0 is raised to $2V = 20\Gamma$, and if it is 0, ϵ_0 is unchanged. With this condition on ϵ_0, and by then activating Γ^*, the states of QD0 and QD1 swap independently of the state of QD2. After this auxiliary SWAP operation, Γ can be activated to complete step 4. In step 5, the last Fredkin gate is performed by loading $|q\rangle$ into QD0. Finally, in step 6, the *carry* bit can be read out of QD1, and the full adder is complete.

between two quantum dots, which can be described, for example, by a double square well or a biquadratic potential [49]. Given the model described in Ref. [49], it can be estimated that a change in the barrier height roughly equal to the charging energy U is enough to change the tunnel coupling Γ from approximately 1 to approximately 0 [23], where effectively no electron hopping occurs between the two quantum dots. Therefore, for our estimates, we associate an energetic cost of U with the action of freezing and unfreezing the dynamics. We consider also the worst-case scenario, where both increasing and decreasing the barrier will cost the same amount.

Besides the aforementioned costs, we also consider the costs of charging or discharging each quantum dot, having an associated cost U per electron, and the raising of the on-site potentials ϵ_l, costing the amount raised. Analyzing the protocol in Fig. 3 for the operation of a full adder, we may now count the various actions required at each step and sum their associated costs, as presented in Table I.

With the previously used values of $\Gamma = 44$ μeV, $V = 10\Gamma$, and $U = 21.83\Gamma$, the estimate for the optimal energetic cost to run the full-adder protocol, disregarding measurements, is $28U + 2V \sim 28$ meV. The costs listed in Table I are a theoretical lower bound for the operation of a single full adder. The costs of actually producing the desired changes in the Hamiltonian of a real system will depend on external factors from the experimental setup used to implement this Hamiltonian and perform measurements, which we discuss next.

TABLE I. Full-adder energetic cost. Energetic cost of each action required to perform the protocol illustrated in Fig. 3. The second column refers to the cost of charging or discharging each quantum dot as U per each potential electron coming in or out of each quantum dot at each step. The third and fourth columns refer to the energy changes in the Hamiltonian resulting from our controlling the parameters ϵ_l and Γ or Γ^* of the Hubbard model in Eq. (5). The total sum is $28U + 20\Gamma \sim 28$ meV for $\Gamma = 44$ μeV, $V = 10\Gamma$, and $U = 21.83\Gamma$.

Step	Charging	$C(\epsilon_l)$	$C(\Gamma)$
$0 \to 1$	$4U$	⋯	$2U$
$1 \to 2$	$2U$	⋯	$2U$
$2 \to 3$	$2U$	⋯	$2U$
$3 \to 4$	⋯	20Γ	$2U$
$4 \to 5$	⋯	⋯	$2U$
$5 \to 6$	$2U$	⋯	$2U$
$6 \to 0$	$6U$	⋯	⋯
Total	$16U$	20Γ	$12U$
	15 meV	0.9 meV	12 meV

B. External control

The implementation of external control electronics is an important topic in every scalable processor architecture. Rent's rule is a common empirical law used in such studies. It states that the number of external signals (T) controlling the individual gates inside a logic block (g) scales as a power law:

$$T = tg^p, \tag{6}$$

where t is the number of signals per logic gate and p is Rent's exponent, where the lower the value p, the more optimized the control scheme is [50]. Similarly to classical processors, it is expected that quantum systems will follow a similar rule with progressively lower p as more optimized schemes are designed [51].

In our work we consider a single device implementing a Fredkin gate and a full adder. Therefore, a study of the external control energetics in a scalable architecture scenario is beyond the scope of the current proposal. However, to get a rough estimate of the energetic costs of external control, we can use the results recently published in Ref. [52], where a scalable spin-qubit architecture in quantum dots was proposed with the purpose of optimizing the scaling factor between the number of qubits and external signals for control and measurement, and where a detailed estimate of the heat dissipated by the control equipment is provided. While a scalable architecture for classical computation based on our proposed device and logic encoding will certainly be very different, the technology used for control and readout signals should be similar to what is considered in Ref. [52].

In Ref. [52], a unit cell of four qubits and accompanying control electronics is considered as a building block. Three main sources of heat dissipation are identified: the dynamic power from the charging and discharging of parasitic capacitances between signal lines, the dissipation for the sample-and-hold circuits used to bias the gate electrodes in each quantum dot, and the power dissipated by the finite resistance of signal lines. It is then estimated that for an array of 2^{18} unit cells with 2^{20} qubits, the total dissipation will be on the order of 100 mW.

Assuming that it is possible to design a scalable architecture for our proposed device to implement 2^{18} full adders, with external control electronics comparable to the ones used in Ref. [52] and a similar power dissipation, we can estimate roughly 0.38 μW of power will be dissipated per full adder. In our work we estimate a full-adder operation time of 858 ps, corresponding to six Fredkin gates. However, the external control scheme used in Ref. [52] assumes operation times for one-qubit and two-qubit gates in the 25-ns range, and thus it is not reasonable to assume it could operate on a picosecond timescale with the same power dissipation. Instead, we consider each full adder following our model is tuned to have an operation time of 100 ns, which can be easily done by tuning Γ in our Hamiltonian model. Therefore, a power dissipation of 0.38 μW corresponds to an energetic cost of roughly 2.4×10^5 eV per full adder.

C. A note on fidelity

An important comment to make concerns the energetic cost to reach a desired operation fidelity. In our work, we consider a single time-independent Hamiltonian that implements a Fredkin gate with a theoretical error rate of 10^{-4}. Considering a full adder by repeated execution of the proposed Fredkin gate, we find the theoretical full-adder error rate is roughly 10^{-3} (see Table II in Supplemental Material [44]). In contrast, modern classical computers have much more negligible bit error rates. A common bottleneck is in memory devices, with error rates in the 10^{-15} range [53].

A comparison with conventional computers is fairest when one is considering a quantum device operating with the same fidelity requirements. A detailed study of this topic was done in Ref. [54] by consideration of resource estimates for quantum computing applications with a given target fidelity. Compared with quantum computing, our requirements on operation fidelity are less stringent. Since we need to correct only for bit flips between each gate operation, we may instead consider the application of classical error correcting codes. For example, for majority logic decoding and a repetition code with n instances, up to $n/2$ errors can be corrected, and an error rate of ϵ in each instance is reduced to a total error rate of roughly $\epsilon^{\frac{n+1}{2}}$. If we consider then an error-corrected logic block for one-bit addition composed of nine of our proposed full adders with majority logic decoding, the output would have a total error rate close to 10^{-15}, comparable to the error rate of conventional memory devices, with an order of magnitude increase in the energetic cost estimate. This exponential decrease in the error rate would incur at most a linear energetic cost, but potentially lower than that considering a single-input control signal to the logic block could be demultiplexed into the individual full adders.

D. Cryogenic costs

Another operational cost to consider is that of cryogenic equipment. Given that we are considering specific estimates for heat dissipation at specific cryogenic temperatures, the overall energetic costs should also consider the power input required by the cryogenic equipment to transfer the heat into a room temperature environment [55]. For a refrigerator with a cooling power P_{cool} at a given target cryogenic temperature T_c, transferring the heat to room temperature T_w with Carnot efficiency will lead to an input

power requirement P_{in} given by [56]

$$P_{\text{in}}^{\text{Carnot}} = P_{\text{cool}} \frac{T_w - T_c}{T_c}. \tag{7}$$

However, empirical studies of cryogenic equipment used in current laboratories [57] have found the relation to be closer to

$$P_{\text{in}}^{\text{real}} \sim P_{\text{cool}} \times 10^3 \times \frac{T_w - T_c}{T_c^2}. \tag{8}$$

Similar expressions with the same ratios can be written for the energetic cost directly, which we can then use to correct our previous estimates to provide the effective cost per full-adder operation when accounting for the cost of cryogenic cooling. For the Hamiltonian estimate of an energetic cost of 28 meV at an operation temperature of 100 mK, with an extra order of magnitude increase to account for the target fidelity, the corrected cost considering also the transfer of the dissipated heat under Carnot efficiency to a room temperature environment will be roughly 8.4×10^2 eV, while the corrected cost considering current laboratory equipment efficiency will be roughly 8.4×10^6 eV. Similarly, we can correct the estimates for an external control operating at 1 K, so the 2.4×10^5 eV cost per full adder becomes 7.2×10^8 eV at Carnot efficiency, or 7.2×10^{11} eV for laboratory equipment efficiency.

The first thing to note is that the estimates we provide here consider a single-stage heat transfer, which has high power requirements. As discussed in Ref. [54], the use of multistage cryogenics, i.e., using heat extraction at multiple intermediate temperatures between room temperature and the target cold temperature, may provide considerably better heat extraction efficiencies, although at this point it is unclear if the control electronics of a quantum-based classical computer could be arranged in a way to exploit multistage cryogenics. Secondly, a recent experiment demonstrated an autonomous energy harvester [58] utilizing resonant tunneling quantum dots. With such a device, the heat produced by this technology could potentially be reused as electrical power for the control electronics instead of being dissipated. Reusing dissipated energy for electrical power has long been an important technological problem to solve [59], but so far no successful implementations in classical computing have been achieved.

V. DISCUSSION AND CONCLUSIONS

In this work we explore the idea of using coherent quantum dynamics to perform energy-efficient classical computation by proposing a full adder based on semiconductor quantum dots. We present in Table II a comparison of our energetic estimates with the classical technology introduced in Sec. II B. Similarly to recent studies on quantum computing [54], we discuss several important aspects that will need to be further explored to make a precise claim on the advantages of quantum-based classical computers over current classical computers, such as the cost and scalability of external control, the overhead associated with attaining competitive gate fidelities, and the cost associated with cryogenic cooling.

Regarding fidelity and external control, some authors [60,61] have argued that, in general, the energy required for this control may be significant. This is because the control system needs to have enough energy so that quantum fluctuations of the control and entanglement with the logical system do not have a significant impact on the gate's fidelity. To the best of our knowledge, this requirement has not been shown to apply universally, and was subject to some debate [62–64]. Furthermore, in a recent superconducting experiment [65] it was shown that a single qubit extracts one only quantum of energy from the driving field

TABLE II. Energetic cost estimate comparison. The top three rows are the energy cost estimates per bit operation in modern supercomputers, transistor-based full adders, and quantum dot cellular automata discussed in Sec. II B. In the bottom two rows we present the estimates provided for the operation of our proposed quantum dot full adder, including the lower bounds obtained directly from the Hamiltonian model, which assumes a working temperature equal to the quantum dot temperature of 100 mK, as well as the external control estimates considering a scalable architecture similar to the one in Ref. [52], which assumes the working temperature of the control electronics at 1 K. In the fidelity column we assume a 1-order-of-magnitude increase in the base cost obtained from an error-correcting scheme as described in Sec. IV C. For cryogenic technologies we also present the estimates corrected for the cost of cryogenic cooling assuming Carnot efficiency (third column) and laboratory equipment efficiency (fourth column), as discussed in Sec. IV D. While these estimates are considerably greater, we discuss in Sec. IV D some possible ways to alleviate them in the future.

Technology		Approximate cost per bit operation (eV)			
		Base cost	Fidelity	Cryogenic cooling corrected	
Modern supercomputers, $T = 300$ K		10^5	⋯	⋯	⋯
Transistor full adders, $T = 300$ K		10^3	⋯	⋯	⋯
QD cellular automata, $T = 1$ K		1	⋯	10^2	10^5
QD full adder	(Hamiltonian, $T = 0.1$ K)	10^{-2}	10^{-1}	10^3	10^7
QD full adder	(external control, $T = 1$ K)	10^5	10^6	10^9	10^{12}

during a gate operation. Nevertheless, it is unclear if such a fundamental observation can be translated into practical and substantial gains in the energy efficiency of the control electronics.

Regarding cryogenic cooling, as we have discussed, the transfer of heat to the environment will be an important limitation to be tackled given the potentially disruptive costs associated with the operation of refrigerators. Designing a quantum-based classical computer from the ground up with a focus on energy harvesting could be a promising direction, supported by the recent results in Ref. [58].

Our approach is to encode the logical state of each bit with one or two electrons in a single quantum dot. While our encoding is not compatible with quantum computing, similar devices exploiting quantum dynamics with the goal of energy efficiency may also be designed using compatible qubit encodings. Nevertheless, the possibility of encoding logic in more general quantum states eases some restrictions on device design, which may be beneficial for the future scalability of such technologies. Besides quantum dots, other platforms currently being explored for quantum computing, such as trapped ions or superconductors, may also be considered, as recently done in Ref. [66] for trapped ions. While some quantum computing platforms may be found to be more energy efficient, semiconductor quantum dots may have an important advantage for large-scale processor development: their compatibility with the already advanced semiconductor fabrication techniques [25].

Our results are a first step in a road map to develop energy-efficient classical computers exploiting quantum dynamics. Several significant challenges will need to be addressed, such as the study of the energetics of quantum technologies [66–69], the development of energy-efficient control systems and cryogenic equipment, compatible data buses [23] and memory devices, and ultimately the combination of all elements into a scalable and energy-efficient processor architecture. Our work proposes a first step in this direction, which may prove to be a promising alternative for the future of high-performance computers when current transistor-based semiconductor technologies reach their absolute limits.

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[1] G. E. Moore, Cramming more components onto integrated circuits (1965).
[2] L. B. Kish, End of Moore's law: Thermal (noise) death of integration in micro and nano electronics, Phys. Lett. A **305**, 144 (2002).
[3] J. Koomey, S. Berard, M. Sanchez, and H. Wong, Implications of historical trends in the electrical efficiency of computing, IEEE Ann. History Comput. **33**, 46 (2010).
[4] J. G. Koomey, in *AIP Conference Proceedings*, Vol. 1652 (American Institute of Physics, 2015), p. 82.
[5] E. Masanet, A. Shehabi, N. Lei, S. Smith, and J. Koomey, Recalibrating global data center energy-use estimates, Science **367**, 984 (2020).
[6] U. Gupta, Y. G. Kim, S. Lee, J. Tse, H.-H. S. Lee, G.-Y. Wei, D. Brooks, and C.-J. Wu, Chasing carbon: The elusive environmental footprint of computing, IEEE Micro (2022).
[7] P. Benioff, The computer as a physical system: A microscopic quantum mechanical Hamiltonian model of computers as represented by Turing machines, J. Stat. Phys. **22**, 563 (1980).
[8] P. Benioff, Quantum Mechanical Models of Turing Machines That Dissipate No Energy, Phys. Rev. Lett. **48**, 1581 (1982).
[9] E. Fredkin and T. Toffoli, Conservative logic, Int. J. Theor. Phys. **21**, 219 (1982).
[10] L. B. Levitin and T. Toffoli, Thermodynamic Cost of Reversible Computing, Phys. Rev. Lett. **99**, 110502 (2007).
[11] I. Hänninen, H. Lu, C. S. Lent, and G. L. Snider, *Energy recovery and logical reversibility in adiabatic CMOS multiplier* (Springer, 2013), p. 25.
[12] R. Landauer, Irreversibility and heat generation in the computing process, IBM J. Res. Develop. **5**, 183 (1961).
[13] J. Preskill, Quantum computing 40 years later, (2021), arXiv preprint ArXiv:arXiv:2106.10522.
[14] D. A. Lidar and T. A. Brun, *Quantum Error Correction* (Cambridge University Press, 2013).
[15] E. Grumbling and M. Horowitz, *Quantum Computing: Progress and Prospects* (National Academies Press, Washington: DC, 2018).
[16] I. L. Chuang, N. Gershenfeld, and M. Kubinec, Experimental Implementation of Fast Quantum Searching., Phys. Rev. Lett. **80**, 3408 (1998).
[17] F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. Brandao, D. A. Buell, and B. Burkett, Quantum supremacy using a programmable superconducting processor, Nature 505 (2019).
[18] H.-S. Zhong, H. Wang, Y. H. Deng, M. C. Chen, L. C. Peng, Y. H. Luo, J. Qin, D. Wu, X. Ding, Y. Hu, and P. Hu,

Quantum computational advantage using photons, Science 1460 (2020).
[19] J. von Neumann, C. S. (ed.),, and J. M. (ed.), *Fault-tolerant classical computing, in Automata Studies* (Princeton University Press, 1956), p. 43.
[20] D. Gottesman, in *Quantum Information Science and Its Contributions to Mathematics, Proceedings of Symposia in Applied Mathematics*, Vol. 68 (2010), p. 13.
[21] D. P. DiVincenzo, The physical implementation of quantum computation, Fortschritte der Phys.: Prog. Phys. **48**, 771 (2000).
[22] B. Antonio, J. Randall, W. Hensinger, G. Morley, and S. Bose, Classical computation by quantum bits, (2015), arXiv preprint ArXiv:1509.03420.
[23] D. Lewis, J. P. Moutinho, A. Costa, Y. Omar, and S. Bose, Low-dissipation data bus via coherent quantum dynamics, (2023), arXiv preprint ArXiv:2304.02391.
[24] Y. Omar, A. Costa, S. Bose, J. P. Moutinho, and M. Pezzutto, PCT/PT2021/050022 (2022).
[25] M. Gonzalez-Zalba, S. de Franceschi, E. Charbon, T. Meunier, M. Vinet, and A. Dzurak, Scaling silicon-based quantum computing using CMOS technology, Nat. Electron. **4**, 872 (2021).
[26] C. Figgatt, A. Ostrander, N. M. Linke, K. A. Landsman, D. Zhu, D. Maslov, and C. Monroe, Parallel entangling operations on a universal ion-trap quantum computer, Nature **572**, 368 (2019).
[27] W. Stallings, *Computer Organization and Architecture: Designing for Performance* (Prentice Hall, Upper Saddle River, NJ, 2010), 8th ed.
[28] K. Mangla and S. Saxena, Analysis of different CMOS full adder circuits based on various parameters for low voltage VLSI design., Int. J. Eng. Tech. Res. **3**, 1460 (2015).
[29] M. Hasan, A. H. Siddique, A. H. Mondol, M. Hossain, H. U. Zaman, and S. Islam, Comprehensive study of 1-bit full adder cells: review, performance comparison and scalability analysis, SN Appl. Sci. **3**, 1 (2021).
[30] K. Navi, R. Farazkish, S. Sayedsalehi, and M. R. Azghadi, A new quantum-dot cellular automata full-adder, Microelectron. J. **41**, 820 (2010).
[31] S. Hashemi, M. Tehrani, and K. Navi, An efficient quantum-dot cellular automata full-adder, Sci. Res. Essays **7**, 177 (2012).
[32] E. Taherkhani, M. H. Moaiyeri, and S. Angizi, Design of an ultra-efficient reversible full adder-subtractor in quantum-dot cellular automata, Optik **142**, 557 (2017).
[33] D. Abedi, G. Jaberipur, and M. Sangsefidi, Coplanar full adder in quantum-dot cellular automata via clock-zone-based crossover, IEEE Trans. Nanotechnol. **14**, 497 (2015).
[34] C. S. Lent and P. D. Tougaw, A device architecture for computing with quantum dots, Proc. IEEE **85**, 541 (1997).
[35] D. Kim, D. Ward, C. Simmons, J. K. Gamble, R. Blume-Kohout, E. Nielsen, D. Savage, M. Lagally, M. Friesen, and S. Coppersmith, *et al.*, Microwave-driven coherent operation of a semiconductor quantum dot charge qubit, Nat. Nanotechnol. **10**, 243 (2015).
[36] H.-O. Li, G. Cao, G.-D. Yu, M. Xiao, G.-C. Guo, H.-W. Jiang, and G.-P. Guo, Conditional rotation of two strongly coupled semiconductor charge qubits, Nat. Commun. **6**, 1 (2015).
[37] H.-O. Li, G. Cao, G.-D. Yu, M. Xiao, G.-C. Guo, H.-W. Jiang, and G.-P. Guo, Controlled Quantum Operations of a Semiconductor Three-Qubit System, Phys. Rev. Appl. **9**, 024015 (2018).
[38] G. Cao, H.-O. Li, T. Tu, L. Wang, C. Zhou, M. Xiao, G.-C. Guo, H.-W. Jiang, and G.-P. Guo, Ultrafast universal quantum control of a quantum-dot charge qubit using Landau–Zener–Stückelberg interference, Nat. Commun. **4**, 1 (2013).
[39] Z. Shi, C. Simmons, D. R. Ward, J. Prance, X. Wu, T. S. Koh, J. K. Gamble, D. Savage, M. Lagally, and M. Friesen, *et al.*, Fast coherent manipulation of three-electron states in a double quantum dot, Nat. Commun. **5**, 1 (2014).
[40] A. Imre, G. Csaba, L. Ji, A. Orlov, G. Bernstein, and W. Porod, Majority logic gate for magnetic quantum-dot cellular automata, Science **311**, 205 (2006).
[41] I. Amlani, A. O. Orlov, G. Toth, G. H. Bernstein, C. S. Lent, and G. L. Snider, Digital logic gate using quantum-dot cellular automata, Science **284**, 289 (1999).
[42] A. Orlov, I. Amlani, G. Bernstein, C. Lent, and G. Snider, Realization of a functional cell for quantum-dot cellular automata, Science **277**, 928 (1997).
[43] The TOP500 project, https://www.top500.org/project/.
[44] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PRXEnergy.2.033002 for supporting calculations and a discussion.
[45] C. Simmons, M. Thalakulam, B. Rosemeyer, B. Van Bael, E. Sackmann, D. Savage, M. Lagally, R. Joynt, M. Friesen, and S. Coppersmith, *et al.*, Charge sensing and controllable tunnel coupling in a Si/SiGe double quantum dot, Nano Lett. **9**, 3234 (2009).
[46] G.-D. Yu, H.-O. Li, G. Cao, M. Xiao, H.-W. Jiang, and G.-P. Guo, Tunable capacitive coupling between two semiconductor charge qubits, Nanotechnology **27**, 324003 (2016).
[47] T. Hensgens, T. Fujita, L. Janssen, X. Li, C. Van Diepen, C. Reichl, W. Wegscheider, S. D. Sarma, and L. M. Vandersypen, Quantum simulation of a Fermi–Hubbard model using a semiconductor quantum dot array, Nature **548**, 70 (2017).
[48] D. Schröer, A. D. Greentree, L. Gaudreau, K. Eberl, L. C. L. Hollenberg, J. P. Kotthaus, and S. Ludwig, Electrostatically defined serial triple quantum dot charged with few electrons, Phys. Rev. B **76**, 075306 (2007).
[49] S. Yang, X. Wang, and S. DasSarma, Generic Hubbard model description of semiconductor quantum-dot spin qubits, Phys. Rev. B **83**, 161301 (2011).
[50] B. S. Landman and R. L. Russo, On a pin versus block relationship for partitions of logic graphs, IEEE Trans. Comput. **100**, 1469 (1971).
[51] D. P. Franke, J. S. Clarke, L. M. Vandersypen, and M. Veldhorst, Rent's rule and extensibility in quantum computing, Microprocess. Microsyst. **67**, 1 (2019).
[52] J. M. Boter, J. P. Dehollain, J. P. G. vanDijk, Y. Xu, T. Hensgens, R. Versluis, H. W. L. Naus, J. S. Clarke, M. Veldhorst, F. Sebastiano, and L. M. K. Vandersypen, Spiderweb Array: A sparse Spin-Qubit Array, Phys. Rev. Appl. **18**, 024053 (2022).
[53] N. Mielke, T. Marquart, N. Wu, J. Kessenich, H. Belgal, E. Schares, F. Trivedi, E. Goodness, and L. R. Nevill, in *2008*

IEEE International Reliability Physics Symposium (IEEE, 2008), p. 9.

[54] M. Fellous-Asiani, J. H. Chai, Y. Thonnart, H. K. Ng, R. S. Whitney, and A. Auffèves, Optimizing resource efficiencies for scalable full-stack quantum computers, (2022), arXiv preprint ArXiv:2209.05469.

[55] M. J. Martin, C. Hughes, G. Moreno, E. B. Jones, D. Sickinger, S. Narumanchi, and R. Grout, Energy use in quantum data centers: Scaling the impact of computer architecture, qubit performance, size, and thermal parameters, IEEE Transactions on Sustainable Computing (2022).

[56] V. Parma, Cryostat design, (2015), arXiv preprint ArXiv:1501.07154.

[57] D. S. Holmes, in *2021 IEEE International Roadmap for Devices and Systems Outbriefs* (IEEE, 2021), p. 1.

[58] G. Jaliel, R. K. Puddy, R. Sánchez, A. N. Jordan, B. Sothmann, I. Farrer, J. P. Griffiths, D. A. Ritchie, and C. G. Smith, Experimental Realization of a Quantum Dot Energy Harvester, Phys. Rev. Lett. **123**, 117701 (2019).

[59] B. E. White, Beyond the battery, Nat. Nanotechnol. **3**, 71 (2008).

[60] J. Gea-Banacloche, Minimum Energy Requirements for Quantum Computation, Phys. Rev. Lett. **89**, 217901 (2002).

[61] J. Gea-Banacloche and L. B. Kish, Comparison of energy requirements for classical and quantum information processing, Fluctuation Noise Lett. **3**, C3 (2003).

[62] W. M. Itano, Comment on "some implications of the quantum nature of laser fields for quantum computations", Phys. Rev. A **68**, 046301 (2003).

[63] S. J. van Enk and H. J. Kimble, Reply I to "Comment on 'Some implications of the quantum nature of laser fields for quantum computation' ", Phys. Rev. A **68**, 046302 (2003).

[64] J. Gea-Banacloche, Reply II to "Comment on 'Some implications of the quantum nature of laser fields for quantum computations' ", Phys. Rev. A **68**, 046303 (2003).

[65] J. Stevens, D. Szombati, M. Maffei, C. Elouard, R. Assouly, N. Cottet, R. Dassonneville, Q. Ficheux, S. Zeppetzauer, and A. Bienfait, *et al.*, Energetics of a Single Qubit Gate, Phys. Rev. Lett. **129**, 110601 (2022).

[66] S. Pratapsi, P. Huber, P. Barthel, S. Bose, C. Wunderlich, and Y. Omar, Classical half-adder using trapped-ion quantum bits: Towards energy-efficient computation, (2022), arXiv preprint ArXiv:2210.10470.

[67] L. Buffoni, S. Gherardini, E. Z. Cruzeiro, and Y. Omar, Third law of thermodynamics and the scaling of quantum computers, (2022), arXiv preprint ArXiv:2203.09545.

[68] A. Auffèves, Quantum Technologies Need a Quantum Energy Initiative, PRX Quantum **3**, 020101 (2022).

[69] D. Jaschke and S. Montangero, Is quantum computing green? an estimate for an energy-efficiency quantum advantage, (2022), arXiv preprint ArXiv:2205.12092.