Photonic interlacing architectures for learning discrete linear unitaries

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Recent investigations suggest that the discrete linear unitary group $U(N)$ can be represented by interlacing a finite sequence of diagonal phase operations with an intervening unitary operator. However, despite rigorous numerical justifications, no formal proof has been provided. Here, we show that elements of $U(N)$ can be decomposed into a sequence of N-parameter phases alternating with one-parameter propagators of a lattice Hamiltonian. The proof is based on building a Lie group by alternating these two operators and showing its completeness to represent $U(N)$ for a finite number of layers. This is numerically verified by using Haar random matrices as targets, showing a convergence for exactly N layers. As a specific application, we propose an integrated all-optical logic gate device that performs OR, NAND, XOR, and XAND tasks within a lossless and passive optical circuit design.

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I. INTRODUCTION

Since the pioneering work of Reck *et al.* [1], there has been an ever-increasing interest in realizing optical structures that perform arbitrary discrete linear unitary operations. This interest is driven by the exciting properties of optical propagation, such as processing capabilities, lower energy consumption, and faster processing speeds than their electronic counterparts. The last one is central in classical and quantum optical information processing [2–7]. Further research has been driven to perform optical operation through free-space propagation [8–11].

The rapid developments of photonic integrated circuit technologies have positioned them as a natural platform for large-scale implementation of photonic unitary circuits through multipath interference networks and reconfigurable phase shifters [12–18]. In the context of classical photonics, the implementation of linear operations has gone beyond the realm of unitaries to cover general matrix operations [19,20], which find applications in optical convolutional units [21,22], orthogonal communication channels [23,24], and experimental realization of mode-division demultiplexing [25].

Recent studies have shown promising results in this field, and further research is underway to advance these technologies. Research has been focused on developing devices that can perform all-optical unitary operations packaged in on-chip form-factor architectures [2,3,16–19,26,27]. Alternative architectures based on cascading of a fixed intervening operator with diagonal phase shift layers, capable of representing universal unitary matrices, have been reported in the literature [13,16,26,28–31]. Such an architecture can be realized on-chip with multimode interference couplers [13], or multicore waveguide couplers [16,26], interlaced with programmable phase shifters. In particular, recently, we showed that nonuniform photonic lattices of particularly designed coupling coefficients and length to implement a discrete fractional Fourier transform operation can be utilized as the intervening operation for realizing programmable unitaries through such an interlacing architecture [16,17]. While a formal proof of the universality of this construction is not currently available, strong numerical evidence, i.e., a phase transition in the norm of representation error, suggests that arbitrary unitary matrices can be realized with remarkable precision, even within the numerical noise error.

This work focuses on the factorization of $N \times N$ unitary matrices in terms of diagonal unitaries and families of one-parameter unitaries established through the propagator of lattice Hamiltonians. This approach has two fundamental benefits. First, the one-parameter unitaries enable a group structure that imposes a finite upper limit on the number of matrices necessary for the factorization. Second, the proposed factorization can be implemented using elementary optical components, such as phase shifters and waveguide arrays, making it ideal for photonic applications. The so-constructed architecture is numerically tested and shown to reconstruct arbitrary unitary matrices successfully with satisfactory accuracy. This is achieved by optimizing the space of parameters defining the architecture, composed of N^2 phase shifters and N waveguide lengths, which overparameterize the optimization problem in question (N^2 parameters required for $N \times N$

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unitaries). To illustrate our results, an all-logical logic gate device is proposed and simulated as a particular application, resulting in a passive photonic unit. The latter is achieved by using a lossless single-stack optical circuit design, unlike other approaches that require amplitude modulation or complex multistack structures [32,33]. This provides an architecture design based on silicon-on-silica platforms that can be fabricated in open-access foundries without requiring any specialized fabrication process. This provides an architecture design based on silicon-on-silica platforms compatible with open-access foundries without requiring any specialized fabrication process.

The paper is organized as follows. Section II proposes a representation for arbitrary $N \times N$ unitary matrices based on a factorization in terms of other particular unitary matrices. This is essential as it allows for proof of the finiteness of the architecture factorization, yielding a termination criterion for iterative algorithms that search for the optimal factorization length. The latter is corroborated by numerical tests, where a significant drop in the reconstruction error is found at exactly N layers. In Sec. III, an all-optical implementation of the proposed factorization is discussed. This allows for a compact on-chip device based merely on coupled waveguides of different lengths and layers of passive phase elements. Particularly, a three-port logic gate photonic circuit is introduced to illustrate the potential applications of the device, which is further reinforced by comparing the ideal model with full-wave simulations. Such a circuit operates by purely passive means, rendering an energy-efficient solution that performs the AND, OR, NAND, and XOR operations.

II. PROOF OF UNIVERSALITY

A. Notation

Let us consider $\mathcal{U}$ as an arbitrary element of the group $U(N)$ of unitary $N \times N$ matrices, $\mathcal{U} \in U(N)$. It is desirable to find a factorization of unitary matrices in terms of a set of unitary matrices that serve as building blocks to reconstruct any $\mathcal{U} \in U(N)$. Indeed, several such factorizations have been introduced and discussed in the literature of lossless photonic architectures [16,17,28,30]. Throughout this manuscript, we consider the particular factorization,

$$\mathcal{U}(\boldsymbol{x}) = e^{iQ^{(M)}} e^{i\ell_{M-1}H} e^{iQ^{(M-1)}} \cdots e^{i\ell_1 H} e^{iQ^{(1)}}, \tag{1}$$

where $M \in \mathbb{Z}^+$ is the total number of layers required in the factorization and $Q^{(n)}$ are diagonal matrices containing the phase components $Q^{(n)}_{j,k} = \phi^{(n)}_j \delta_{j,k}$, with $\phi^{(n)}_j \in (0, 2\pi]$ for all $j, k \in \{1, \ldots, N\}$ and $n \in \{1, \ldots, M\}$. Furthermore, $\boldsymbol{x}$ stands for the tuple composed of the previous parameters ϕ's and ℓ.

Here, $H = H^\dagger$ is a Hermitian matrix in $\mathbb{C}^N$ characterizing the coupled waveguide array, whereas ℓ_n stands for the waveguide coupling length. Since H contains the information about the mode coupling between nearest waveguides, we focus on operators whose matrix representation renders a tridiagonal matrix; i.e.,

$$H_{p,q} = \kappa_{p-1}\delta_{p,q-1} + \kappa_p \delta_{p,q+1} + \nu_p \delta_{p,q}, \tag{2}$$

for $p, q, \in \{1, \ldots, N-1\}$. This structure follows from the coupled-mode theory [34] and the evanescent wave coupling between nearest neighbors and onsite coupling due to phase mismatch. From Eq. (1), it is clear that the architecture contains NM programmable phase shifter parameters and $N-1$ coupling lengths to be optimized based on the given target matrix $\mathcal{U}$. It is worth noting that the length of the waveguide arrays is fixed and cannot be adjusted within this particular architecture, which can be optimized beforehand in order to construct the unitary optical unit of interest. The mathematical proof below ensures that any unitary operator can be built this way.

B. Existence of layer number bound

In this section, we prove that, for every positive N, any $\varepsilon > 0$, and any unitary $N \times N$ matrix, there exists M and a factorization (1) of length M for $\mathcal{U}$ up to ε error ($\varepsilon = 0$ for a subclass of cases, explained below). This result serves as a termination criterion for a numerical (e.g., optimization-based) algorithm that, for the smallest $M = N$, tries to find a factorization up to ε and, if it fails, increments M by 1 and continues.

Remark 1. In our computational experiments, we never had to go beyond $M = N$.

Let $\mathbb{R}$ and $\mathbb{C}$ denote the fields of real and complex numbers, respectively. For a field F, such as $\mathbb{R}$ or $\mathbb{C}$, let $\mathrm{GL}(N, F)$ denote the group of all invertible $N \times N$ matrices with entries in F.

Lemma 1. Let

$$T_N := \{e^{i\mathrm{diag}(\phi_1,\ldots,\phi_N)} \mid \phi_1, \ldots, \phi_N \in \mathbb{R}\}$$

(which are diagonal matrices with diagonal entries $e^{i\phi_j}$) and, for a matrix H,

$$G_H := \overline{\{e^{i\ell H} \mid \ell \in \mathbb{R}\}},$$

the closure as a real Lie group. Then, there exists a nonnegative integer M such that

$$G := T_N \cdot G_H \cdot T_N \cdot G_H \cdot \cdots \ (M \text{ times}) \tag{3}$$

is a real Lie subgroup of $U(N)$. Moreover, if the ratios of H's nonzero eigenvalues are rational numbers, then it is not necessary to take the closure in the definition of G_H, that is,

$$G_H = \{e^{i\ell H} \mid \ell \in \mathbb{R}\}. \tag{4}$$

Proof. By Ref. [35, P. 8, Problem 14], the ratios of the nonzero elements from $a_1, \ldots, a_N$ are rational numbers if and only if

$$D := \{e^{i\ell\,\mathrm{diag}(a_1,\ldots,a_N)} \mid \ell \in \mathbb{R}\}$$

is a real Lie subgroup of $U(N)$. Therefore, the ratios of the nonzero eigenvalues of the matrix H are rational if and only if $\{e^{i\ell H} \mid \ell \in \mathbb{R}\}$ is a real Lie subgroup of $U(N)$ and so $\{e^{i\ell H} \mid \ell \in \mathbb{R}\} = \overline{\{e^{i\ell H} \mid \ell \in \mathbb{R}\}} = G_H$. The result in Eq. (3) now follows from Ref. [36, Sec. 7.5].

The statement of Lemma 1 does not guarantee that the Lie group G as defined in Eq. (3) is equal to the whole $U(N)$. We will now establish a sufficient condition for $G = U(N)$ that allows for physically meaningful matrices H. For this, let $\mathcal{J}$ be the set of matrices J such that the Lie algebra generated by J and the Lie algebra of T_N contain a matrix $\mathcal{M}$ that is conjugate to a single Jordan block of size N.

Example 1. Consider a matrix H from (2) such that $\kappa_i \neq 0$ for all $i \in \{1, \ldots, N-1\}$. A direct computation shows that the vector space spanned over $\mathbb{C}$ by

- the Lie brackets of H with the standard basis of the Lie algebra of T_N and
- the Lie brackets of the above again with the standard basis of the Lie algebra of T_N

contains a matrix $\mathcal{M}$ that is conjugate to a single Jordan block of size N. Therefore, $H \in \mathcal{J}$.

Lemma 2. For all $H \in \mathcal{J}$, the real Lie group G defined by Eq. (3) is equal to $U(N)$.

Proof. Since G is a compact Lie group, its complexification $G_{\mathbb{C}}$ is a reductive group [35, p. 246, Problem 22]. Moreover, $G_{\mathbb{C}}$ also contains a maximal torus $T_{\mathbb{C}}$ (the complexification of T_N) of $\mathrm{GL}(N, \mathbb{C})$ and so $G_{\mathbb{C}}$ is of maximal rank. By Ref. [36, Sec. 26.2, Corollary A(b)], the center $Z(G_{\mathbb{C}})$ of $G_{\mathbb{C}}$ is contained in $T_{\mathbb{C}}$. By Ref. [37, Théorème 5], $G_{\mathbb{C}}$ is the connected component of the normalizer of and therefore is the centralizer of $Z(G_{\mathbb{C}}) \subset T_{\mathbb{C}}$ in $\mathrm{GL}(N, \mathbb{C})$. Thus, $G_{\mathbb{C}}$ is conjugate to a direct product $\mathrm{GL}(k_1, \mathbb{C}) \times \cdots \times \mathrm{GL}(k_s, \mathbb{C})$ for some positive integers $s, k_1, \ldots, k_s$ (see, e.g., Ref. [38, Lemma 14.0.6] or proof of Ref. [36, Sec. 9.1, Proposition]). Since the Lie algebra of $G_{\mathbb{C}}$ contains $\mathcal{M}$ that is conjugate to a single Jordan block of size N, we have $s = 1$ and $k_1 \equiv k = N$. Hence, $G_{\mathbb{C}} = \mathrm{GL}(N, \mathbb{C})$ and so $G = U(N)$.

Remark 2. Even though Lemma 2 establishes the equality $G = U(N)$, the definition of G involves taking a closure in the components G_H. In Corollary 1, we will clarify how to practically use the closure and when we know that we can avoid taking the closure due to Eq. (4).

Corollary 1. Consider a matrix H from Eq. (2) such that $\kappa_i \neq 0$ for all $i \in \{1, \ldots, N-1\}$. Then, for every positive integer N, matrix $\mathcal{U} \in U(N)$, and $\varepsilon > 0$, there exist a positive integer M and sets of real numbers $\{\ell_p\}_{p=1}^{M-1}$ and $\{\phi_n^{(p)}\}_{p=1,n=1}^{N,M}$ forming the tuple $\boldsymbol{x}$ such that

$$\|\mathcal{U} - \mathcal{U}(\boldsymbol{x})\| \leqslant \varepsilon$$

in the standard matrix norm [see notation (1)], where $\|A\| := \sqrt{tr(AA^{\dagger})}$ is the Frobenius norm. Moreover, if the ratios of H's nonzero eigenvalues are rational numbers, then $\boldsymbol{x}$ can be chosen so that $\mathcal{U}(\boldsymbol{x}) = \mathcal{U}$.

III. PHOTONIC DESIGN AND PERFORMANCE

A. Structure components

The proposed factorization is particularly suitable for optical implementations due to the nature of diagonal phase matrices, which can be represented in photonic circuits through layers of phase shifters. The photonic implementation of the proposed factorization is shown in Fig. 1. Recent progress on phase elements allows the tuning of phases of about π radians in structures as long as 20 μm using phase-change materials [39,40]. In turn, the interlacing matrices $F_\ell = e^{i\ell H}$ match the wave evolution of electromagnetic waves through coupled waveguide arrays.

This relation arises from coupled-mode theory [34], where the wave evolution is ruled by the discrete Schrödinger-like equation $-id\vec{E}/dz = H\vec{E}$, where the propagation coordinate z plays the role of the time parameter in the Schrödinger equation. Here, H is an $N \times N$ tridiagonal Hamiltonian characterizing the coupling between a given waveguide and its two nearest neighbors, related to the overlap of the evanescent waves outside the waveguide cores.

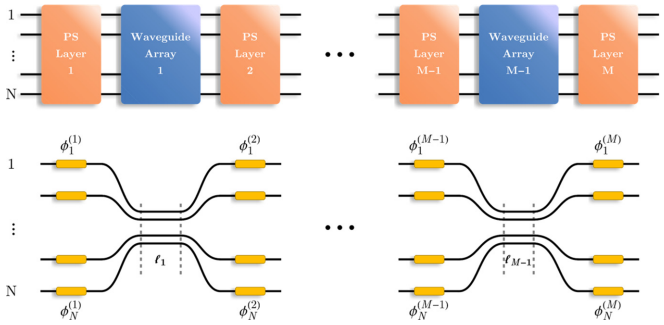

FIG. 1. Sketch of the proposed factorization and its physical realization for an N-port device through waveguide arrays with lengths ℓ_j and phase elements $\phi_n^{(m)}$ for a finite number of layers M.

Such an overlap is isotropic from one waveguide to its neighbor, leading to coupling parameters that render a Hermitian matrix Hamiltonian H. In this form, the tridiagonal matrix form used in our proof is compatible with the matrix representation of coupled waveguide arrays. Two noteworthy cases for H are the J_x lattice [41–43] and the homogeneous lattice [44,45], both with on-site terms $\nu_n = 0$ and coupling parameters

$$\kappa_n^{(Jx)} = \widetilde{\kappa}\sqrt{(N-n)n}/2 \quad \text{and} \quad \kappa_n^{(h)} = \widetilde{\kappa},$$

respectively, with $n \in \{1, \ldots, N-1\}$ and $\widetilde{\kappa}$ a scaling factor obtained from the geometries, wavelength, and other relevant physical parameters of the waveguides [42].

The J_x lattice has linearly increasing eigenvalues

$$\frac{\lambda_m^{(Jx)}}{\widetilde{\kappa}} = m - \frac{N+1}{2}, \quad m \in \{1, \ldots, N\},$$

whereas the homogeneous lattice has

$$\frac{\lambda_m^{(h)}}{\widetilde{\kappa}} = 2\cos(\pi m/(N+1)), \quad m \in \{1, \ldots, N\}.$$

These are examples of Hamiltonians with either rational or irrational eigenvalue ratios so that an arbitrary ε precision can be achieved (see Corollary 1). Throughout the manuscript, without lack of generality, we fix $\widetilde{\kappa} = 1$ for simplicity.

Remark 3. Although our proof has established the existence of a finite number of layers M to render the universality of the proposed factorization, the exact value of M is yet to be found. Furthermore, for an arbitrary $N \times N$ unitary matrix $\mathcal{U}$, our factorization yields $M(N+1) - 1$ free parameters for an M-layer architecture, whereas any matrix $\mathcal{U} \in U(N)$ is defined, in general, by N^2 parameters. This establishes the lower bound for the number of layers as $M \geqslant N$.

B. Parameter optimization

Let $\mathcal{U}_t$ be an arbitrary unitary target matrix and

$$\boldsymbol{x} = \left\{\phi_p^m\right\}_{p=1,m=1}^{N,M} \cup \{\ell_m\}_{m=1}^{M-1}$$

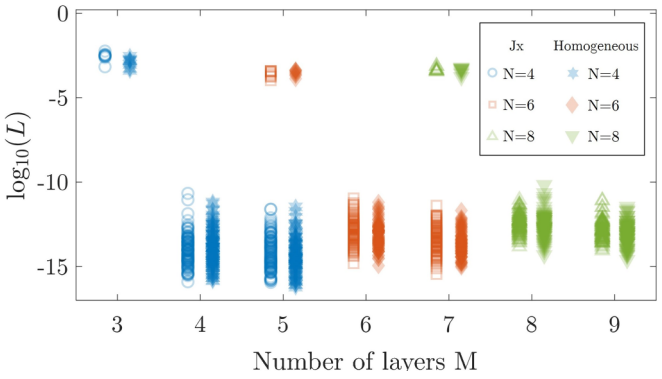

FIG. 2. Error norm $\log_{10}(L)$ obtained from the optimization routine for the J_x (open markers) and homogeneous (filled markers) lattice. For both cases, the matrix dimension has been fixed to $N = 4, 6, 8$, whereas the number of layers for each case is $M = N - 1$, $M = N$, and $M = N + 1$.

the tuple of parameters used in the factorization (1) to reconstruct the target matrix. To determine the number of layers M and the parameter set $\boldsymbol{x}$, we define the error norm as the positive semidefinite function

$$L(\boldsymbol{x}) = \frac{\|\mathcal{U}(\boldsymbol{x}) - \mathcal{U}_t\|^2}{N^2}. \tag{5}$$

If, for some $\boldsymbol{x}$, the error norm minimum is zero, $L(\boldsymbol{x}) = 0$, the factorization (1) exactly reconstructs the target matrix $\mathcal{U}_t$. Since $M = N$ is the minimum number of layers (equivalently $N^2 + N - 1$ parameters), the factorization $\mathcal{U}(\boldsymbol{x})$ poses an overparameterized problem, the solution of which $(\boldsymbol{x})$ may not be unique. Thus, any set $\boldsymbol{x}$ that produces an error norm below a prescribed tolerance is accepted as a solution. For this task, we focus on the Levenberg-Marquardt algorithm, suitable for least-squares problems such as the one defined by the error norm (5), proved useful in other similar optimization tasks [16,17]

Remark 4. Because of the numerical nature of the optimization routine, no set of parameters renders L exactly zero. Thus, one has to impose a performance tolerance $\delta > 0$ so that the parameter set $\boldsymbol{x}$ is said to reconstruct $\mathcal{U}_t$ whenever $L \leqslant \delta$.

To avoid any bias in the choice of target matrices, we randomly construct N_T target matrices generated through the Haar measure [46]. The error norm for each target matrix is optimized by fixing M and running the optimization routine until either $L \leqslant \delta$ or N_{it} iterations have been performed. The Hamiltonians H used for testing purposes correspond to the J_x and the homogeneous lattices. Results of the optimization routine are presented in Fig. 2, with tests run for $N = 4, 6, 8$ and $M = N - 1, N, N + 1$. Although it was previously established that $M \geqslant N$, we perform the optimization for $M = N - 1$ to identify any transition in the behavior of L. $N_T = 100$ target matrices were tested for each configuration. In all testing cases, the error norm drastically drops at $M = N$, and no further improvement is found for $M = N + 1$. This reveals that such a transition indeed occurs for $M = N$, which was set as the required minimum number of layers to achieve universality for Eq. (1).

C. All-optical logic gate circuit and simulation

The proposed architecture is examined by considering $N = 3$ ports so that 11 parameters shall be optimized, that is, 9 phase shifters and 2 waveguide lengths. Furthermore, the J_x lattice Hamiltonian is used as the exponential Lie algebra generator H. This particular choice is handy since its eigenvalues $\lambda_n^{(J_x)} = n$, rendering a unitary evolution that is periodic: $e^{i(\ell+2\pi)H} \equiv e^{i\ell H}$. That is, the lattice length becomes $\ell \mod 2\pi$. Thus, even if the optimization routine produces a negative or a large value of ℓ, we can always find the equivalent one: $\ell \in (0, 2\pi]$. In this form, we do not need to constrain the optimization routine, which speeds up the optimization process.

As a particular example, we consider constructing an all-logical logic gate device. Indeed, such a task has been achieved on combined gain and loss in an optical fiber [32] and stub optical lattices showcasing a flat band in the dispersion relations [33]. In the former, a nonunitary process is required to account for a lossy system, whereas the second approach involves a multistack structure that renders a decorated photonic lattice.

The proposed approach achieves logic gate operations using a lossless optical circuit design on a single stack layout. To this end, we consider the noncanonical orthonormal basis

$$\vec{v}_1 = \frac{(1,-1,0)}{\sqrt{2}}, \quad \vec{v}_2 = \frac{(1,1,-\sqrt{2})}{2}, \quad \vec{v}_3 = \frac{(1,1,\sqrt{2})}{2}$$

so that the target unitary becomes $\mathcal{U}_t = (\vec{v}_1^T, \vec{v}_2^T, \vec{v}_3^T)$. The corresponding reconstructed matrix $\mathcal{U}(\boldsymbol{x})$ is represented through Eq. (1) after proper optimization of the involved parameter set $\boldsymbol{x}$.

The photonic circuit performing the logic gate operation is divided into two parts. In the first stage, a series of programmable Mach-Zehnder interferometers (MZIs) controlled by the phase shifters $\chi_{1,2}$ and $\theta_{1,2}$ is introduced so that the input laser E_{in} splits into the inputs $y_{1,2,3}$ used for the logic gate operation, where $y_i \in \mathbb{C}$, $1 \leqslant i \leqslant 3$; see the dotted rectangle in Fig. 3. Here, $y_{1,2}$ are the logic ports to be processed, whereas y_3 is used as a control port to control the logic gate operation. In the second stage, the photonic unit comprises the interlaced structure (1), implemented through waveguide arrays and passive phase elements; see the dashed rectangle in Fig. 3. This unit processes the inputs $y_{1,2,3}$ into the required logic operation at the output ports $z_{1,2,3}$.

Each interlacing unitary matrix is implemented through coupled waveguide arrays of different lengths. The waveguides are built up on a silicon-on-silica structure, where the core (Si) and the surrounding silica cladding (SiO_2) refractive indexes are $n_{\text{co}} = 3.41$ and $n_{\text{cla}} = 1.4711$, respectively. More specifically, the waveguide cores have a 500 nm width and 200 nm height, surrounded by a silica substrate. This enables the generation of only the fundamental TE mode. Full-wave simulations are computationally expensive to implement; we thus approximate the three-dimensional (3D) waveguide system to an equivalent two-dimensional model that carries the same information as the 3D one. This is done using *effective index theory*, from which one obtains the parameters $n_c^{(\text{eff})} = 2.71$ for a monochromatic input source at 1550 nm. An array of Mach-Zehnder interferometers is coupled to the

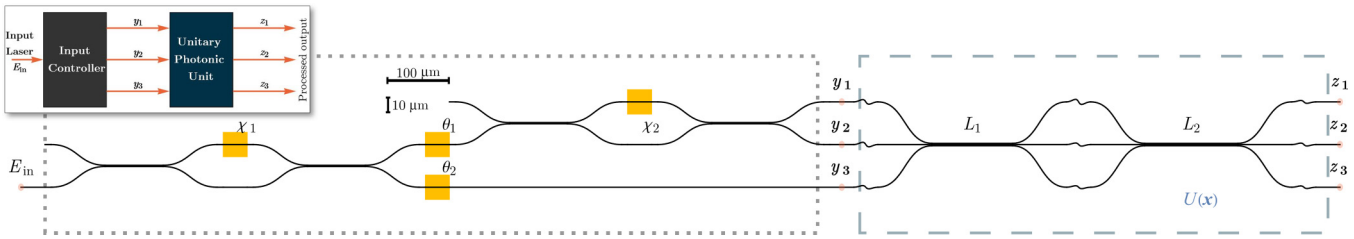

FIG. 3. Block diagram and photonic circuit sketch for the proposed logic gate operation. A single input field E_{in} excites the architecture, producing the logic gate input fields $y_{1,2,3}$ during the input controller stage (dotted rectangle) by tuning the active phase shifters χ_1, χ_2, θ_1, and θ_2 (yellow boxes). The latter inputs are then processed in the photonic unitary unit constructed through Eq. (1) (dashed rectangle). Here, the physical waveguide coupling lengths are $L_j := \widetilde{\kappa}\ell_j$, with $\widetilde{\kappa}$ a design scaling factor and ℓ_j the optimized length parameters.

architecture input to individually manipulate the input ports $y_{1,2,3}$ from a single source; see Appendix for details.

The complete integrated photonic circuit used in the simulations is sketched in Fig. 3. Here, $L_{1,2} = \widetilde{\kappa}\ell_{1,2}$ is the physical lattice coupling length, with $\widetilde{\kappa} \approx (280/\pi)\,\mu\text{m/rad}$ and $\ell_{1,2}$ the lengths obtained from the optimization routine. Note that the first stage of the architecture has a series of MZIs that split the input field E_{in} into the required input ports $y_{1,2,3}$. Each MZI comprises two 50/50 directional couplers with coupling lengths of 96 μm and separated by 500 nm (edge-to-edge distance). Likewise, the waveguide array separation (edge-to-edge) is set to 500 nm, whereas the coupling lengths L_j are determined once the optimization is performed.

The phase shifters $\chi_{1,2}$ allow for tuning the desired input in $\mathcal{U}_t$, whereas the phase shifters $\theta_{1,2}$ are introduced to compensate for any phase change produced during the amplitude modulation. Tunable phase elements can be introduced using phase-change materials [39], where a phase modulation as compact as 11 μm per π radians is feasible. In turn, waveguide rerouting is used to introduce the passive phase delays $\phi_j^{(n)}$ extracted from the optimization.

The phase shifters are operated according to the rules shown in Table I to produce the required input and output operation. The control port y_3 is accordingly manipulated to switch the logic gate operation. For $y_3 = 0$, the XOR and OR operations are reproduced at ports z_1 and $z_{2,3}$, respectively. A second operation is established for $y_3 \neq 0$, where the logic gates nand and and are now performed in ports z_2 and z_3, respectively, as long as the threshold values are correctly fixed. We particularly focus on the case $y_3 = \sqrt{2}y_2$, with $y_2 \neq 0$, so that $z_3 = 0$ for $y_1 = y_2$, which is required to perform the xor and nand gates. This particular case is possible by tuning $(\chi_1, \chi_2) = (\widetilde{\chi}_0, \pi)$ and $(\chi_1, \chi_2) = (\pi/2, \pi/2)$, where $\widetilde{\chi}_0 = \arctan(\sqrt{2})$.

To illustrate the functionality of the proposed architecture, the corresponding full-wave simulations are shown in Fig. 4(a) for each of the settings presented in Table I. Here, the simulated power distribution throughout the device is depicted for all settings, where the unitary input and output ports, y_j and z_j, respectively, are shown, allowing for proper operation to be tracked. This shows the light routing for all the phase shifter configurations. For this particular device, the phase information is irrelevant. Thus, no further measurements other than the output power $P_j^{(\text{out})} \propto |z_j|^2$ are required.

In contradistinction to binary operations, the measured optical power $P_j^{(\text{out})} \propto |z_j|^2 \geqslant 0$. Thus, to establish a binary-like operation, we define the threshold values Th_j for each output port z_j so that $P_j^{(\text{out})} < Th_j$ and $P_j^{(\text{out})} \geqslant Th_j$ can be interpreted as logic 0 and 1 readouts, respectively, for $j \in \{1, 2, 3\}$. Furthermore, the threshold values must be fixed to account

TABLE I. Photonic unit normalized power inputs ($|y_j|^2$) and power outputs ($|z_j|^2$), for $j \in \{1, 2, 3\}$, used to perform the logic gate operation. The operation settings are shown for different configurations of the tunable phase duple (χ_1, χ_2), where $\widetilde{\chi}_0 = 2\arctan(\sqrt{2})$.

(χ_1, χ_2)	$\lvert y_1\rvert^2$	$\lvert y_2\rvert^2$	$\lvert y_3\rvert^2$	$\lvert z_1\rvert^2$	$\lvert z_2\rvert^2$	$\lvert z_3\rvert^2$
No E_{in}	0	0	0	0	0	0
$(0, 0)$	1	0	0	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{4}$
$(0, \pi)$	0	1	0	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{4}$
$(0, \frac{\pi}{2})$	$\frac{1}{2}$	$\frac{1}{2}$	0	0	$\frac{1}{2}$	$\frac{1}{2}$
				XOR	OR	OR
				$\text{Th}_1 < \frac{1}{2}$	$\text{Th}_2 < \frac{1}{4}$	$\text{Th}_3 < \frac{1}{4}$
(χ_1, χ_2)	$\lvert y_1\rvert^2$	$\lvert y_2\rvert^2$	$\lvert y_3\rvert^2$	$\lvert z_1\rvert^2$	$\lvert z_2\rvert^2$	$\lvert z_3\rvert^2$
(π, any)	0	0	1	0	$\frac{1}{2}$	$\frac{1}{2}$
$(\widetilde{\chi}_0, 0)$	$\frac{1}{3}$	0	$\frac{2}{3}$	$\frac{1}{6}$	$\frac{1}{12}$	$\frac{9}{12}$
$(\widetilde{\chi}_0, \pi)$	0	$\frac{1}{3}$	$\frac{2}{3}$	$\frac{1}{6}$	$\frac{1}{12}$	$\frac{9}{12}$
$(\frac{\pi}{2}, \frac{\pi}{2})$	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{2}$	0	0	1
				XOR	NAND	AND
				$\text{Th}_1 < \frac{1}{6}$	$\text{Th}_2 < \frac{1}{12}$	$\frac{9}{12} < \text{Th}_3 < 1$

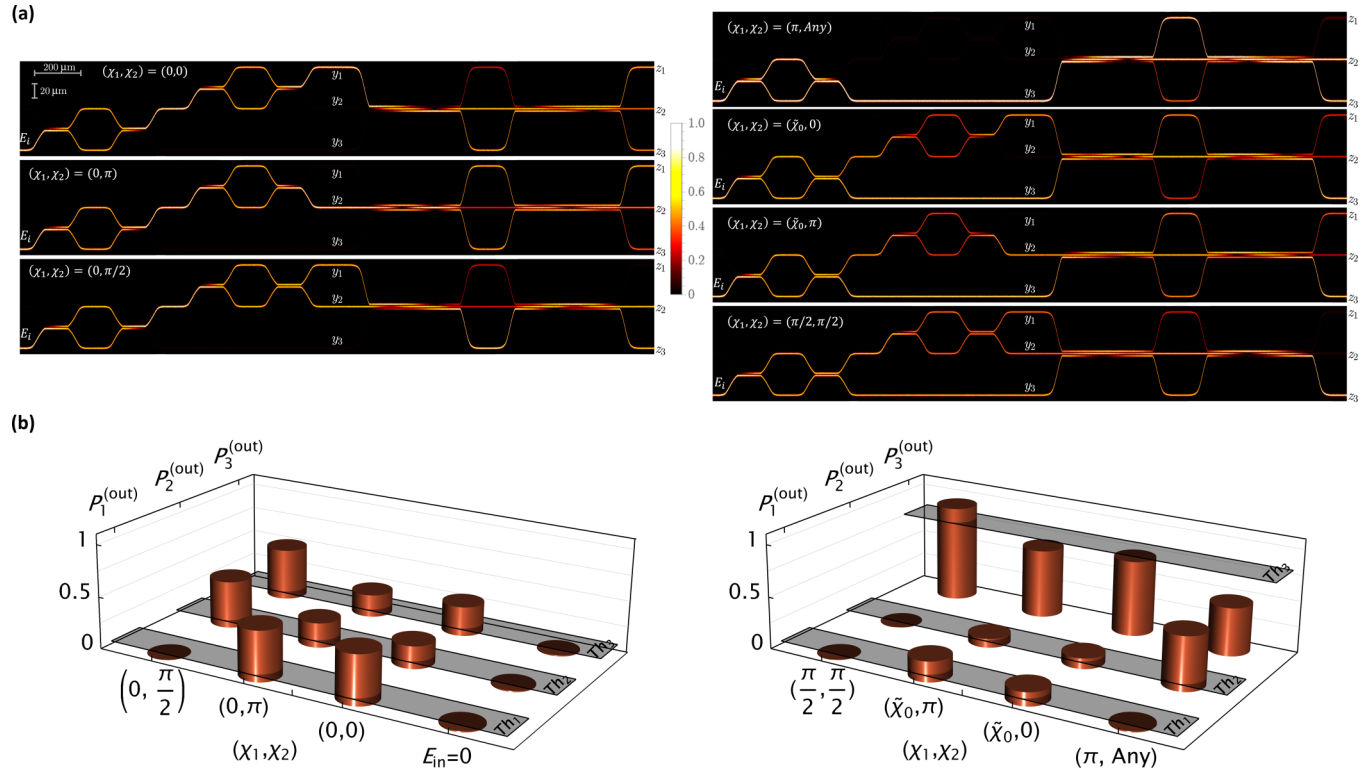

FIG. 4. (a) Density plot of $|\vec{E}(x,y)|$ computed from full-wave simulations for different operation settings of the duple (χ_1,χ_2). (b) Normalized output power $P_j^{(out)} \propto |z_j|^2$ for the configurations in Table I and the corresponding threshold values Th_j, for $j \in \{1,2,3\}$.

for deviations due to mild manufacturing imperfections and design flaws. The ideal thresholds shown in Table I provide us with the allowed threshold intervals. Indeed, Fig. 4(b) shows the simulated measurement for all the operation settings. The horizontal strips denote the prefixed normalized threshold values Th_j, set to recover the desired logic gate functionality and to account for deviations from the ideal case due to channel cross-talk, mild defects, and losses around the bending arms. For instance, in the case $(\pi/2,\pi/2)$, no power is expected at the ports $z_{1,2}$, yet a small amount is observed in the simulations. The proper readouts are gathered by fixing the thresholds $\mathrm{Th}_1 = \mathrm{Th}_2 = 0.075$, whereas $\mathrm{Th}_3 = 0.8$ allows recovering the and operation at the port z_j for $y_3 \neq 0$.

IV. CONCLUSION

The present work provides a formal proof for the universality of photonic interlacing architectures in representing the discrete linear unitary group $U(N)$. It demonstrates that elements of $U(N)$ can be decomposed into a sequence of N-parameter phases alternating with one-parameter propagators of a lattice Hamiltonian, with a finite number of layers. Numerical tests using Haar random unitary matrices as targets reveal that specifically N layers are required to reconstruct the targets with error norms within the numerical error regime.

The proposed architecture can be implemented using basic photonic circuit components and is capable of reconstructing arbitrary unitary matrices. Unlike other similar structures, this solution requires one less layer, resulting in an $M = N$layered design instead of $M = N + 1$. This reduction is achievable because we reach the minimum number of trainable parameters necessary to cover the $U(N)$ group, which is$N^2 - 1$ when accounting for a single global phase. In our design, we can factor out one global phase out of $M - 1 \equiv N - 1$ layers [17], allowing for $N - 1$parameters per phase layer. Additionally, the length parametersℓ_j are also trainable, resulting in a total of N^2 parameters.

Numerical tests and full-wave simulations support the theoretical findings, confirming the potential of this approach for developing energy-efficient and compact on-chip photonic devices for various passive and active applications. Among the passive applications, we demonstrate the feasibility of designing an all-optical logic gate using a lossless and passive optical circuit. This design is unitary (power-conserving), entirely passive, and straightforward, making it compatible with the typical manufacturing processes used by open-access foundries, without the need for any specialized fabrication process.

The proposed all-optical logic gate provides a simplified alternative compared to other methods discussed in the literature, such as lossy optical fiber approaches [32] and the use of stub multistacked optical lattices [33]. Additionally, this design is compatible with other passive photonic solutions employed for beam steering and direction-of-arrival detection tasks [22].

The present design is not solely limited to passive implementations. Although the coupling length of the fabricated waveguide arrays cannot be tuned once the sample is manufactured, there are active solutions to induce changes in the effective coupling length. This has been experimentally achieved in tunable waveguide arrays [47,48], where thermo-

optical effects change the coupling coefficients of the couplers as $\kappa_p \to \kappa_p'$. If all the coupling coefficients at the mth layer are simultaneously adjusted so that $\kappa_p' = \gamma_m \kappa_p$, where $\gamma_m > 0$ is a tunable scaling factor, then this scaling factor can be incorporated into the coupling length. This leads to the modified trainable length parameter $\ell_m' = \gamma_m \ell_m$, for $m \in \{1, \ldots, M = N\}$.

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DATA AVAILABILITY

No data were created or analyzed in this study.

APPENDIX: PHOTONIC INPUT STATE GENERATOR

The circuit design presented in the main manuscript is divided into two parts: the programmable MZI array that produces the desired input signal and the passive photonic unit that processes the input and produces the logic gate operation at the output. In the current design, each MZI is composed of two passive directional couplers and two active phase shifters (yellow boxes in Fig. 3). Each of the latter components is described through a unitary matrix. Particularly, the wave evolution in each directional coupler is determined by the coupled-mode theory, leading to

$$U_{\mathrm{DC}} = e^{-i\ell\kappa\sigma_1} \equiv \cos(\kappa\ell)\sigma_o - i\sin(\kappa\ell)\sigma_1,$$

with σ_0 the 2×2 identity matrix and $\sigma_1 \equiv \sigma_x$ the corresponding x projection of the Pauli matrix. In the latter, it is assumed that both waveguides have the same dimensions so that any additional phase mismatch can be disregarded, and κ is proportional to the overlap integral of the guided modes in each waveguide [49]. Here, the waveguide width and thickness are 500 and 220 nm, respectively. The edge-to-edge distance between waveguides has been fixed to 500 nm, which, combined with a coupling length of 96 μm, renders a 50/50 or power divider operation ($\kappa\ell = \pi/4$). Additionally, the phase shifter layers are represented by diagonal matrices, and the input vector is fixed as $(0, 0, E_{\mathrm{in}})^T$, where the input field enters the lowest channel (third input). From the previous considerations and following the circuit shown in Fig. 3, it is straightforward to show that the photonic unit inputs take the form

$$y_1 = e^{i\left(\theta_1 + \frac{\chi_1+\chi_2}{2} - \pi\right)} \cos\left(\frac{\chi_1}{2}\right) \sin\left(\frac{\chi_2}{2}\right),$$
$$y_2 = e^{i\left(\theta_1 + \frac{\chi_1+\chi_2}{2} - \pi\right)} \cos\left(\frac{\chi_1}{2}\right) \cos\left(\frac{\chi_2}{2}\right),$$
$$y_3 = e^{i\left(\theta_2 + \frac{\chi_1}{2} - \frac{\pi}{2}\right)} \sin\left(\frac{\chi_1}{2}\right).$$

It is worth noting that the phase shifters $\chi_{1,2}$ produce amplitude modulation at $y_{1,2,3}$ while introducing additional phases. To address this, the extra phase shifters $\theta_{1,2}$ were included to compensate for any other phase change produced during the modulation or waveguide routing. Thus, elements $\theta_{1,2}$ are a function of $\chi_{1,2}$, which we fix as $\theta_1 = (\pi - (\chi_1 + \chi_2)/2)$ and $\theta_2 = (\pi - \chi_1)/2$ to remove any extra phase. From this, the results shown in Table I follow straightforwardly.

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